On-Chip Buck Converter with Spiral Ferrite Inductor and Reducing IR Drop in 3D Stacked Integration

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***Abstract*— In this paper, two topics about an on-chip DC-DC buck converter are described. First, the buck converter with an inductor on interposer is investigated for mobile applications. Simulation results indicate that the efficiency of the buck converter is improved by introducing a ferrite film to the inductor. Next, a circuit technique to reduce IR drop in 3D stacked integration using the buck converter is proposed. In this paper, 3D stacked-die system, which consists of stacked dies and silicon interposer, is fabricated and measurement results show that the proposed technique achieves 78% decrease in IR voltage drop compared with the conventional approach.**

Keywords*— *3D stacked integration, Ferrite, Interposer, IR Drop, On-chip DC-DC buck converter

I. INTRODUCTION

A buck converter is often used as a DC-DC voltage down converter, since the buck converter provides high conversion efficiency at rather high current output among different types of DC-DC voltage down converters.

In this paper, the following two topics about the buck converter for mobile applications and 3D IC's are described. 1) Efficiency improvement of the buck converter by introducing high permeability material to an inductor on interposer is investigated [1]. 2) A circuit technique to reduce IR drop in 3D stacked integration using the buck converter is presented [2].

II. EFFICIENCY INCREASE IN BUCK CONVERTER BY INTRODUCTION OF HIGH PERMEABILITY MATERIAL TO INDUCTOR ON INTERPOSER

A buck converter requires an inductor. Since mobile devices have been currently smaller and thinner, miniaturization of the inductor used for the buck converter is required. Although it is one of promising solutions that inductors are implemented in IC package or interposer, the inductance and Q factor of such inductors are smaller, which results in worsening the efficiency of the buck converter. Therefore, introduction of high permeability material to the inductor is expected to improve the efficiency. In this paper, the efficiency of the buck converter using inductor on interposer with a ferrite film is investigated as shown in Fig. 1.

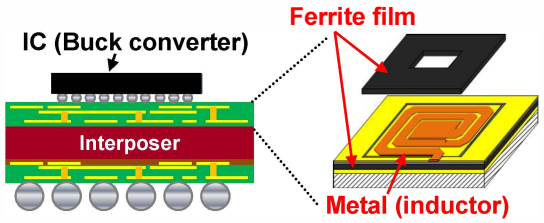

Fig. 1. Inductor on Interposer with ferrite film.

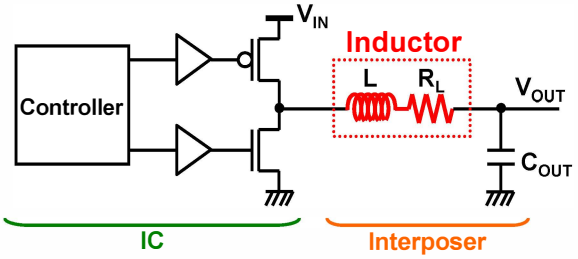

Fig. 2. Circuit schematic of buck converter with inductor on interposer.

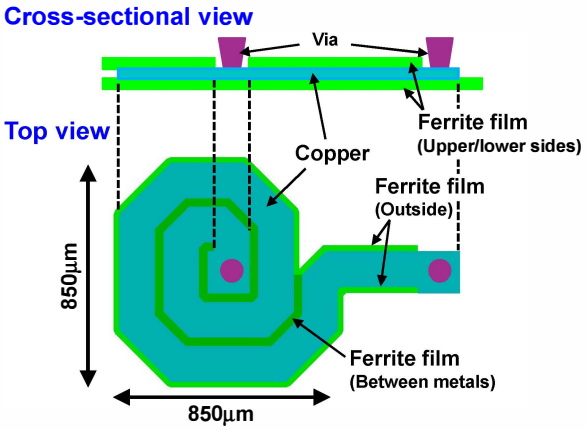

Fig. 3. Layout of spiral ferrite inductor.

Fig. 2 shows a circuit schematic of the buck converter evaluated in this paper. A controller circuit, buffers, and drivers of the buck converter are implemented in the IC, while an inductor is fabricated in the interposer using metal interconnects of the interposer. The layout of the inductor is illustrated in Fig. 3. In this paper, the

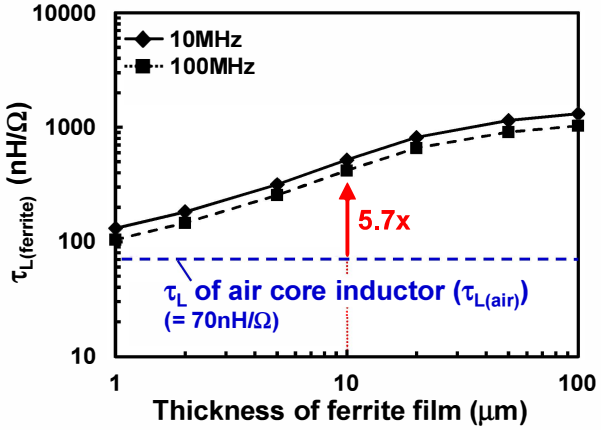

Fig. 4. Dependence of τ_L of ferrite inductor and air core inductor.

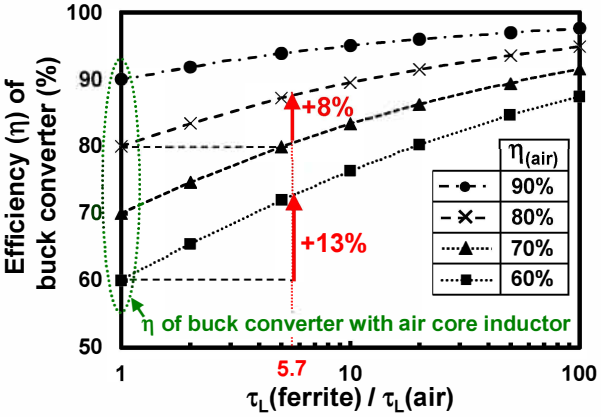

Fig. 5. Efficiency increase of buck converter by using ferrite inductor.

inductance of the inductor is simulated by a 3D electromagnetic simulator (Agilent EMPro).

According to [3], the efficiency of the buck converter depends on τ_L, which is given by

$$\tau_L = L/R_L, \quad (1)$$

where L and R_L are the inductance and the DC resistance of the inductor, respectively. As τ_L increases, the efficiency of the buck converter improves. Therefore, τ_L is evaluated to investigate the efficiency improvement of the buck converter by using the ferrite inductor in this paper.

Fig. 4 shows the dependence of τ_L on the thickness of the ferrite film. $\tau_{L(ferrite)}$ and $\tau_{L(air)}$ are τ_L of the ferrite inductor and the air core inductor, respectively. When the thickness of the ferrite film is 10μm, $\tau_{L(ferrite)}$ is 5.7 times larger than $\tau_{L(air)}$. Fig. 5 shows the efficiency improvement of the buck converter by using the inductor with the ferrite film when the input/output voltage of the buck converter is 1.8/1.0V, the output current is 1.0A, and the switching frequency is 100MHz. By using the inductor with the 10μm-thick ferrite film, the efficiency of buck converter is improved by 13% and 8% when the efficiencies of buck converter with the air core inductor are 60 and 80%, respectively.

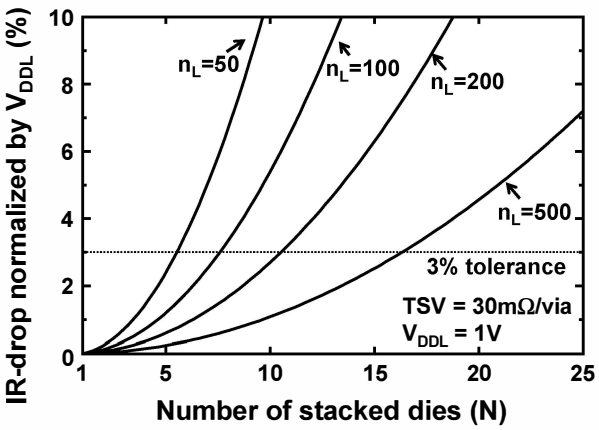

Fig. 6. Calculated IR drop in 3D integration. n_L is the total number of TSV's per die used for power delivery. Each die is assumed to consume 1A.

III. Reducing IR Drop in 3D Integration using Buck Converter on Top Die Scheme

Recently, 3-dimensional integration based on TSV's (through silicon vias) have been explored extensively for achieving low power and high performance to break the limit of single-chip 2D integration. The TSV and associated bump connection structure (TSV link) inherently have parasitic resistance and thus the supply voltage is exposed to IR drop due to the TSV link resistance [4,5]. The increase of IR drop is shown in Fig. 6. The IR drop is calculated as a function of the number of stacked dies (N) and the total number of TSV's per die (n_L) used for power delivery. If allowable IR drop is assumed to be 3% of the nominal power supply voltage (V_{DDL}), it is seen from the figure that hundreds of TSV's are needed to make the IR drop within the tolerance.

In order to reduce the IR drop due to TSV, we proposed a Buck Converter on Top die (BCT) scheme [2]. Figs. 7 and 8 show a typical 3D integration with the conventional power supply scheme and the proposed BCT scheme. In the conventional power supply scheme (Fig. 7), all the current is supplied from a buck converter which is either implemented on the bottom die or is implemented as a separate die residing external to the 3D stacked dies. Since the top die can be far from the power supply circuit, the IR drop gets large as the current must go through many serially-connected TSV's.

In contrast, a buck converter is added on the topmost die (Die N) in the proposed BCT scheme, and the current to an upper half of the 3D integration (Die (N/2)+1 ~ Die N) is delivered from the added BCT (Fig. 8). Each buck converter on the top die and the bottom die stably supply the specified voltage and the current to the furthest die (Die N/2, Die (N/2)+1) from a buck converter through less number of TSV's compared with the conventional case. Thus, the maximum IR drop gets smaller and improved.

In order to evaluate the effectiveness of the proposed BCT scheme, we fabricated 3D stacked-die system, which consists of stacked dies and silicon interposer. Its

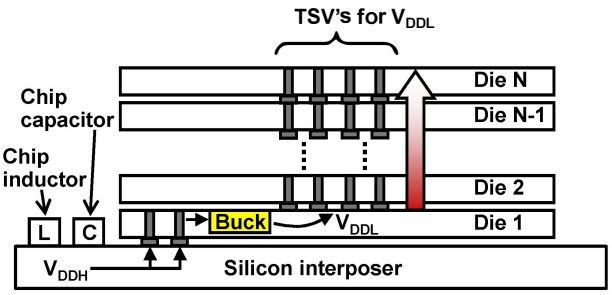

Fig. 7. Conventional power supply scheme.

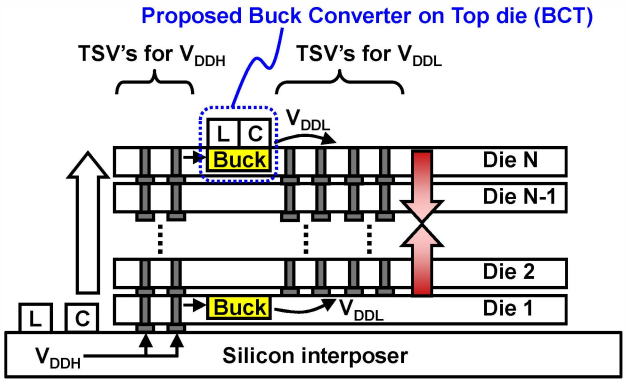

Fig. 8. Proposed Buck Converter on Top die (BCT) scheme.

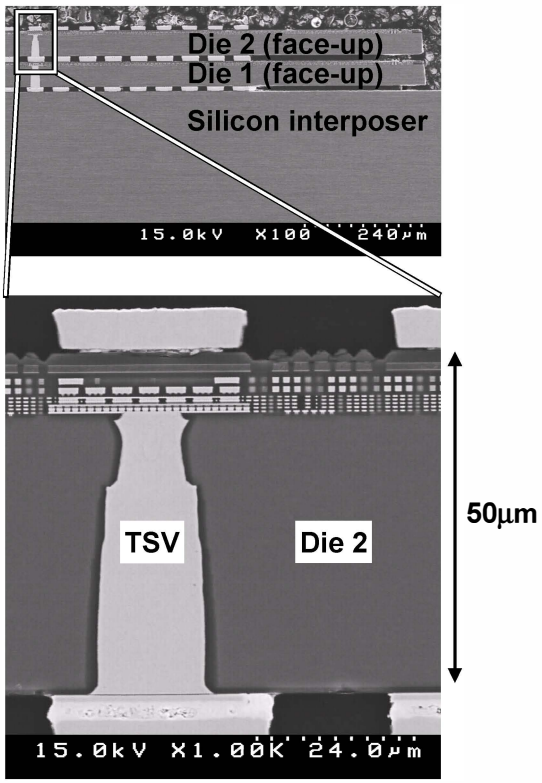

Fig. 9. Cross sectional view of 3D integrated system. The upper photo is a global view and the lower photo is a magnified view around a TSV.

cross sectional view is shown in Fig. 9. Two face-up dies are stacked on top of a silicon interposer with a via-last process. The diameter of the TSV is 20µm and the minimum pitch of the TSV's is 50µm. The resistance of a TSV link is 29mΩ (typical). Although only two dies are stacked physically as shown in Fig. 9, 8-die stack case is emulated by the daisy chain of TSV's in two stacked dies in this paper.

The technology used to implement circuits is 8-metal, 90nm CMOS. The typical operation voltage for logic transistors is 1.2V while I/O transistors accept typically 3.3V. Thus, 3.3V is used for V_{DDH} and 1.2V for V_{DDL} in the 3D stacked-die system design.

A microphotograph of the fabricated two stacked dies mounted on top of a silicon interposer is shown in Fig. 10. The silicon interposer is needed to accept 50µm pitch TSV's, which cannot be realized by a PCB board whose design rule is loose. Two identical buck converters are implemented on a die to expect yield improvement in this 3D stacked-die system.

The photo in Fig. 11 shows an assembled 3D stacked-die device. A chip inductor and two chip capacitors are directly mounted on the top die. The blue part in the picture is a silicon interposer. The chip inductor and capacitor for a buck converter is 3.9nH and 1µF, respectively. These values are chosen to optimize the buck converter design following the design theory described in [3].

Fig. 12 shows the measured and simulated IR drop in the fabricated 3D stacked-die system. The simulation

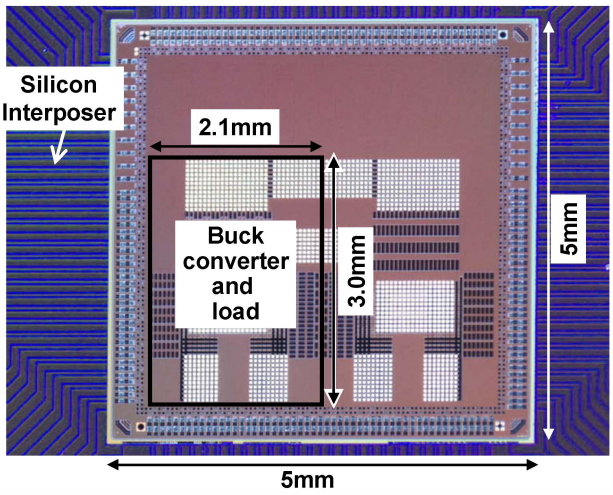

Fig. 10. Two stacked dies using TSV's are mounted on top of a silicon interposer.

results are obtained using SPICE. Although the voltage of only selected locations can be monitored in the manufactured 3D stacked-die system due to TSV constraints, the simulation results can be used to extrapolate the measured points since the simulation results agree very well with the measured results as is seen in Fig. 12. It is shown that the proposed scheme achieves 78% decrease in IR voltage drop compared with the conventional approach. That is, the IR drop is reduced to less than 1/4 by introducing the BCT scheme.

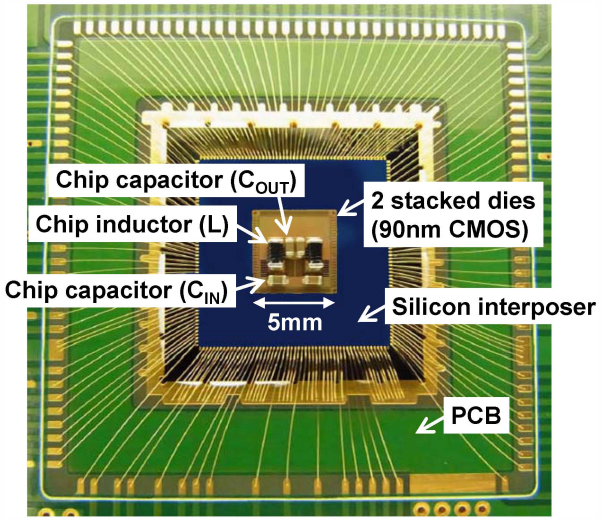

Fig. 11. Photograph of assembled system on a PCB board. Chip inductor and chip capacitor are mounted directly on top of stacked dies at the center of the photo.

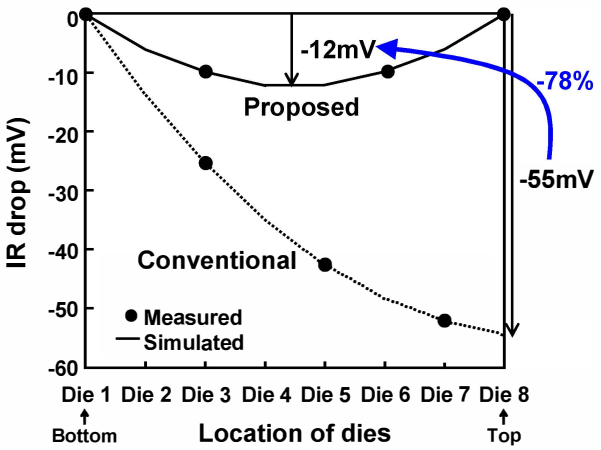

Fig. 12. Measured IR drop and simulated results.

IV. Conclusions

In this paper, the two topics about the on-chip buck converter were described. First, we investigated the efficiency improvement of the buck converter by introducing high permeability material to an inductor on interposer. The simulation results indicated that the efficiency of the buck converter is improved by 8% by using the inductor with the 10μm-thick ferrite film when the efficiency of the buck converter with the air core inductor is 80%. Next, we proposed the buck converter on top die (BCT) scheme to reduce IR drop in 3D stacked integration. 3D stacked-die system, which consists of stacked dies and silicon interposer, was fabricated and measurement results showed that the proposed BCT scheme achieves 78% decrease in IR voltage drop compared with the conventional approach.

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References

[1] H. Fuketa, Y. Shinozuka, K. Ishida, M. Takamiya, T. Fujii, H. Shimizu, K. Kobayashi, T. Sato, and T. Sakurai, "Efficiency Increase in On-Chip Buck Converter by Introduction of High Permeability Material to Inductor on Interposer," in Proc. *International Conference on Ferrites (ICF)*, p. 75, 2013.

[2] Y. Shinozuka, H. Fuketa, K. Ishida, F. Furuta, K. Osada, K. Takeda, M. Takamiya, and T. Sakurai, "Reducing IR Drop in 3D Integration to Less Than 1/4 Using Buck Converter on Top Die (BCT) Scheme," in Proc. *IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 210-215, 2013.

[3] G. Schrom, P. Hazucha, F. Paillet, D. S. Gardner, S. T. Moon, and T. Karnik, "Optimal Design of Monolithic Integrated DC-DC Converters," in Proc. *IEEE International Conference on IC Design and Technology (ICICDT)*, pp.1-3, 2006.

[4] P. Singh, R. Sankar, X. Hu, W. Xie, A. Sarkar, and T. Thomas, "Power Delivery Network Design and Optimization for 3D Stacked Die Designs," in Proc. *IEEE International 3D System Integration Conference*, pp. 1-6, 2010.

[5] M. Jung and S. Lim, "A Study of IR-Drop Noise Issues in 3D ICs with Through-Silicon-Vias," in Proc. *IEEE International 3D System Integration Conference*, pp. 1-6, 2010.