92% Start-up Time Reduction by Variation-Tolerant Chirp Injection (CI) and Negative Resistance Booster (NRB) in 39MHz Crystal Oscillator

Shunta Iguchi, Hiroshi Fuketa, Takayasu Sakurai, and Makoto Takamiya
University of Tokyo, Tokyo, Japan

Abstract

To reduce the start-up time of a crystal oscillator (XO), a chirp injection (CI) and a negative resistance booster (NRB) are proposed. By combining CI and NRB, the measured start-up time of a 39-MHz XO in 180-nm CMOS is reduced by 92% from 2.1ms to 158µs, which is the shortest time in the published XO's. The measured start-up time variations due to the ±20% supply voltage change or the temperature change are less than 13%.

Introduction

To reduce the power consumption of RF transceivers, an intermittent operation and an agile transition between a sleep mode and an active mode are required. The start-up time (t_{START}) of the RF transceiver from the sleep mode to the active mode is limited by a crystal oscillator (XO) for the RF carrier generation, because t_{START} of XO is the longest in the RF transceiver due to a high Q (> 10000) of a quartz crystal. The long t_{START} prevents the agile mode transition and increases power consumption of the RF transceiver. Therefore, in this paper, new start-up time reduction techniques for a 39-MHz XO are proposed.

Start-up Time Reduction Techniques

Fig. 1 shows a strategy to reduce t_{START} of a conventional Pierce XO shown in Fig. 2 (a). t_{START} is determined by the negative resistance ($|R_N|$) and the internal noise (V_{NOISE}) [1]. To reduce t_{START} in this paper, V_{NOISE} is increased by the proposed chirp injection (CI), and $|R_N|$ is temporarily increased by the proposed negative resistance booster (NRB).

In the previously reported constant frequency injection (CFI) [2] shown in Fig. 2 (b), a ring oscillator (RO) is connected to Out and X1 to increase V_{NOISE} during the start-up. RO is calibrated to have the same frequency as XO. CFI, however, will fail to work, because XO has the high Q and the frequency of RO should be the exactly same as that of XO. Even if RO is perfectly calibrated, the frequency of RO drifts due to the variation of the supply voltage (V_{DD}) and the temperature, and CFI fails to work.

To solve the problem, CI shown in Fig. 2 (c) is proposed. In CI, instead of the constant-frequency RO in CFI, a chirp generator is used to increase V_{NOISE}. The chirp is a signal in which the frequency decreases with time. Fig. 3 shows a circuit schematic of the chirp generator. When CI_en changes from low to high, the control voltage (V_{CNT}) of VCO is varied from V_{DD} to 0V. The frequency of the chirp is designed to cross the XO frequency (= 39MHz) considering PVT variations. Therefore, CI is more tolerant to PVT variations than CFI.

To increase $|R_N|$ for reducing t_{START}, NRB is added to CI and the finally proposed XO is shown in Fig. 2 (d). Fig. 4 shows a timing chart of the proposed XO. When a wake-up signal is received, both CI_en and NRB_en are activated. While CI_en is high, Chirp is injected to Out and X1. When NRB_en is high, Inv3 is added to Inv1 to increase $|R_N|$, thereby reducing t_{START}. In this paper, t_{START} is defined as the time from the wake-up signal to the timing when the amplitude of Out is equal to 90% of that of the steady-state Out. The activation period of CI_en (t_{CI}) is shorter than that of NRB_en (t_{NRB}).

Experimental Results

The 4 XO's in Fig. 2 are fabricated in 180-nm CMOS process and compared. The Inv1 in Fig. 2 is designed to have an oscillation allowance of 5 for XO. Fig. 5 shows a die photo and a layout of the proposed XO with CI and NRB. Table I shows a performance summary of the proposed XO with CI and NRB.

Fig. 6 shows a measured time dependence of the chirp frequency of the chirp generator. The chirp frequency crosses the XO frequency (= 39MHz) across the best and the worst corners. Based on the results, t_{CI} is fixed to 40µs.

Optimum gate width of Inv3 and t_{NRB} for NRB are discussed. Fig. 7 shows a measured gate ratio dependence of t_{START} and the steady-state power in the XO with NRB at infinite t_{NRB}. CI is disabled. The gate width of Inv3 is normalized to that of Inv1. By increasing the gate ratio, $|R_N|$ is increased and t_{START} is reduced at the cost of increasing power. The gate ratio of 13 is used for NRB. In this case, t_{START} is reduced by 87%, while the power increases by a factor of 4.9. Fig. 8 shows a measured t_{NRB} dependence of t_{START} in the XO with NRB. By increasing t_{NRB}, t_{START} is decreased and saturated at t_{NRB} > 160µs. To reduce the power overhead due to NRB, t_{NRB} of 164µs is used.

Fig. 9 shows measured start-up waveforms of the conventional XO (Fig. 2 (a)) and the proposed XO with CI and NRB (Fig. 2 (d)). By combining CI and NRB, t_{START} is reduced by 92% from 2.1ms to 158µs.

To compare the variation tolerance of the 4 XO's in Fig. 2, V_{DD} and the temperature are varied. Fig. 10 (a) shows a measured V_{DD} dependence of t_{START} at 25ºC. The typical V_{DD} is 1.5V and V_{DD} is varied ±20%. Fig. 10 (b) shows a measured V_{DD} dependence of relative variations of t_{START}. The variation of t_{START} is normalized by t_{START} at V_{DD} of 1.5V. t_{START} variation of CFI is much larger than that of CI, because CFI is calibrated at V_{DD} of 1.5V and the RO frequency changes with V_{DD}, which indicates CI is more variation-tolerant than CFI. t_{START} variation of the conventional XO is as high as 201%, while that of the proposed CI and NRB is less than 13%. Fig. 11 shows a measured temperature dependence of t_{START} at V_{DD} of 1.5V. The typical temperature is 25ºC and the temperature is varied from -30ºC to 125ºC. Similar to Fig. 10 (a), t_{START} of CFI is longer than that of CI except for 25ºC, because CFI is calibrated at 25ºC. t_{START} variation of the proposed CI and NRB is less than 7% and the lowest in 4 XO's.

Fig. 12 shows comparisons of t_{START} of 4 XO's at the typical, low V_{DD}, and high temperature conditions. t_{START} is normalized by t_{START} of the conventional XO at each condition. In CFI, the reduction of t_{START} is only 31% at the high temperature condition, while the proposed CI and NRB reduces t_{START} by more than 92% at the all conditions. Therefore, the proposed CI and NRB is variation-tolerant.

Table II shows a comparison with previously reported XO's [3-6]. This work shows the shortest t_{START} of 158µs and achieves the PVT variation tolerance. Thus, the proposed XO with CI and NRB enables the agile mode transition between the sleep and active mode, and reduces the power consumption of the RF transceiver.

Acknowledgment

This work was partly supported by STARC. The VLSI chips were fabricated in the chip fabrication program of VDEC in collaboration with Rohm Corp. and Toppan Printing Corp.

References

[1] A. Rusznyak, JSSC, pp. 259-268, 1987.
[2] Y. Kwon *et al.*, TCAS-I, pp. 324-336, 2012.
[3] Y. Chang *et al.*, JSSC, pp. 421-434, 2012.
[4] R. van Langevelde *et al.*, RFIC Symp., pp. 113-116, 2009.
[5] Data sheet of CC2540, Texas Instruments, [Online].
[6] S. Iguchi *et al.*, VLSI Symp., pp. C142-C143, 2013.

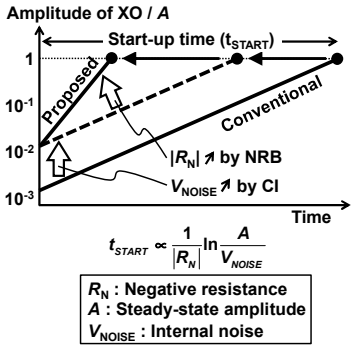

Fig. 1. Strategy to reduce t_{START} of XO.

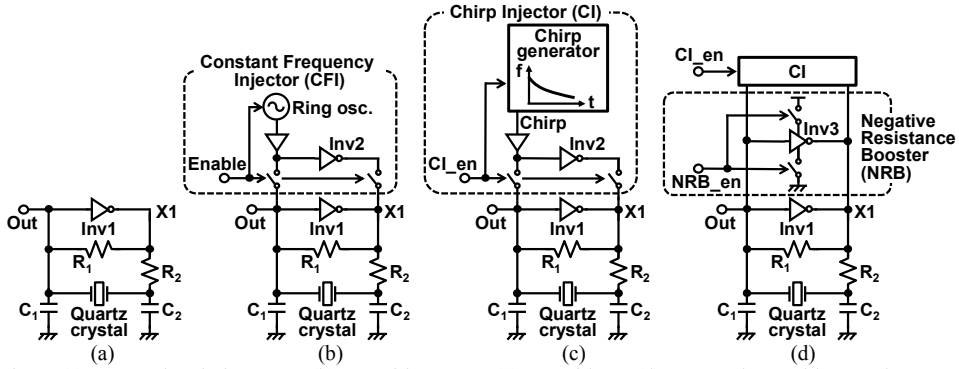

Fig. 2. (a) Conventional Pierce XO. (b) XO with CFI [2]. (c) XO with CI. (d) Proposed XO with CI and NRB.

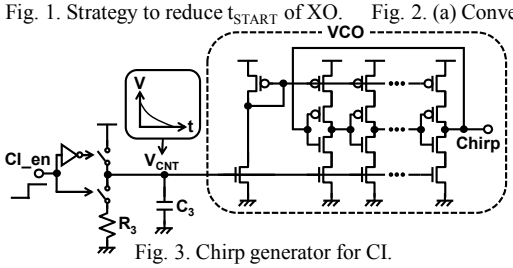

Fig. 3. Chirp generator for CI.

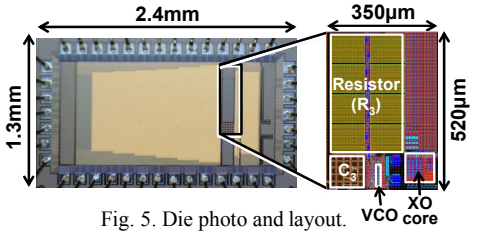

Fig. 5. Die photo and layout.

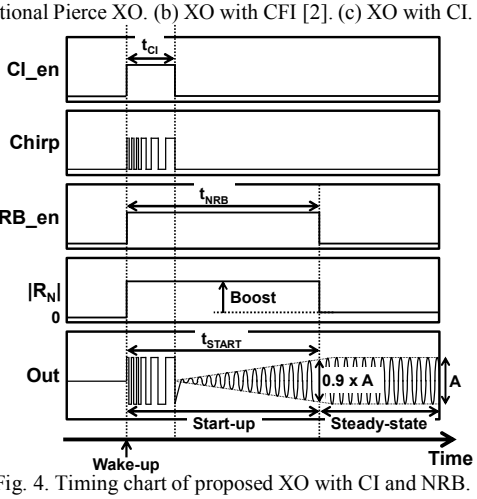

Fig. 4. Timing chart of proposed XO with CI and NRB.

Table I Performance summary.

Frequency	39MHz
CMOS process	180nm
Supply voltage	1.5V
Core area	0.12mm²
R_1	500kΩ
R_2	10Ω
C_1, C_2	12pF, 12pF
Power	181μW
Start-up energy	434nJ
Start-up time (t_{START}) at 1.5V, 25ºC	158μs
t_{START} variation (1.2V to 1.8V) at 25ºC	< 13%
t_{START} variation (-30ºC to 125ºC) at 1.5V	< 7%

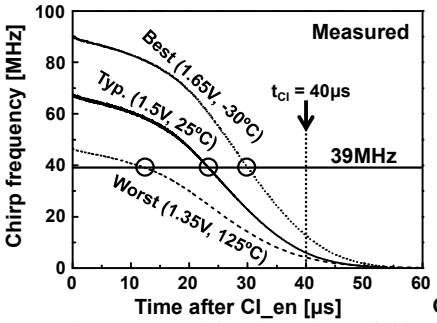

Fig. 6. Measured time dependence of chirp frequency.

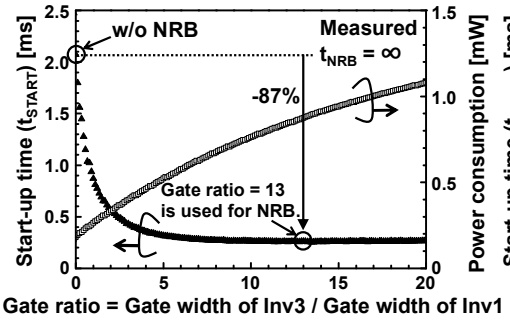

Fig. 7. Measured gate ratio dependence of t_{START} and steady-state power in XO with NRB.

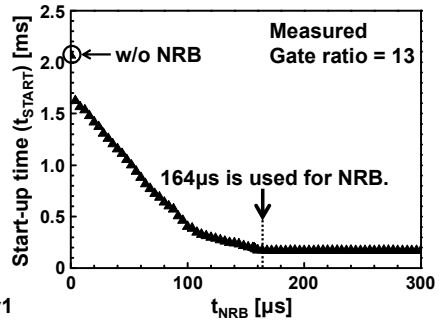

Fig. 8. Measured t_{NRB} dependence of t_{START} in XO with NRB.

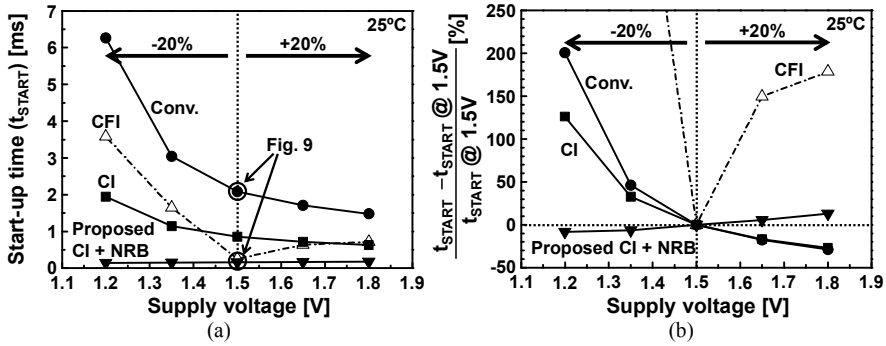

Fig. 10. Measured V_{DD} dependence of (a) t_{START} and (b) relative variations of 4 XO's in Fig. 2 at 25ºC.

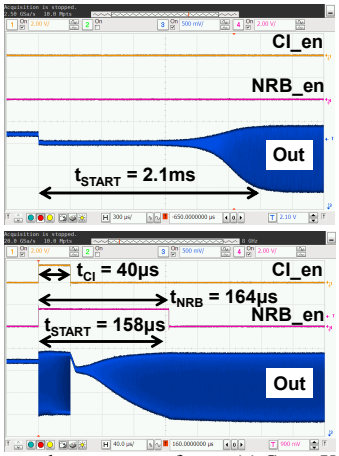

Fig. 9. Measured start-up waveforms. (a) Conv. XO (Fig. 2 (a)). (b) Proposed XO with CI and NRB (Fig. 2 (d)).

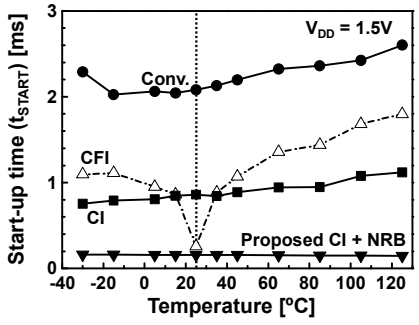

Fig. 11. Measured temperature dependence of t_{START} of 4 XO's in Fig. 2 at V_{DD} = 1.5V.

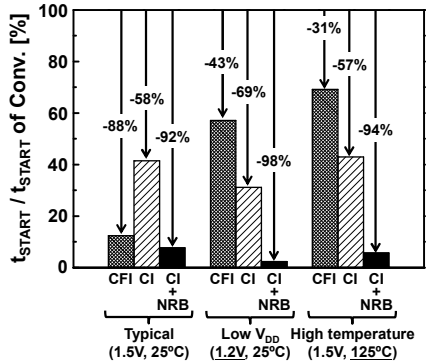

Fig. 12. Comparisons of t_{START} of 4 XO's.

Table II Comparison with previously reported XO's.

		[3]	[4]	[5]	[6]	This work
Frequency	MHz	26	19	32	39	39
CMOS process	nm	65	130	NA	40	180
Supply voltage	V	1.2	1.2	3.0	0.7	1.5
Power	μW	1440	22	180	69	181
Start-up time (t_{START})	μs	3200	1200	250	259	158
t_{START} is robust to PVT variations.		No	No	NA	No	Yes