Design Method of Class-F Power Amplifier With Output Power of −20 dBm and Efficient Dual Supply Voltage Transmitter

Shunta Iguchi, *Student Member, IEEE*, Akira Saito, Kazunori Watanabe, Takayasu Sakurai, *Fellow, IEEE*, and Makoto Takamiya, *Senior Member, IEEE*

***Abstract*—The efficiency of power amplifiers (PAs) with a small output power (P_{OUT}) for short-range wireless sensor networks is limited by the loss in matching networks. To achieve high efficiency, a new design method which calculates the complicated design parameters in a class-F PA with a merged filter and matching networks is proposed. The design method provides a new quantitative conclusion that reducing both the power supply voltage (V_{DD}) and the impedance transformation ratio increases the efficiency of a PA with a small P_{OUT}. Using this result, a dual-V_{DD} scheme is realized to increase the efficiency of a transmitter (TX). At a P_{OUT} of −20 dBm, compared with the conventional single-V_{DD} scheme, the drain efficiency (DE) of the PA and the global efficiency (GE) of the TX with the dual-V_{DD} scheme are increased by factors of 2.1 and 1.5, respectively. A PA fabricated by a 40 nm CMOS process achieved a DE of 42% at a P_{OUT} of −17 dBm. The TX with the PA achieves the highest GE of 28% at a P_{OUT} of −20 dBm and the lowest energy of 36pJ/bit (= 36 μW@1Mbps with on-off keying) among the published results for TXs.**

***Index Terms*—Dual power supply voltage, high efficiency, low power, low voltage, matching networks, power amplifier.**

I. Introduction

WIRELESS sensor networks comprise a large number of small sensor nodes distributed throughout the home, in buildings, or in cities. The sensors continuously monitor and sense the activity of people, the temperature, and the humidity, and the measured data are transmitted and received by each sensor node via short-range wireless communication (e.g., 1–10 m). In such a system, the sensor nodes have the potential to operate autonomously using energy harvested from the environment via solar cells or thermoelectric generators, because the cost of maintaining and supplying power to a huge number of sensors is preventing the commercial realization of such systems. For autonomous operation, one of the challenges is the severe constraint of the power consumption of the transmitter (TX). The huge power consumption of the power amplifier (PA) is one of the critical problems in TXs. Therefore, in this paper, we report the development of an ultralow-power TX with a highly efficient PA having a small output power (P_{OUT}) for short-range wireless communication.

In the target application, each node operates as a router and configures an *ad hoc* network with symmetrical communication. The power consumption (P_{TOTAL}) of the TX and the receiver (RX) should be equalized in symmetrical communication. In this study, the target communication distance is 1 m and the data rate is 1 Mbps with modulation by on-off keying (OOK) in the 314 MHz band of the ARIB STD-T93 radio communication standard of Japan. The pass loss is assumed to be 25 dB and the typical TX/RX antenna loss is 5 dB in the 314 MHz band. A loss of 35 dB and an RX sensitivity of −55 dBm [1] specify the target P_{OUT} of the TX as −20 dBm. In addition, P_{TOTAL} for the TX should be less than 38 μW [1] owing to the symmetrical communication. This means that the global efficiency ($GE = P_{OUT}/P_{TOTAL}$) of the TX must be higher than 26% (= 10 μW/38 μW).

Fig. 1 shows the dependence of the drain efficiency (DE) on P_{OUT} for previously reported PAs [1]–[12]. In PAs [2]–[5] for conventional wireless communications (e.g., cell phones and WLANs) where the communication distance is 100 m–1 km, P_{OUT} is +10 to +30 dBm and DE is higher than 40%. In contrast, in PAs [1], [6]–[8] for short-range wireless sensor networks where the communication distance is 1–10 m, P_{OUT} is −20 to −10 dBm and DE is less than 30%. This implies that the design of a highly efficient PA with a small P_{OUT} is quite difficult. In [1], DE and GE are respectively 20% and 16% at a P_{OUT} of −20 dBm (with OOK modulation), which does not meet the design target ($GE > 26\%$). Therefore, the purpose of this study is to achieve a GE higher than 26% at a P_{OUT} of −20 dBm.

An outline of this paper is given as follows. In Section II, a design method for a class-F PA with a small P_{OUT} is shown with a new quantitative analysis of the loss in the matching networks ($P_{MATCHING}$) and the degradation of DE at a small P_{OUT}. In Section III, a dual power supply voltage (V_{DD}) scheme [13] that reduces the power consumption of a TX is described. In Section IV, the measured results for a TX with the dual-V_{DD} scheme having a P_{OUT} of −20 dBm are given. In Section V, the conclusions are given.

II. Design of PA With Small P_{OUT}

The DE of a PA with a small P_{OUT} must be maximized because its power consumption (P_{PA}) accounts for a large proportion of that of a TX. However, there has been little research

Manuscript received December 14, 2013; revised March 28, 2014; accepted April 08, 2014. Date of publication June 09, 2014; date of current version September 25, 2014. This work was carried out as part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO). This paper was recommended by Associate Editor S. Levantino.

S. Iguchi, T. Sakurai, and M. Takamiya are with the University of Tokyo, Tokyo 153-8505, Japan (e-mail: shiguchi@iis.u-tokyo.ac.jp; tsakurai@iis.u-tokyo.ac.jp; mtaka@iis.u-tokyo.ac.jp).

A. Saito was with the Semiconductor Technology Academic Research Center, Kanagawa 222-0033, Japan. He is now with Sharp Corp., Nara 632-8567, Japan (e-mail: saito.akira@sharp.co.jp).

K. Watanabe was with the Semiconductor Technology Academic Research Center, Kanagawa 222-0033, Japan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2014.2321202

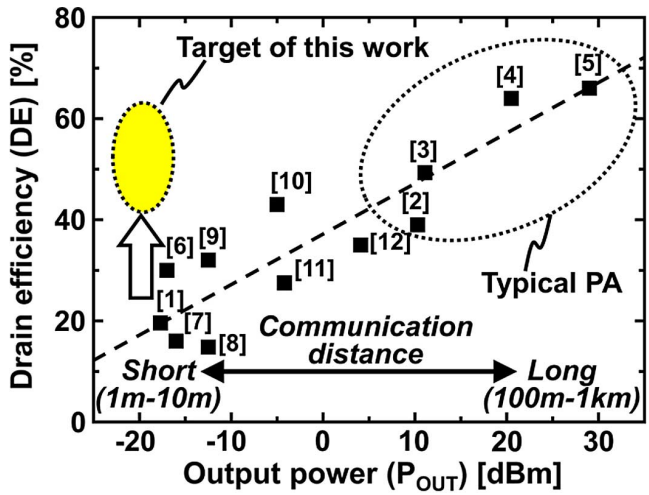


Fig. 1. Dependence of drain efficiency on $\mathrm{P_{OUT}}$ for previously reported PAs and target of this work.

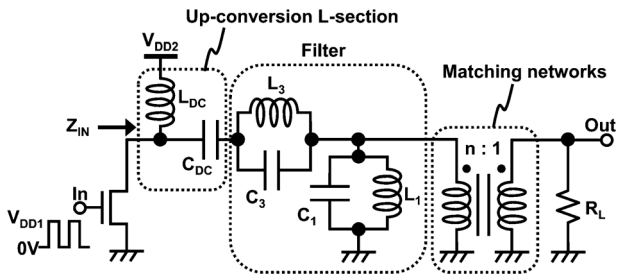


Fig. 2. Schematic of class-F PA. The up-conversion L-section, filter, and matching networks are clearly distinguished.

on the development of PAs with a $\mathrm{P_{OUT}}$ of -20 to -10 dBm, and the degradation of DE at a small $\mathrm{P_{OUT}}$ has not been quantitatively discussed. In this section, the difference between PAs with a small and large $\mathrm{P_{OUT}}$ is explained from the viewpoint of the impedance transformation. Then, a new design method for a class-F PA with a small $\mathrm{P_{OUT}}$ ($= -17$ dBm[1]) is presented. Finally, a quantitative discussion on reducing $\mathrm{P_{MATCHING}}$ and increasing DE at a small $\mathrm{P_{OUT}}$ is given.

A. Difference Between PAs With Small and Large P_{OUT}

Fig. 2 shows a schematic of a class-F PA. The up-conversion L-section, filter, and matching networks are clearly distinguished in this figure to clarify the importance of the impedance transformation at a small $\mathrm{P_{OUT}}$. These three sections are finally merged to reduce the circuit components and the loss. $\mathrm{V_{DD1}}$ is the amplitude of the input (In) and $\mathrm{V_{DD2}}$ is the power supply voltage of the PA. $\mathrm{L_{DC}}$ is a choke inductor, $\mathrm{C_{DC}}$ is an AC-coupling capacitor, $\mathrm{R_L}$ is a load resistance ($= 50\ \Omega$), $\mathrm{L_1}$ and $\mathrm{C_1}$ resonate at the fundamental frequency (f_0), and $\mathrm{L_3}$ and $\mathrm{C_3}$ resonate at the third harmonic ($3f_0$). These resonators provide high impedance at the third harmonic of the fundamental frequency. The third-harmonic peaking with maximally flat waveforms [14] achieves the theoretically maximum DE of 88%. Because of their high efficiency, class-F PAs are used in many wireless applications.

In digital PAs (e.g., class D, E, F), the highest DE is obtained at an appropriate load impedance ($\mathrm{Z_{IN}}$) where the power factor is 1 (reactive power $= 0$). Generally, such load impedance is achieved by inserting matching networks. The load impedance viewed from a transistor has to satisfy

$$\mathrm{Re}\left[Z_{IN}(\omega_0)\right] = n^2 R_L \tag{1}$$

$$\mathrm{Im}\left[Z_{IN}(\omega_0)\right] = 0, \tag{2}$$

where n is the impedance transformation ratio and ω_0 is the fundamental angular frequency ($= 2\pi f_0$). When (1) and (2) are satisfied, the $\mathrm{P_{OUT}}$ of the class-F PA in Fig. 2 is theoretically given by [15]

$$P_{OUT} = \frac{81 V_{DD2(IDEAL)}^2}{128 n^2 R_L} \propto \left(\frac{V_{DD2(IDEAL)}}{n}\right)^2, \tag{3}$$

where $V_{\mathrm{DD2(IDEAL)}}$ is the ideal $\mathrm{V_{DD2}}$ without losses except for the switching loss ($\mathrm{P_{SW}}$) of 12%.

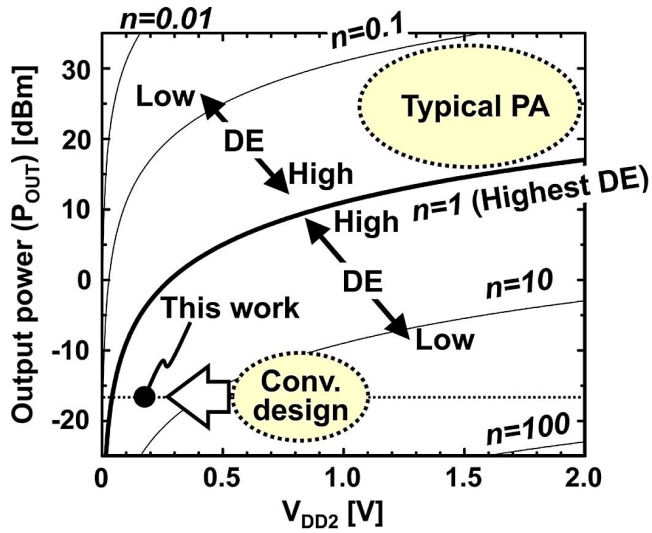


Fig. 3. Dependence of output power on $\mathrm{V_{DD2}}$ calculated using (3). The impedance transformation ratio (n) is varied from 0.01 to 100.

Fig. 3 shows the dependence of $\mathrm{P_{OUT}}$ on $\mathrm{V_{DD2}}$ calculated using (3) when n is varied from 0.01 to 100. DE reaches the maximum value at $\mathrm{n} = 1$ because the impedance transformation is not required at $\mathrm{n} = 1$. A larger distance from $\mathrm{n} = 1$ results in a larger $\mathrm{P_{MATCHING}}$ and lower DE owing to the large impedance transformation. In the typical PA design with a $\mathrm{P_{OUT}}$ of $+10$ to $+30$ dBm, a higher-$\mathrm{V_{DD2}}$ design is effective for reducing n and $\mathrm{P_{MATCHING}}$ while it may have the problem of breakdown in the power transistor. On the other hand, the PA design with a $\mathrm{P_{OUT}}$ of -17 dBm in this study is different from the typical PA design with a large $\mathrm{P_{OUT}}$. To reduce n at a small $\mathrm{P_{OUT}}$, a lower-$\mathrm{V_{DD2}}$ design is preferable. The ideal $\mathrm{V_{DD2}}$ at a $\mathrm{P_{OUT}}$ of -17 dBm is 0.04 V while conventional PAs with a small $\mathrm{P_{OUT}}$ [1], [6]–[8] have been designed with a $\mathrm{V_{DD}}$ of 0.5–1.0 V. This difference in $\mathrm{V_{DD2}}$ between the ideal value and that in the conventional designs increases $\mathrm{P_{MATCHING}}$, thereby DE is reduced. To achieve a highly efficient design for a PA with a small $\mathrm{P_{OUT}}$, in this section, the dependences of $\mathrm{P_{MATCHING}}$ and DE on n are quantitatively analyzed.

B. Design Method for Class-F PA With Small P_{OUT}

PAs (class A, B, C, E, F) intrinsically have an up-conversion L-section topology comprising $\mathrm{L_{DC}}$ and $\mathrm{C_{DC}}$ as shown in Fig. 2. The up-conversion L-section topology transforms $\mathrm{R_L}$ ($= 50\ \Omega$) to $\alpha \mathrm{R_L}$ ($\alpha > 1$). Therefore, in conventional class-F PAs [16]–[18] with a large $\mathrm{P_{OUT}}$, a down-conversion impedance transformation is required and $\mathrm{Z_{IN}}$ must be transformed from

[1]When the average $\mathrm{P_{OUT}}$ of a TX is -20 dBm with OOK modulation, the maximum $\mathrm{P_{OUT}}$ of the PA is -17 dBm.

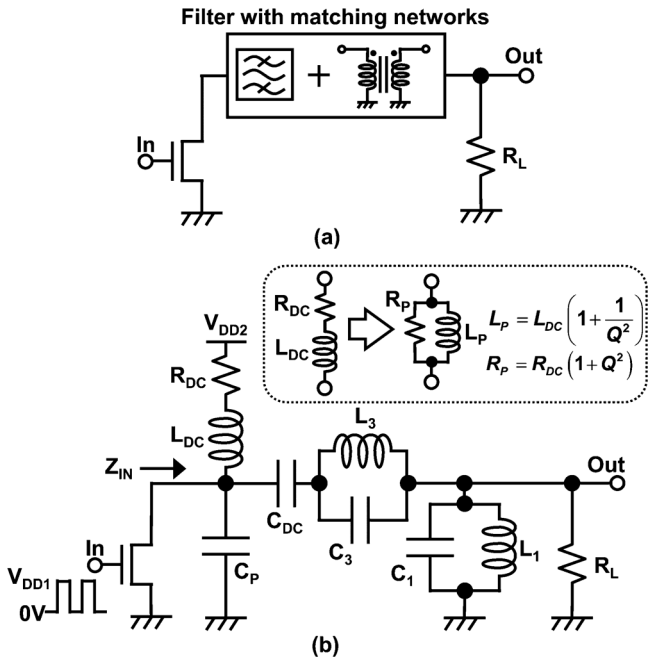


Fig. 4. Schematic of class-F PA with merged filter and matching networks. (a) Block diagram. (b) Detailed schematic.

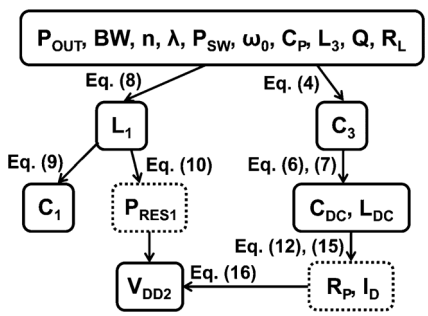


Fig. 5. Proposed design method for class-F PA with small $\mathrm{P_{OUT}}$.

$\alpha \mathrm{R_L}$ to a lower value (e.g., 10 Ω). In contrast, for PAs with a small $\mathrm{P_{OUT}}$, $\mathrm{Z_{IN}}$ should be transformed to a higher value (e.g., 250 Ω). This indicates that the appropriate impedance transformation can be provided by the intrinsic up-conversion L-section topology at a small $\mathrm{P_{OUT}}$.

In this study, a class-F PA with merged filter and matching networks is adopted to reduce the matching components and the loss. Figs. 4(a) and (b) respectively show a block diagram and a detailed schematic of a class-F PA with a small $\mathrm{P_{OUT}}$, in which the filter and matching networks are merged by using the intrinsic up-conversion L-section topology. $\mathrm{R_{DC}}$ is the equivalent series resistance of $\mathrm{L_{DC}}$, $\mathrm{R_P}$ is the equivalent parallel resistance of $\mathrm{R_{DC}}$, Q is the quality factor of the inductors, and $\mathrm{C_P}$ is the parasitic capacitance of the drain of the transistor in Fig. 4(b).

Fig. 5 shows the proposed design method for a class-F PA with a small $\mathrm{P_{OUT}}$, where BW is the bandwidth of the TX, λ is the channel-length modulation coefficient of the power transistor, $\mathrm{P_{RES1}}$ is the loss in the resonator consisting of $\mathrm{L_1}$ and $\mathrm{C_1}$, and $\mathrm{I_D}$ is the average drain current of the power transistor with a conduction angle of π. In this design method, the complicated design parameters in a class-F PA with a merged filter and matching networks are calculated using some approximations to reduce the complexity of the equations. Using this design method, $\mathrm{L_1}$, $\mathrm{C_1}$, $\mathrm{C_3}$, $\mathrm{C_{DC}}$, $\mathrm{L_{DC}}$, and $\mathrm{V_{DD2}}$ are determined from the given parameters of $\mathrm{P_{OUT}}$, BW, n, λ, $\mathrm{P_{SW}}$, ω_0, $\mathrm{C_P}$, $\mathrm{L_3}$, Q, and $\mathrm{R_L}$.

First, $\mathrm{C_3}$ is given by

$$C_3 = \frac{1}{9\omega_0^2 L_3} \tag{4}$$

because the resonator consisting of $\mathrm{C_3}$ and $\mathrm{L_3}$ should provide high impedance at the third harmonic. In this design method, the loss $(\mathrm{P_{RES3}})$ in the resonator consisting of $\mathrm{L_3}$ and $\mathrm{C_3}$ is negligible because $\mathrm{P_{RES3}}$ is negligibly small. The third harmonic $(\mathrm{V_{m3}})$ that corresponds to the voltage between the resonator consisting of $\mathrm{C_3}$ and $\mathrm{L_3}$ is 9 times smaller than the fundamental component $(\mathrm{V_m})$ of the drain voltage [14]. This verifies that $\mathrm{P_{RES3}}$ is negligibly small compared with $\mathrm{P_{RES1}}$. $\mathrm{L_3}$ should be chosen to easily implement the other parameters (e.g., $\mathrm{C_{DC}}$) because $\mathrm{L_3}$ does not affect DE.

In Fig. 4(b), $\mathrm{Z_{IN}}$ (ω_0) without $\mathrm{R_{DC}}$ is written as

$$Z_{IN}(\omega_0) = C_P \| L_{DC} \| \left\{ C_{DC} + (L_3 \| C_3) + R_L \right\}. \tag{5}$$

Then, $\mathrm{C_{DC}}$ and $\mathrm{L_{DC}}$ are calculated as follows by solving (5) for the conditions given by (1) and (2) using the approximation of $\mathrm{n^2 - 1 \approx n^2}$:

$$C_{DC} = \frac{72\omega_0 L_3 - 64\sqrt{n^2 R_L^2 - R_L^2}}{64\omega_0 R_L^2 - 64\omega_0 n^2 R_L^2 + 81\omega_0^3 L_3^2} \tag{6}$$

$$L_{DC} \approx \frac{nR_L}{\omega_0(1 + n\omega_0 R_L C_P)}. \tag{7}$$

By choosing appropriate values of these parameters, $\mathrm{Z_{IN}}$ is converted to $\mathrm{n^2 R_L}$ and a third harmonic-peaking is obtained. Then, $\mathrm{L_1}$, $\mathrm{C_1}$, and $\mathrm{P_{RES1}}$ are given by

$$L_1 = \frac{2\pi BW R_L}{\omega_0^2} \tag{8}$$

$$C_1 = \frac{1}{\omega_0^2 L_1} \tag{9}$$

$$P_{RES1} = \frac{R_L P_{OUT}}{\omega_0 Q L_1}. \tag{10}$$

In the design of the PA with a small $\mathrm{P_{OUT}}$, BW can be widened because the regulations for low-power radio communication (e.g., UWB and ARIB STD-T93) are not strict compared with those for high-speed radio communication (e.g., WLANs and cellular networks). The BW in the design should be widened by a large $\mathrm{L_1}$, thereby achieving a small $\mathrm{P_{RES1}}$.

Fig. 6(a) and (b) show respectively an equivalent circuit of the class-F PA and another equivalent circuit including the output resistance $(\mathrm{r_O})$ of the power transistor, where $\mathrm{I_d}$ is the drain current in the small-signal model. In this design method, the power transistor is modeled as a current source in the saturation

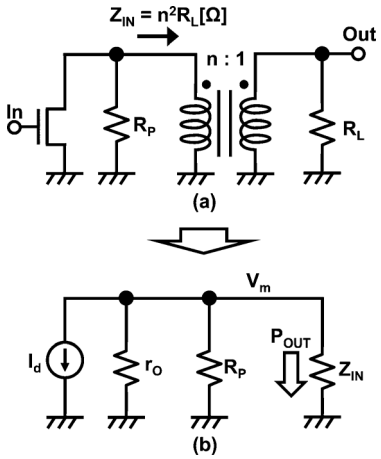


Fig. 6. Equivalent circuits of class-F PA in proposed design method. (a) Equivalent circuit using transformer model including R_P. (b) Equivalent circuit including r_O of power transistor.

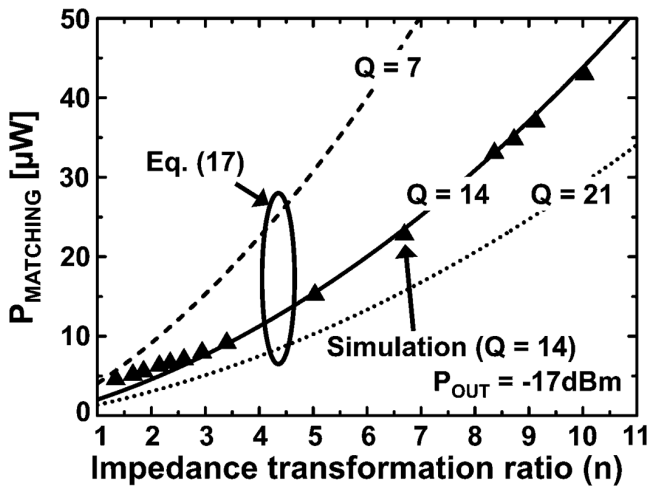


Fig. 7. Simulated dependence of $P_{MATCHING}$ on n and dependence calculated using (17) with P_{OUT} of 20 μW and C_P of 1.5 pF. Q is varied from 7 to 21.

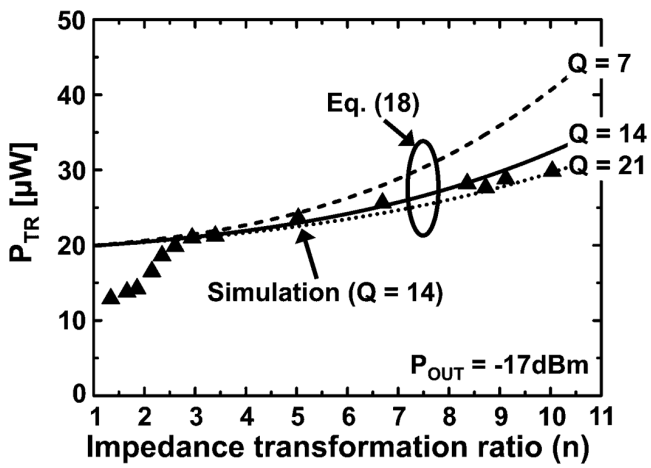


Fig. 8. Simulated dependence of P_{TR} on n and dependence calculated using (18) with P_{OUT} of 20 μW, C_P of 1.5 pF, λ of 0.5, and P_{SW} of 19.5 μW. Q is varied from 7 to 21.

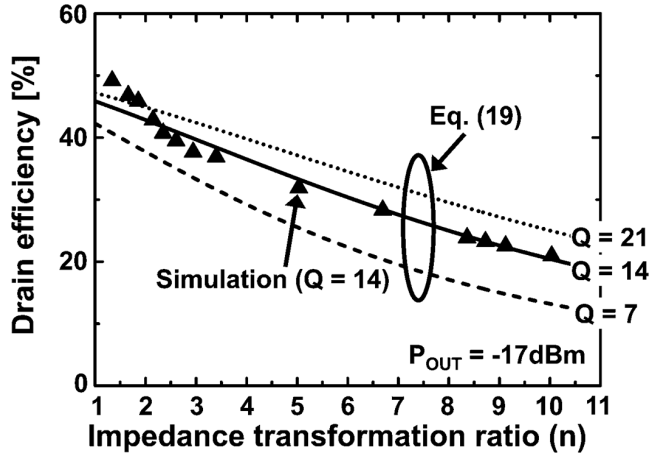


Fig. 9. Simulated dependence of DE on n and dependence calculated using (19) with P_{OUT} of 20 μW, CP of 1.5 pF, λ of 0.5, and P_{SW} of 19.5 μW. Q is varied from 7 to 21.

region.[2] r_O and R_P in Fig. 6(b) are written as follows using the approximation of $1 + Q^2 \approx Q^2$:

$$r_O = \frac{1}{\lambda I_d} \tag{11}$$

$$R_P = R_{DC}(1 + Q^2) \approx \frac{nQR_L}{1 + n\omega_0 R_L C_P}. \tag{12}$$

V_m in Fig. 6(b) is given by

$$V_m = \frac{I_d}{\left(\frac{1}{r_O} + \frac{1}{R_P} + \frac{1}{n^2 R_L}\right)} = n\sqrt{P_{OUT} R_L}. \tag{13}$$

From (13), I_d is given by

$$I_d = \frac{(n + Q + \omega_0 C_P n^2 R_L)\sqrt{P_{OUT}}}{nQ\sqrt{R_L}(1 - n\lambda\sqrt{P_{OUT} R_L})}. \tag{14}$$

Then, I_D is given by

$$I_D = \frac{2\sqrt{2}}{\pi} I_d. \tag{15}$$

In this design method, the dominant losses of P_{SW}, P_{RES1}, and $P_{MATCHING}$, and the loss of r_O in the power transistor (P_{ro}) are considered and estimated. These losses change the ideal equation for V_{DD2} given by (3). The modified V_{DD2} is given by

$$V_{DD2(REAL)} = V_{DD2(IDEAL)} + \frac{P_{SW} + P_{RES1}}{I_D}, \tag{16}$$

where $V_{DD2(REAL)}$ is V_{DD2} upon taking P_{SW}, P_{RES1}, $P_{MATCHING}$, and P_{ro} into consideration. In (16), the effects of $P_{MATCHING}$ and P_{ro} are included in I_D.

C. Quantitative Analysis for Reducing $P_{MATCHING}$ and Increasing DE at small P_{OUT}

In PAs with a small P_{OUT}, $P_{MATCHING}$ and the loss in the power transistor (P_{TR}) are the dominant losses. Therefore, the quantitative estimation and analysis of $P_{MATCHING}$ and P_{TR} are required to design highly efficient PAs with a small P_{OUT}.

[2]This assumption may include a small error because the power transistor operates in a large-signal mode; however, a rough estimation can be obtained from this assumption [19]. Therefore, the power transistor is modeled as a current source to make the design method concise. The error resulting from this assumption is discussed in Section II-C.

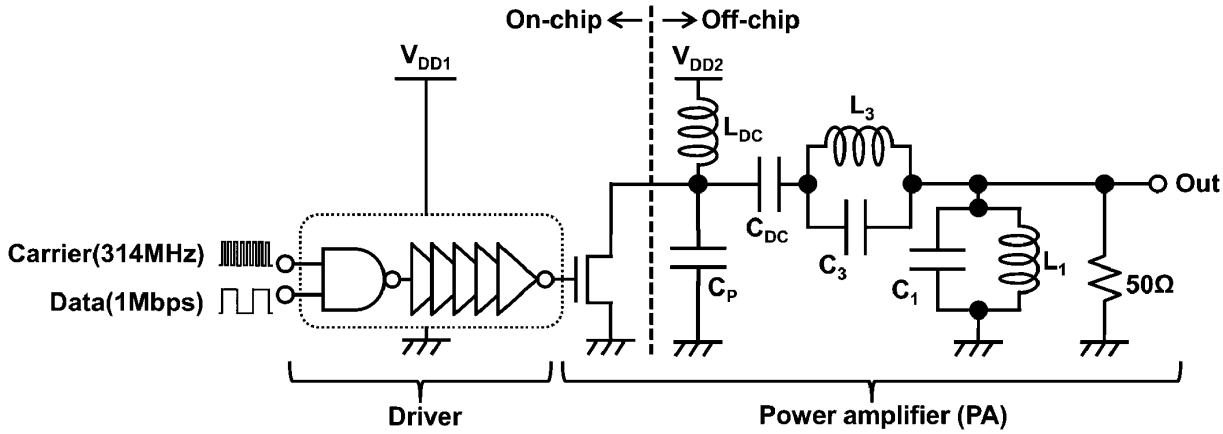


Fig. 10. Schematic of TX with class-F PA.

In this section, $P_{MATCHING}$, P_{TR}, and DE are quantitatively estimated.

In Fig. 6(b), $P_{MATCHING}$ is modeled as the loss in R_P. The impedance transformation is carried out using the intrinsic up-conversion L-section topology of L_{DC} and C_{DC}. Therefore, the value of $P_{MATCHING}$ corresponding to the impedance transformation is given by the loss in R_P. P_{TR} is the sum of P_{ro} and P_{SW}. $P_{MATCHING}$ and P_{TR} in the power transistor are calculated as follows using (14) with consideration of the loss due to V_{m3} $(= V_m/9)$:

$$P_{MATCHING} = \frac{100nP_{OUT}(1 + n\omega_0 C_P R_L)}{81Q} \tag{17}$$

$$P_{TR} = \frac{100n\lambda(n + Q + n^2\omega_0 C_P R_L)\sqrt{P_{OUT}^3 R_L}}{81Q(1 - n\lambda\sqrt{P_{OUT}R_L})} + P_{SW}. \tag{18}$$

Fig. 7 shows the simulated dependence of $P_{MATCHING}$ on n and the dependence calculated using (17). Q is varied from 7 to 21, because Q for an on-chip inductor is less than 10 [19] and Q for an off-chip inductor is less than 20 [20] in the 314 MHz band. From (17), $P_{MATCHING}$ is mainly determined by n, while it is independent of P_{TR}. The dependence of $P_{MATCHING}$ shown in Fig. 7 shows that a larger n results in a larger $P_{MATCHING}$. When n and Q are 9.7 and 14, respectively, at a V_{DD2} of 0.5 V [1], the calculated $P_{MATCHING}$ is 42 μW, which is 2.1 times larger than P_{OUT}. Therefore, it is difficult to achieve a high DE at a V_{DD2} of 0.5 V. To reduce $P_{MATCHING}$, a low V_{DD2} $(=$ small n$)$, a miniaturized process $(=$ small $C_P)$, and an inductor with a high Q should be used.

Fig. 8 shows the simulated dependence of P_{TR} on n and the dependence calculated using (18). The dependence of P_{TR} shown in Fig. 8 shows that a larger n results in a larger P_{TR} while the dependence is less than that of $P_{MATCHING}$. The inconsistency of P_{TR} for $n < 3$ is next discussed. At small values of n, V_{DD2} is increased, and the power transistor operates in the linear region. The modeling of the power transistor as a current source is not valid in this region, resulting in the inconsistency when $n < 3$. As shown in Fig. 8, upon reducing P_{TR}, n should be reduced. This gives the same conclusion as that for $P_{MATCHING}$, a design with a smaller n is preferable at a small P_{OUT}.

From (10), (17), and (18), DE is given by

$$DE = \frac{P_{OUT}}{P_{OUT} + P_{RES1} + P_{MATCHING} + P_{TR}}. \tag{19}$$

Fig. 9 shows the simulated and calculated dependences of DE on n. The agreement of the results obtained using (19) and by simulation verifies the consistency of the proposed design method and the discussion. For the target GE of 26%, DE should be higher than 26% because the driver power (P_{DRIVER}) is included in P_{TOTAL}. For DEs of more than 30, 35, and 40%, n should be smaller than 6.1, 4.5, and 2.9, respectively. To increase DE at a small P_{OUT}, a design with a smaller n $(=$ smaller $V_{DD2})$ is essential. Hence, both n and V_{DD2} must be reduced ($n = 3.4$ and $V_{DD2} = 0.2$ V in this work) to smaller values than those in conventional designs ($V_{DD2} = 0.5$–1.0 V) [1], [6], [7], [9].

III. Design of Low-Power Transmitter With Dual-V_{DD} Scheme

In this section, a dual-V_{DD} scheme [13] is realized to maximize GE for a TX with a P_{OUT} of -20 dBm with OOK modulation. In the previous section, the importance of a small n and a low V_{DD2} for the design of a highly efficient class-F PA was explained. However, in the TX design with a small P_{OUT}, the driver power (P_{DRIVER}) is not negligible. In previous studies, P_{DRIVER} was 100 μW at a P_{OUT} of 20–560 μW [9], and P_{DRIVER} was 8.5 μW at a P_{OUT} of 8 μW [1]. Thus, P_{DRIVER} is comparable to P_{OUT}. Therefore, an optimization method for minimizing P_{TOTAL} by considering P_{DRIVER} is realized for the class-F PA designed by the proposed design method. In the optimized design, the minimum P_{TOTAL}, corresponding to the maximum GE, is determined by calculating P_{TOTAL} for every n.

Fig. 10 shows a schematic of the TX with the class-F PA. The carrier frequency is 314 MHz for the ARIB STD-T93 radio communication standard of Japan and the data rate is 1 Mbps with OOK modulation. As shown in Fig. 10, P_{TOTAL} is the sum of P_{DRIVER} (the power of the mixer can be neglected) and P_{PA}.

In an ideal class-F PA [14], V_{DD1} does not depend on P_{OUT} and n. However, in this optimization, V_{DD1} must be changed with n. The reason for this is discussed below. I_D is given by (15). Fig. 11 shows the simulated and calculated dependences of I_D on n. As shown in Fig. 11, I_D decreases as n increases. I_D is determined by the drive capability of the power transistor in the PA. To control the drive capability, the design can be optimized by a conventional single-V_{DD} scheme with variable W at fixed V_{DD1} $(= V_{DD2})$ or a dual-V_{DD} scheme with a variable V_{DD1} at a fixed W. In the previous section, it was verified that a smaller n achieves a higher DE; therefore, a design with a smaller n is fundamentally required to maximize GE. However, the smaller n results in a lower V_{DD2}, thereby V_{DD2} is less than 0.5 V at

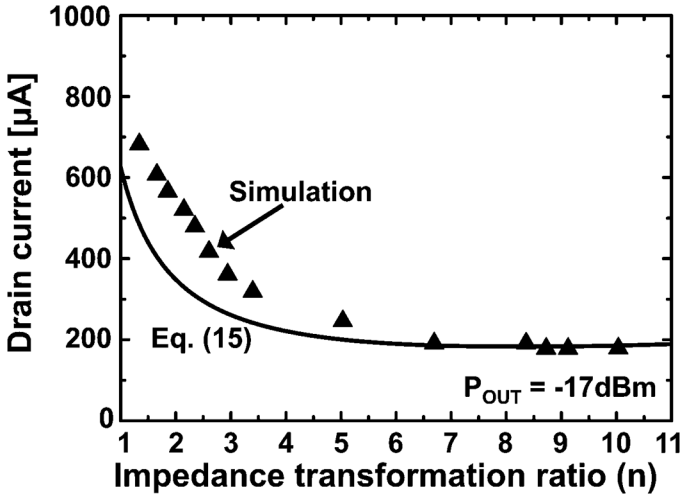


Fig. 11. Simulated dependence of ID on n and dependence calculated using (15). The inconsistency of I_D for $n < 3$ is caused by modeling as the current source in the linear region.

$n < 9.7$. This implies that the single-V_{DD} scheme is not suitable for design optimization at a smaller n because the transistors in the driver do not operate at $V_{DD1} < 0.5$ V owing to the huge delay in the sub-/near-threshold operation. On the other hand, in the dual-V_{DD} scheme, the transistors can operate at $n < 9.7$ because the smaller n results in a larger V_{DD1} ($\geq$0.5 V). From this discussion, V_{DD1} is changed with n to control the drive capability of the transistor to maximize GE.

Figs. 12(a), (b), and (c) show the simulated and calculated n dependences in a TX with a P_{OUT} of -20 dBm. V_{DD1}, P_{DRIVER}, P_{PA}, and P_{TOTAL} are calculated by [21]

$$V_{DD1(SAT)} = V_{TH} + \frac{\sqrt{2\beta\lambda I_D V_{DD2} + I_D^2\theta^2 + 2\beta I_D} + I_D\theta}{\beta(\lambda V_{DD2} + 1)} \tag{20}$$

$$V_{DD1(LIN)} = V_{TH} + \frac{\beta V_{DD2}^2 + 2I_D}{2(\beta V_{DD2} - I_D\theta)} \tag{21}$$

$$P_{DRIVER} = fC_{DRIVER}V_{DD1(SAT)\ or\ (LIN)}{}^2 \tag{22}$$

$$P_{PA} = P_{OUT} + P_{RES1} + P_{MATCHING} + P_{TR} \tag{23}$$

$$P_{TOTAL} = P_{PA} + P_{DRIVER}, \tag{24}$$

where $V_{DD1(SAT)}$ is V_{DD1} in the saturation region of the power transistor, $V_{DD1(LIN)}$ is V_{DD1} in the linear region of the power transistor, $\beta = \mu_n C_{OX} W/L$, θ is a fitting parameter used to describe the degradation of mobility, V_{TH} is the threshold voltage of the power transistor, C_{DRIVER} is the equivalent capacitance of the driver, μ_n is the mobility of electrons, W is the width of the power transistor, and L is the length of the power transistor. Equations (20) and (21) are selectively used depending on the operation mode of the transistor.

Fig. 12(a) shows the simulated and calculated dependences of P_{TOTAL}, P_{DRIVER}, and P_{PA} on n, Fig. 12(b) shows the simulated and calculated dependences of V_{DD1} and V_{DD2} on n, and Fig. 12(c) shows the simulated and calculated dependences of C_{DC} and L_{DC} on n. In Fig. 12(b), when n is reduced, I_D is increased as shown in Fig. 11, then, V_{DD1} is increased because the higher I_D requires a higher drive voltage (V_{DD1}) in the power transistor. In a similar manner, as shown in Fig. 12(a), P_{DRIVER} is increased when n is reduced because P_{DRIVER} is proportional to V_{DD1}^2.

As shown in Fig. 12(b), a conventional TX [1] with a single-V_{DD} is designed with $n = 8.7$ and $V_{DD1} = V_{DD2} =$ 0.47 V. In contrast, as shown in Fig. 12(a), P_{TOTAL} is minimized at $n = 3.4$, thereby GE is maximized at $n = 3.4$. The corresponding values of V_{DD1} and V_{DD2} are 0.56 V and 0.2 V, respectively, as shown in Fig. 12(b). Table I shows the parameters in the conventional single-V_{DD} design and the dual-V_{DD} design.

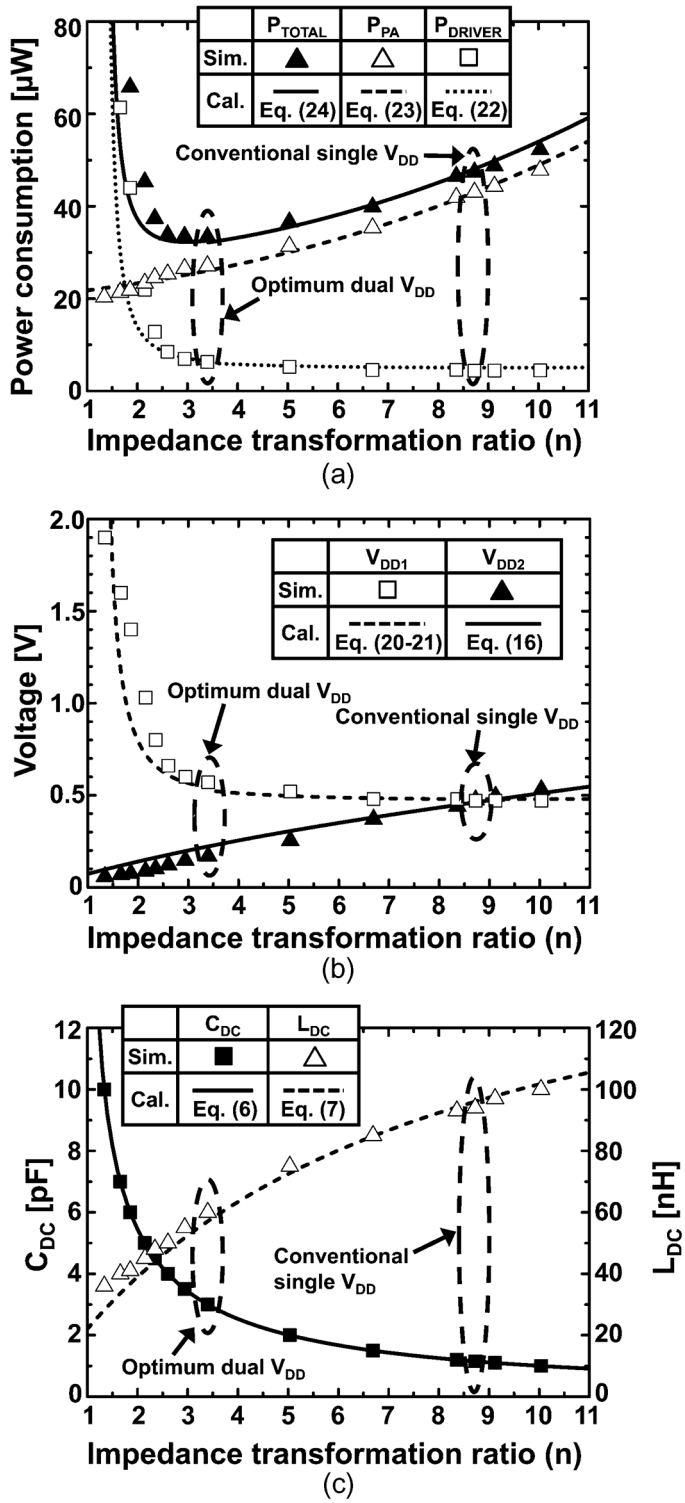


Fig. 12. SPICE-simulated and calculated impedance transformation ratio (n) dependences in TX at P_{OUT} of -20 dBm. (a) Power consumption vs. n. (b) V_{DD1} and V_{DD2} vs. n. (c) C_{DC} and L_{DC} vs. n.

Fig. 12 shows the good agreement between the results obtained by simulation and calculation. This shows the validity

TABLE I
PARAMETERS IN CONVENTIONAL SINGLE-V_{DD} DESIGN AND DUAL-V_{DD} DESIGN

	Conventional single-V_{DD}	Dual-V_{DD} scheme
V_{DD1}	0.47V	0.56V
V_{DD2}	0.47V	0.2V
C_{DC}	1pF	3pF
L_{DC}	100nH	60nH

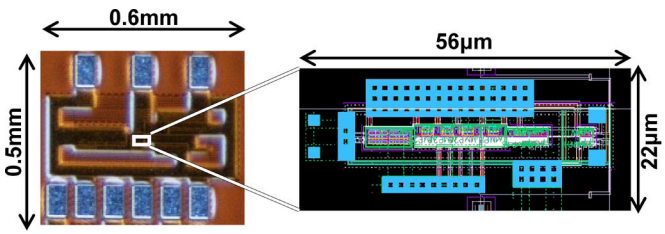


Fig. 13. Die micrograph and layout of TX with dual-V_{DD} scheme fabricated by 40 nm CMOS process.

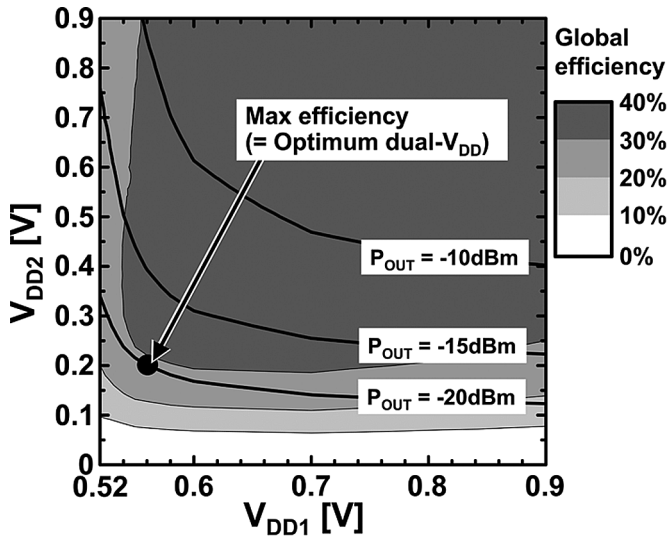


Fig. 14. Measured contours of GE and P_{OUT} when V_{DD1} and V_{DD2} are varied. Gray levels represent the values of GE. The lines are the contours of P_{OUT}. At the target P_{OUT} of -20 dBm, the maximum GE is 28% at $V_{DD1} = 0.56$ V and $V_{DD2} = 0.2$ V

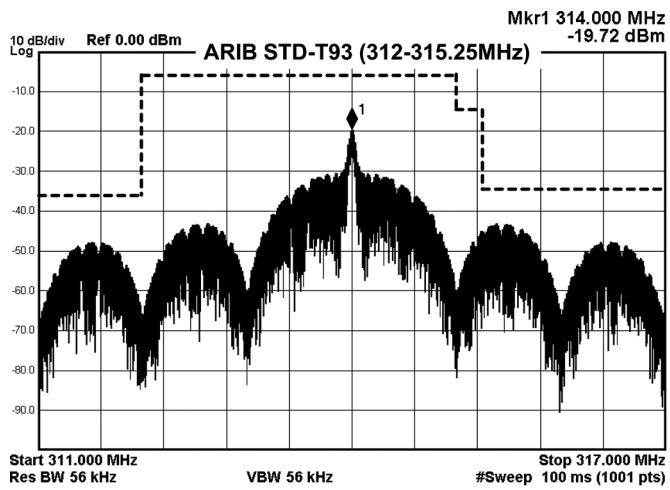


Fig. 15. Measured output spectrum of the TX. The 314 MHz carrier is modulated by 1 Mbps OOK.

of the new design method for a class-F PA with merged filter and matching networks, and that the quantitative analysis of the losses with a small P_{OUT} is consistent.

The difference between the optimization of DE and GE is discussed. In the optimization of DE, when n is reduced from 10 to 1, V_{DD2} is reduced [Fig. 12(b)] and P_{PA} is reduced [Fig. 12(a)] because $P_{MATCHING}$ decreases in proportional to n (Fig. 7); therefore, DE is maximized at $n = 1$. Alternatively, in the optimization of GE as n decreases, V_{DD1} is increased [Fig. 12(b)] and P_{DRIVER} is increased [Fig. 12(a)]. When n is reduced, V_{DD1} rapidly increases [Fig. 12(b)] because the transistor operation changes from the saturation region to the linear region, thereby the corresponding P_{DRIVER} rapidly increases [Fig. 12(a)]. Therefore, P_{TOTAL} is minimized at $n = 3.4$ [Fig. 12(a)] and GE is maximized at $n = 3.4$. By considering this trade-off between P_{PA} and P_{DRIVER}, the optimum n can be decided in the dual-V_{DD} scheme.

IV. MEASUREMENT RESULTS AND DISCUSSION

To demonstrate the advantageousness of the dual-V_{DD} scheme [13], a test chip is fabricated by a 1.1 V, 40 nm CMOS process. Fig. 13 shows a die micrograph and the layout. The die size is 0.5 mm $\times$ 0.6 mm and the core area of the TX is $56\ \mu m \times 22\ \mu m$. The measured parameters of the conventional single-V_{DD} scheme and the dual-V_{DD} scheme are given in Table I, and the same two resonators with the following parameters are used: $L_1 = 22$ nH, $C_1 = 11$ pF, $L_3 = 2.7$ nH, and $C_3 = 12$ pF.

Fig. 14 shows the measured GE and P_{OUT} for the TX in the dual-V_{DD} scheme when V_{DD1} and V_{DD2} are varied. At the target P_{OUT} of -20 dBm, the maximum GE is 28% at $V_{DD1} = 0.56$ V and $V_{DD2} = 0.2$ V, which corresponds to the simulated results in Figs. 12(a) and (b). These results show that the dual-V_{DD} scheme and the design optimization $(n = 3.4)$ achieve the highest GE at a P_{OUT} of -20 dBm.

Fig. 15 shows the measured output spectrum of the TX. The 314 MHz carrier is modulated with 1 Mbps OOK modulation. The measured P_{OUT} of -20 dBm satisfies the ARIB STD-T93 radio communication standard of Japan. The spectrum mask is satisfied as a result of the low P_{OUT} even with the larger harmonics owing to the operation of the power transistor in the linear region. In addition, the robustness against spectrum distortion can loosen the ripple requirement of DC-DC converters to generate V_{DD2} in the dual-V_{DD} method.

Figs. 16 and 17 show the measured dependences of DE and GE on P_{OUT}, respectively. The conventional single-V_{DD} scheme and the dual-V_{DD} scheme are compared. In the single-V_{DD} scheme, V_{DD1} is equal to V_{DD2} and V_{DD1} is varied. In the dual-V_{DD} scheme, V_{DD1} and V_{DD2} are varied according to the optimum V_{DD1} and V_{DD2} shown in Fig. 14. At the target P_{OUT} of -17 dBm for DE and -20 dBm for GE, DE and GE for the TX with the dual-V_{DD} scheme are 2.1 and 1.5 times higher than those with the conventional single-V_{DD} scheme, respectively.

The power overhead required to generate V_{DD2} from V_{DD1} is next discussed. The design issue of the dual-V_{DD} scheme is that a DC-DC converter is required to generate V_{DD2} from V_{DD1}. DC-DC converters with an input voltage of 0.56 V, output voltage of 0.2 V, output current of 50 μA, and efficiency of more than 66% are required in this study. Some low-voltage and low-output-power DC-DC converters that have the potential to satisfy these requirements of the dual-V_{DD} scheme have

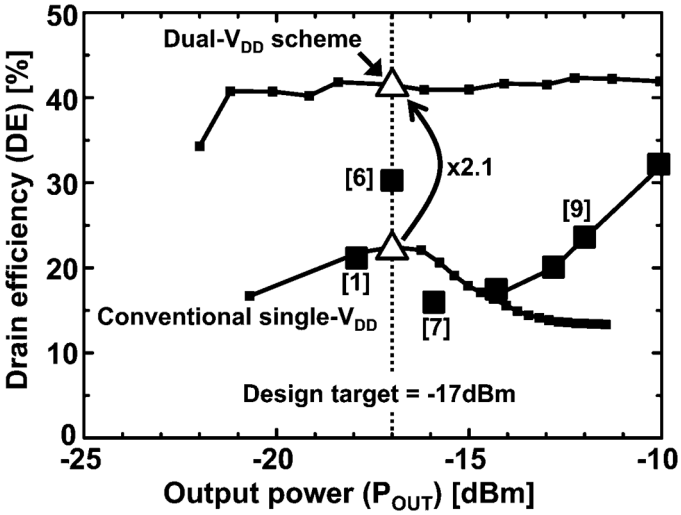


Fig. 16. Measured dependence of DE on output power. The conventional single-V_{DD} scheme and dual-V_{DD} scheme are compared. Results of previous studies are also shown.

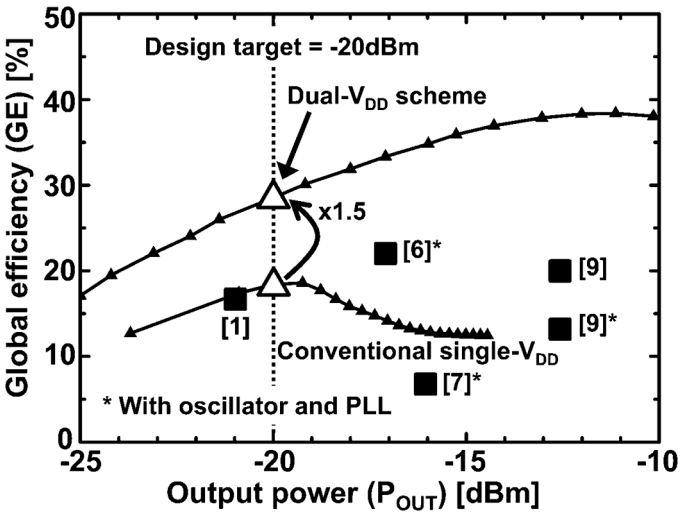


Fig. 17. Measured dependence of GE on output power. The conventional single-V_{DD} scheme and dual-V_{DD} scheme are compared. Results of previous studies are also shown.

been reported. A 0.45 V-input and 0.34 to 0.44 V-output buck converter [22] with an output current of 0.67–410 μA was used in an on-chip gate boost technique to achieve an efficiency of more than 90% at a low input voltage and a low output current. A-low-output voltage (0.3–0.55 V) buck converter [23] with an input voltage of 0.6–1.1 V and a discontinuous conduction mode (DCM) controller was reported to achieve an efficiency of 90% at an output voltage of 0.35 V. Neither DC-DC converter, however, satisfies all the requirement of the dual-V_{DD} scheme. Therefore, the development of 0.2 V-output DC-DC converters with an efficiency of more than 66% is a future research challenge to achieve a higher GE using the dual-V_{DD} scheme.

In Figs. 16 and 17 and Table II, the results of this work [13] are compared with those of previously reported TXs with small P_{OUT} values of -20 to -10 dBm. [1], [6], [7], [9]. The previous results are shown in descending order of P_{OUT} in Table II. The TX with the dual-V_{DD} scheme achieves the highest DE of 42% and the highest GE of 28%, thereby achieving the lowest energy of 36 pJ/bit ($=$ 36 μW@1 Mbps) among the reported TXs.

TABLE II
COMPARISON WITH RESULTS OF PREVIOUS STUDIES

	Unit	[9]	[7]	[6]	[1]	This work [13]
CMOS technology	nm	65	130	130	40	40
Supply voltage	V	0.7	1	1	0.5	V_{DD1}:0.56 V_{DD2}:0.2
Frequency	MHz	2400	300-450	400	315	315
Data rate	Mbps	1	0.1	0.2	1	1
PA class	-	Class-D	Edge-combiner	Edge-combiner	Class-F	Class-F
Output power (P_{OUT})	dBm	-12.5	-16	-17	-21	-20
Drain efficiency	%	32	16	30	20	42
Power consumption of TX (P_{TOTAL})	μW	440	400	90	52	36
GE w/o Osc. & PLL	%	20	-	-	16	28
GE w/ Osc. & PLL	%	13	6.3	22	-	-
Energy	pJ/bit	440	4000	450	52	36
TX includes	-	Osc.+Driver +PA	Osc.+PLL+ Mixer+PA	Osc.+PLL+ Mixer+PA	Mixer+ Driver+PA	Mixer+ Driver+PA

V. CONCLUSION

A low-power and highly efficient transmitter (TX) was developed. To achieve a highly efficient power amplifier (PA) with a small output power (P_{OUT}), a new design method which calculates the complicated design parameters for a class-F PA with a small P_{OUT} is proposed. The proposed design method provides a quantitative analysis of the low efficiency in a class-F PA with a small P_{OUT}, in particular, the dependences of the loss in the matching networks $(P_{MATCHING})$ and the drain efficiency (DE) on the impedance transformation ratio are discussed. On the basis of the quantitative analysis, we conclude that a low power supply voltage (V_{DD}) and a small impedance transformation ratio result in higher efficiency of the PA with a small P_{OUT}. Using this result, a dual-V_{DD} scheme is realized to increase the efficiency of a TX with a PA having a small P_{OUT}. At a P_{OUT} of -20 dBm, compared with the conventional single-V_{DD} scheme, DE and GE for the TX with the dual-V_{DD} scheme are 2.1 and 1.5 times higher, respectively. Compared with previously reported TXs, the TX with the dual-V_{DD} scheme achieves the highest DE of 42% and the highest GE of 28% at a P_{OUT} of -20 dBm, thereby achieving the lowest energy of 36 pJ/bit ($=$ 36 μW@1 Mbps) among the reported TXs.

REFERENCES

[1] A. Saito, K. Honda, Y. Zheng, S. Iguchi, K. Watanabe, T. Sakurai, and M. Takamiya, "An all 0.5 V, 1 Mbps, 315 MHz OOK transceiver with 38- μW carrier-frequency-free intermittent sampling receiver and 52- μW Class-F transmitter in 40-nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 38–39.

[2] J. Fritzin, Y. Jung, P. N. Landin, P. Handel, M. Enqvist, and A. Alvandpour, "Phase predistortion of a class-D outphasing RF amplifier in 90 nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 10, pp. 642–646, Oct. 2011.

[3] H.-S. Oh, T. Song, E. Yoon, and C.-K. Kim, "A power-efficient injection-locked class-E power amplifier for wireless sensor network," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 4, pp. 173–175, Apr. 2006.

[4] J. Fritzin, T. Sundstrom, T. Johansson, and A. Alvandpour, "Reliability study of a low-voltage class-E power amplifier in 130 nm CMOS," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 2010, pp. 1907–1910.

[5] J. Lindstrand, C. Bryant, M. Tormanen, and H. Sjoland, "A 1.6–2.6 GHz 29 dBm injection-locked power amplifier with 64% peak PAE in 65 nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2011, pp. 299–302.

[6] J. Pandey and B. Otis, "A sub-100 μW MICS/ISM band transmitter based on injection-locking and frequency multiplication," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1049–1058, May 2011.

[7] S. Rai, J. Holleman, J. Pandey, F. Zhang, and B. Otis, "A 500 μW neural tag with 2 μVrms AFE and frequency-multiplying MICS/ISM FSK transmitter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 212–213.

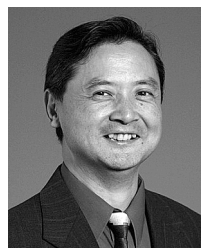
[8] G. Papotto, F. Carrara, A. Finocchiaro, and G. Palmisano, "A 90 nm CMOS 5 Mb/s crystal-less RF transceiver for RF-powered WSN nodes," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 452–454.
[9] A. Paidimarri, P. M. Nadeau, P. P. Mercier, and A. P. Chandrakasan, "A 2.4 GHz multi-channel FBAR-based transmitter with an integrated pulse-shaping power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1042–1054, Apr. 2013.
[10] K. Natarajan, J. S. Walling, and D. J. Allstot, "A class-C power amplifier/antenna interface for wireless sensor applications," in *Proc. IEEE Radio Freq. Integr. Circuits Conf. Dig. Tech. Papers*, Jun. 2011, pp. 1–4.
[11] B. Otis, Y. H. Chee, and J. Rabaey, "A 400 μW-RX, 1.6 mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 396–397.
[12] Y. H. Chee, J. Rabaey, and A. M. Niknejad, "A class A/B low power amplifier for wireless sensor networks," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, pp. 409–412.
[13] S. Iguchi, A. Saito, K. Watanabe, T. Sakurai, and M. Takamiya, "2.1 times increase of drain efficiency by dual supply voltage scheme in 315 MHz class-F power amplifier at output power of -20 dBm," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2012, pp. 345–348.
[14] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 11, pp. 2007–2012, Nov. 1997.
[15] P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*, 1st ed. Dordrecht, The Netherlands: Springer, 2006.
[16] K. Kuroda, R. Ishikawa, and K. Honjo, "Parasitic compensation design technique for a C-band GaN HEMT class-F amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 11, pp. 2741–2750, Nov. 2010.
[17] C. Trask, "Class-F amplifier loading networks: a unified design approach," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1999, pp. 351–354.
[18] A. V. Grebennikov, "Circuit design technique for high efficiency class F amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2000, pp. 771–774.
[19] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Pearson, 2012.
[20] Inductors for High-Frequency Circuits, MLG Series Datasheet TDK [Online]. Available: http://www.tdk.co.jp/tefe02/e521_mlg.pdf
[21] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York: McGraw-Hill, 2001.
[22] X. Zhang, P. Chen, Y. Ryu, K. Ishida, Y. Okuma, K. Watanabe, T. Sakurai, and M. Takamiya, "A 0.45-V input on-chip gate boosted (OGB) buck converter in 40-nm CMOS with more than 90% efficiency in load range from 2 μW to 50 μW," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 194–195.
[23] X. Zhang, Y. Okuma, P. Chen, K. Ishida, Y. Ryu, K. Watanabe, T. Sakurai, and M. Takamiya, "A 0.6-V input 94% peak efficiency CCM/DCM digital buck converter in 40-nm CMOS with dual-mode-body-biased zero-crossing detector," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2013, pp. 45–48.

Shunta Iguchi (S'12) received the B.S. degree in electronic engineering from the University of Electro-Communications, Tokyo, Japan, in 2011 and the M.S. degree in electrical engineering and information systems from the University of Tokyo in 2013, where he is currently pursuing the Ph.D. degree. His research interests include the circuit design of the low-power RF transceiver circuits, the crystal oscillators, and the wireless power transmission circuits.

From August 2011 to September 2011, he worked at Analog Devices, Tokyo, on voltage reference circuits. From August 2013 to September 2013, he worked in the wireless and analog division in Toshiba, Kawasaki, Japan, designing low power wireless transceiver circuits. He is a recipient of the best paper award in 2013 IEEE Wireless Power Transfer Conference.

Akira Saito received the B.S. degree in electronics and communication from Waseda University, Tokyo, Japan, in 1990, and received M.S. degree in electronic engineering and Ph.D. degrees in physics from the University of Tokyo in 1992 and 2000. He joined the Sharp Corporation in 1996. He was a Visiting Researcher at Extremely Low Power LSI Laboratory, Institute of Industrial Science, University of Tokyo, from 2009 to 2013. He has engaged in the researches of the silicon and germanium nano-crystals, liquid crystal display fabrication process, and the digital and analog circuits designs for the digital communication and broadcasting systems such as Bluetooth, 802.11, W-CDMA, and ISDB-T.

Kazunori Watanabe graduated from the Tomakomai Technical College, Japan, in 1975. In 1975, he joined Matsushita Communication Industrial Co., Ltd. (presently Panasonic Mobile Communications Co., Ltd.), Yokohama, Japan. He was engaged in development of a digital system for pager. From 1997 through 2003, he has managed development of the technology for cdmaOne cellular phone. From 2003, he was engaged in system design development of using high frequency semiconductor integrated circuit in Panasonic Corporation Semiconductor Company, Kyoto, Japan. He has been a Visiting Researcher at Extremely Low Power LSI Laboratory, Institute of Industrial Science, University of Tokyo since 2009. He is interested in analog circuits, power supply circuits, and wireless communication systems for extremely low power LSI circuits and systems.



Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in EE from the University of Tokyo, Japan, in 1981. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a Visiting Researcher at the University of California Berkeley, USA, where he conducted research in the field of VLSI CAD. Since 1996, he has been a professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic ICs, and large-area electronics. He has published more than 600 technical publications including 100 invited presentations and several books and filed more than 200 patents.

He is the executive committee chair for VLSI Symposia and a steering committee chair for the IEEE A-SSCC. He served as a conference chair for the Symp. on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the A-SSCC, and VLSI symp., an executive committee member for ISLPED and a program committee member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He is a recipient of 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, 2009 and 2010 IEEE Paul Rappaport award, 2010 IEICE Electronics Society award, 2009 IEICE achievement award, 2005 IEEE ICICDT award, 2004 IEEE Takuo Sugano award and 2005 P&I patent of the year award and four product awards. He delivered keynote speech at more than 50 conferences including ISSCC, ESSCIRC and ISLPED. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS distinguished lecturer. He is an IEICE Fellow.

Makoto Takamiya (S'98–M'00–SM'14) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1995, 1997, and 2000, respectively. In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSI's. In 2005, he joined the University of Tokyo, where he is an Associate Professor of VLSI Design and Education Center. From 2013 to 2014, he was with the University of California, Berkeley, USA, as a Visiting Scholar. His research interests include the circuit design of the low-power RF circuits, the ultra low-voltage logic circuits, the low-voltage power management circuits, and the large area and flexible electronics with organic transistors.

He is a member of the technical program committee of IEEE International Solid-State Circuits Conference and IEEE Symposium on VLSI Circuits. He received 2009 and 2010 IEEE Paul Rappaport Awards and the best paper award in 2013 IEEE Wireless Power Transfer Conference.