A 0.6 V Input CCM/DCM Operating Digital Buck Converter in 40 nm CMOS

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***Abstract*—This paper presents a 0.6 V input, 0.3–0.55 V output buck converter in 40 nm CMOS, for low-voltage low-power wireless sensor network systems. A low power CCM/DCM controller of the buck converter enables automatic selection of DCM or CCM operation depending on load situation, therefore improving the power efficiency. A dual-mode-body-biased (DMBB) zero-crossing detector with both forward body bias mode and zero body bias mode is designed to enable DCM operation with both low supply voltage and normal supply voltage. An ultra-low-power hysteresis voltage detector is proposed for body bias modes selection. The proposed buck converter achieves a peak efficiency of 94% with an output current range of 50 µA to 10 mA. Thanks to the DCM operation, the efficiency at an output current of 10 µA is improved by 20% and 9%, with an output voltage of 0.35 V and 0.5 V, respectively.**

***Index Terms*—Buck converter, DC-DC converter, forward body bias, low voltage, voltage detector.**

I. Introduction

THANKS to the mature fabrication technology, photovoltaic (PV) module becomes one of the most popular power suppliers for wireless sensor nodes and wearable electronic devices [1]–[4]. Combining the PV module with the battery-powered system can effectively extend the battery lifetime. Moreover, PV energy harvesting provides an attractive solution for battery-less system. In these low-power applications, scaling the power supply of digital circuits down to sub/near-threshold region is a promising technique to achieve significant power reduction. In recent advanced CMOS technology, the threshold voltage ($\mathrm{V_{TH}}$) is down to 400 mV. Therefore, there is a strong demand for designing a high efficiency power converter to provide a regulated 0.3 V–0.55 V output voltage ($\mathrm{V_{OUT}}$) with low output current ($<$10 mA). Considering the maximum power point characteristics of a typical single-cell PV module, the targeted $\mathrm{V_{IN}}$ of the power converter should cover as low as 0.6 V.

Until now, various types of step-down voltage converters have been developed for low-voltage operation. A digital low-dropout regulator (LDO) is firstly reported in [5] and utilized for near/sub-threshold logic circuits [6]. By using digital control circuits, the operating voltage can be reduced to 0.5 V with low quiescent current. The conversion efficiency of the LDO, however, is limited by the ratio of $\mathrm{V_{OUT}}$ and $\mathrm{V_{IN}}$, which is not applicable for adaptive power supply voltage control in digital circuits. A low-voltage buck converter with high conversion efficiency is realized in [7]. It uses a delay chain based digital pulse-width modulation (DPWM) technique to reduce the operating voltage but the input voltage is fixed. In addition, a large inductor of 47 mH is required to accommodate low inductor current ripple for continuous conduction mode (CCM) operation.

Even though small inductor is preferred for low-cost small-area application, an inductor current ripple becomes a problem. When the converter is operating under light load condition, the inductor current becomes negative for a certain period which causes a significant loss. To reduce the inductor size while maintaining high conversion efficiency, the discontinuous conduction mode (DCM) operation can be used. The conventional DCM operation is realized by using diode-based nonsynchronous buck converter [8]. However, a large voltage drop cross the diode limits the conversion efficiency, especially when output voltage is low and output current is high. Another solution is combining a current sensing circuit with a power transistor to detect the inductor current. When the inductor current becomes negative, DCM controller keeps inductor current in zero which eliminates an undesirable reverse current. Designing a current sensing circuit, however, is still a challenging task in low-voltage low-power application.

In this paper, a low-voltage low-power buck converter is presented with a new automatic CCM/DCM controller for PV assisted energy-efficient LSI system [9]. The system block diagram is shown in Fig. 1. To manage the power from either the battery or the single-cell PV, the input voltage of the dc-dc

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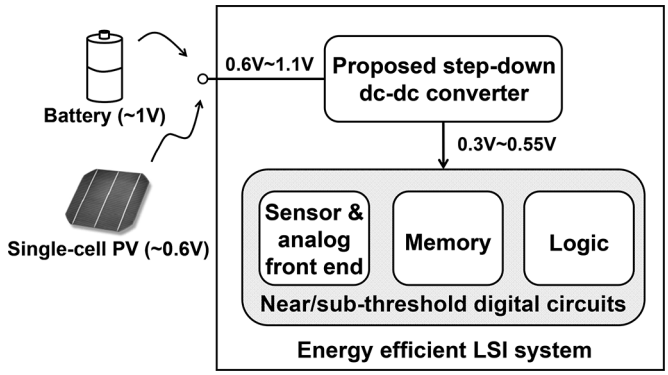


Fig. 1. System block diagram of PV assisted energy-efficient LSI system.

converter should cover from 0.6 V to 1.1 V. The targeted output voltage provided to near/sub-threshold digital circuits is between 0.3 V and 0.55 V for low-power operation. To accommodate the voltage regulation under such a low voltage, a D-flip-flop (DFF) based digital pulse-width modulation (PWM) controller is designed. An automatic CCM/DCM controller adaptively selects the operation mode under different load current to extend the output current range. To detect the inductor current, a dual-mode-body-biased (DMBB) zero-crossing detector is also proposed to enable low-voltage DCM operation for wide operating voltage. The proposed buck converter achieves a peak efficiency of 94% with an output range of 50 μA to 10 mA. Comparing with the conventional diode-mode DCM operation, the conversion efficiency can be improved effectively by 15%, with an output voltage of 0.35 V. Comparing with CCM operation, by applying DMBB for CCM/DCM operation, the conversion efficiency at 100 μA output current is improved by 20% and 9%, with an output voltage of 0.35 V and 0.5 V, respectively.

This paper is organized as follows. The top-level architecture and design considerations of the proposed buck converter are described in Section II. Section III shows the detailed circuit implementation of key building blocks. The experimental results and comparison with the state-of-the-art are shown in Section IV. Finally, a conclusion is given in Section V.

II. System Architecture and Design Considerations

The top-level block diagram of the proposed buck converter is shown in Fig. 2. The proposed buck converter consists of a clock generator, a digital PWM controller, an automatic CCM/DCM controller, and a power stage.

The power stage consists of gate drive buffers, power MOS ($\mathrm{M_P}$ and $\mathrm{M_N}$), and a LC filter. Sizes of $\mathrm{M_P}$ and $\mathrm{M_N}$ are optimized at a center output current of 2 mA, with the trade-off between conduction loss and gate driving loss. In designing a power stage of a buck converter, three important design parameters have to be determined: output capacitor (C), output inductor (L), and switching frequency ($\mathrm{f_{SW}}$). These parameters can be theoretically calculated from basic specifications of buck converter, i.e., input voltage ($\mathrm{V_{IN}}$), output voltage ($\mathrm{V_{OUT}}$), maximum output current ($\mathrm{I_{OUT}}$), output ripple ($\Delta\mathrm{V_{OUT}}$), current ripple of inductor ($\Delta\mathrm{I_L}$), estimated efficiency (η), etc. In this buck converter, digital control block is used for low power applications with less than 10 mA output current, in order to achieve a high efficiency, we would expect a low switching frequency to minimize the switching loss and the digital control loss. Therefore to accommodate low current in the inductor with wide clock period, the inductor size should be relatively large. On the other hand, to minimize the cost of an off-chip inductor and the board size, the package of the inductor should be small. A trade off is made by selecting the largest inductor value available in a 0805 surface-mount device (SMD). Therefore, L of 220 μH is selected.

The output capacitor C is normally calculated from $\Delta\mathrm{I_L}$, $\mathrm{f_{SW}}$, and $\Delta\mathrm{V_{OUT}}$ [10]. In this design, digital controller is used for PWM modulation. Therefore to reduce power consumption of the controller, $\mathrm{f_{SW}}$ is set to a low frequency of 100 kHz. Then the minimum capacitance required can be calculated by the following equation:

$$C_{\min} = \frac{\Delta I_L}{8 \times f_{\mathrm{SW}} \times \Delta V_{\mathrm{OUT}}} = \frac{4\ \mathrm{mA}}{8 \times 100\ \mathrm{kHz} \times 30\ \mathrm{mV}} \approx 167\ \mathrm{nF} \quad (1)$$

where $\Delta\mathrm{I_L}$ is estimated as 40% of the output current (10 mA), and $\Delta\mathrm{V_{OUT}}$ is worst case output ripple of 30 mV Keeping in mind that some ripple introduced by the ESR of the output capacitor is not included in the above equation, and the demand to push down the cutoff frequency ($\mathrm{f_{cutoff}}$) to much lower than $\mathrm{f_{SW}}$, a larger capacitance of 1 μF is chosen for output capacitor C. Then the cutoff frequency of LC filter can be calculated as follows:

$$f_{\mathrm{cutoff}} = \frac{1}{2\pi \times \sqrt{L \times C_{\min}}} \approx 10.7\ \mathrm{kHz}. \quad (2)$$

The ratio of $\mathrm{f_{SW}}$ over $\mathrm{f_{cutoff}}$ is around 9.3, which is large enough for the LC filter to filter out the switching noise in a practical converter.

A clock generator is employed to generate different frequencies for sub-blocks in the digital PWM controller. The system clock (CK1) frequency is 6.4 MHz, in order to have 100 kHz of switching frequency at power stage. The clock generator is simply DFF based power-of-2 frequency divider, generating frequencies of 1/64 and 1/1024 the rate of the main clock. CK1 of 6.4 MHz is used by DFFs. CK2 of 100 kHz is used by the clocked comparator. CK3 is used by the bi-directional shift register (SR). The switching frequency of power stage is set by the digital PWM controller at 100 kHz.

The digital PWM controller is employed to perform closed loop regulation of $\mathrm{V_{OUT}}$. A digital architecture is more attractive than an analog one for low supply voltage (0.6 V) and low output current. It utilizes three clock signals CK1, CK2, and CK3 generated by the clock generator, compares $\mathrm{V_{OUT}}$ with $\mathrm{V_{REF}}$, and then enables a pulse width modulated signal CK_buck for the power stage. More details will be discussed in Section III.

The CCM/DCM controller is employed to automatically generate the required gate signals (CKP and CKN) for $\mathrm{M_P}$ and $\mathrm{M_N}$ either in CCM or DCM operation. It will be explained in detail in Section III.

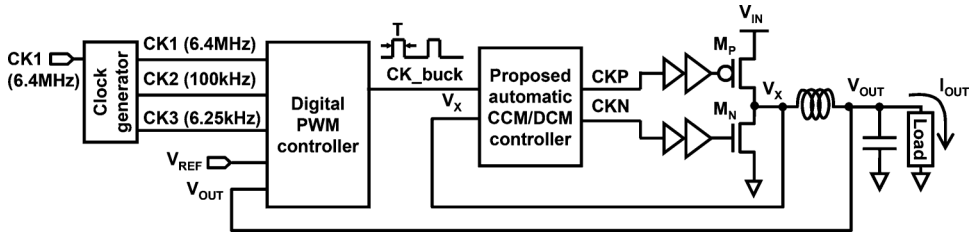


Fig. 2. Top-level block diagram of the proposed buck converter.

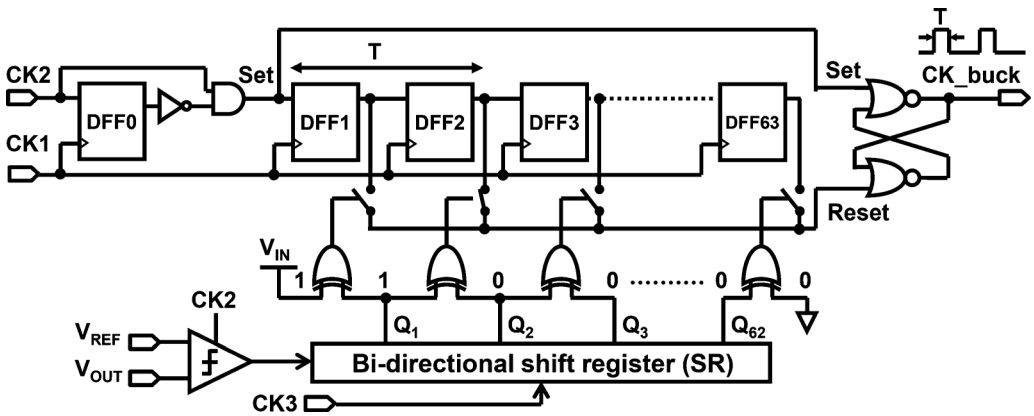


Fig. 3. Circuit diagram of digital PWM controller.

III. Circuit Level Implementation

A. Digital PWM Controller

In order to fit with the low supply voltage (0.6 V), a digital feedback architecture is more attractive than an analog one. The circuit diagram and timing diagram are shown in Figs. 3 and 4, respectively. A Set signal is generated from CK1 and CK2 by DFF0 and two logic gates. A latch-type comparator clocked at 100 kHz is used to compare V_{OUT} with V_{REF}, thereafter control the shifting direction of the SR. SR has thermal-code-like outputs, i.e., Q_{1-62}, as shown in Table I, which has 63 output states. By connecting Q_{1-62} to a serial of exclusive OR gates, and 63 switches, each of SR output state enables one of the switches. Only one of switches is turned on and one of DFFs' outputs is connect to Reset. In this way, a variable delay "T" is obtained to generate variable duty cycle for CK_buck. The variable duty varies from 1/64 (1.5625%) to 63/64 (98.4375%), with a step duty ΔD of 1/64 clock cycle. The reason to choose 64 clock phases in the Digital PWM Controller is to obtain a variable output voltage of buck converter with a tunable output voltage step of 10 mV. Increasing the number of phase can further improve the resolution of digital PWM and ripple, but it also increases the leakage and switching power of DFFs in the digital PWM controller. The tunable output voltage step ($V_{OUTstep}$) is calculated as follows:

$$V_{\mathrm{OUTstep}} = V_{\mathrm{IN}} \times \Delta D = 0.6\ \mathrm{V} \times \frac{1}{64} = 9.375\ \mathrm{mV}. \quad (3)$$

SR is clocked by CK3 which determines the duty varying frequency. CK3 is further reduced to 6.25 kHz to reduce the power consumption of SR, and to improve the light load efficiency. The transient response time is relatively long comparing with high frequency operation. However, the output of the buck converter is provided to near/sub-threshold digital circuits for low-power application, for instance, wireless sensor network,

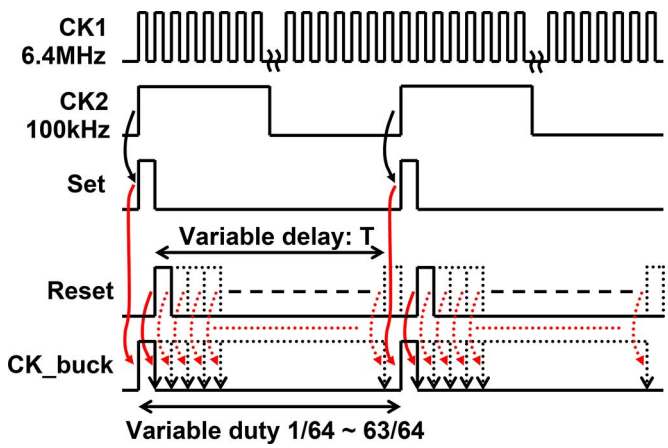


Fig. 4. Timing diagram of digital PWM controller.

TABLE I
Output State of Bi-Directional Shift Register (SR)

State \ Q_i	Q_1	Q_2	Q_3	.....	Q_{61}	Q_{62}
1	0	0	0	.....	0	0
2	1	0	0	.....	0	0
3	1	1	0	.....	0	0
4	1	1	1	.....	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
62	1	1	1	.....	1	0
63	1	1	1	.....	1	1

where the operating speed is limited and the transient performance requirement is relatively low.

CK_buck carrying appropriate duty information is then used by CCM/DCM controller to drive the power stage and to regulate V_{OUT} towards V_{REF}.

B. CCM/DCM Controller

To achieve high conversion efficiency, DCM is usually required in light load condition [11]. For a wide output current range, both CCM and DCM operations are essential for high efficiency. Selection of CCM/DCM is normally enabled by zero voltage switching (ZVS) technique [12], [13]. In previously published buck converters, either an external mode selection signal is required to change modes between CCM and DCM [14], or a complex synchronous logic circuit including DFF is required which consumes more power and may suffer from setup and hold errors at low V_{DD} [15]. While the proposed method offers a simple and low power automatic mode switching by using the proposed automatic CCM/DCM controller.

The circuit diagram of proposed automatic CCM/DCM controller is shown in Fig. 5. In DCM, a zero-cross switching is achieved to maximize the efficiency. The controller consists of only digital standard cells and a proposed dual-mode-body-biased (DMBB) zero-crossing detector. The zero-crossing detector is used to compare V_X with ground, therefore detect if the voltage at V_X has crossed 0 V. The rest digital standard cells generate the required gate driving signals (CKP and CKN), and automatically switch between CCM and DCM operations. A pulse converter is realized with inverters and AND gate, to convert a clock signal IN1 into a pulse signal OUT1. The pulse signals are used to set or reset the inputs of the SR-latch to generate CKN. The timing diagram of proposed automatic CCM/DCM controller is shown in Fig. 6. In CCM condition (Fig. 6(a)), when load current is high, inductor current (I_L) is always larger than zero. CKP is approximately equal to CK_buck. When CKP goes high, meaning M_P is turned off, a Set1 signal is generated by the pulse converter, and then CKN is set to high, so M_N is turned on accordingly. When M_P is turned off, V_X is always less than 0 V due to the conduction voltage drop of M_N, and the output of zero-crossing detector (ZCD) and Reset_DCM is always zero. CKN is then reset to zero by Reset_CCM. In contrast, in DCM condition (Fig. 6(b)), I_L sometimes drops to zero. CKN is set to high in the similar way as CCM. Then at the zero-crossing point (when $V_X = 0$ V and M_P is turned off), a pulse is generated for Reset_DCM and then CKN is reset to zero. In this way, the zero-cross switching (M_N is turned off when I_L becomes zero) is accomplished.

Non-overlap generation function is also implemented in the proposed automatic CCM/DCM controller. In Fig. 5, two buffers (buffer1 and buffer2) are used to adjust delays of different signal paths. The timing diagram of non-overlap clock signal is shown in Fig. 7. t_{CKP} delay is the delay from CK_buck to CKP, t_{CKNset} delay is the delay from CK_buck through Set1 to CKN, and $t_{CKNreset}$ delay is the delay from CK_buck through Reset_CCM to CKN. By adjusting the delays, non-overlap time can be generated. In this design, the loss contribution during the non-overlap time is not significant because of large clock cycle. Therefore, dynamic non-overlap control is not implemented to save power.

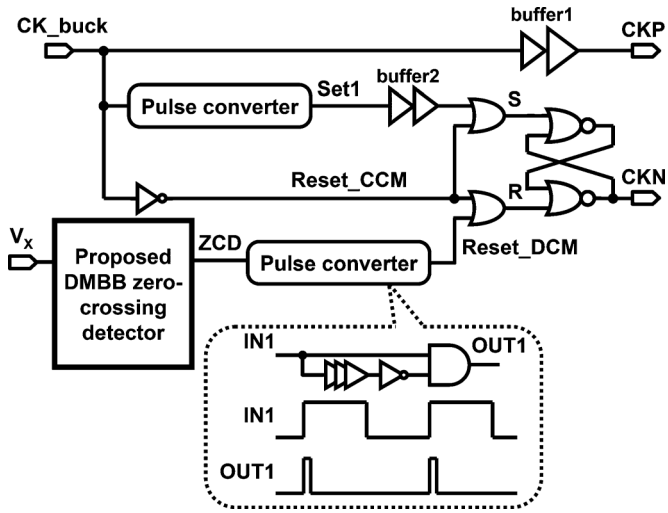


Fig. 5. Circuit diagram of proposed automatic CCM/DCM controller.

C. Dual-Mode-Body-Biased (DMBB) Zero-Crossing Detector

It is of great importance to detect when the inductor current becomes zero in a buck converter. There are several ways of doing current sensing. Simply inserting a resistor in series with the inductor will incur power loss in the resistor and therefore reduces the efficiency. Using low-pass RC network to filter the voltage across the inductor [16] can sense the current, but it needs exact value of inductor and additional R, C components. Using current mirror to sense the current in power MOSFET [17] needs OpAmp and therefore not suitable for low input voltage design.

In this work, a zero-crossing detector is used to sense V_X node voltage to detect when inductor current hits zero. The circuit diagram of proposed DMBB zero-crossing detector is shown in Fig. 8. It is designed to enable DCM operation with both low supply voltage (0.6 V) and normal supply voltage. The DMBB zero-crossing detector is based on a common-source differential input amplifier. M_{P1} and M_{P2} serve as the differential input pair, M_{P3} provides bias current for the amplifier, M_{N1} and M_{N2} are the mirroring components. The matching between M_{P1} and M_{P2}, M_{N1} and M_{N2}, are important, because due to process mismatch variation, there is an offset voltage in the zero-crossing detector. The offset may be positive or negative. If the offset is too large, the power NMOS M_N may be turned off early or late. Therefore, to reduce the offset voltage due to process variation, the transistor widths of M_{P1}, M_{P2}, M_{N1} and M_{N2} are designed to be at least ten times larger than the minimum width, and a gate length of four times the minimum gate length is used. Therefore, the offset of the zero-crossing detector is reduced and the loss caused by offset voltage variation is reduced.

At low V_{DD}, voltage headroom of the amplifier is quite limited. In order to have enough gm, either transistor size or bias current needs to be enlarged, which are definitely not desired for low-power design. A forward body bias is therefore beneficial in this design to alleviate the lack of voltage headroom with low

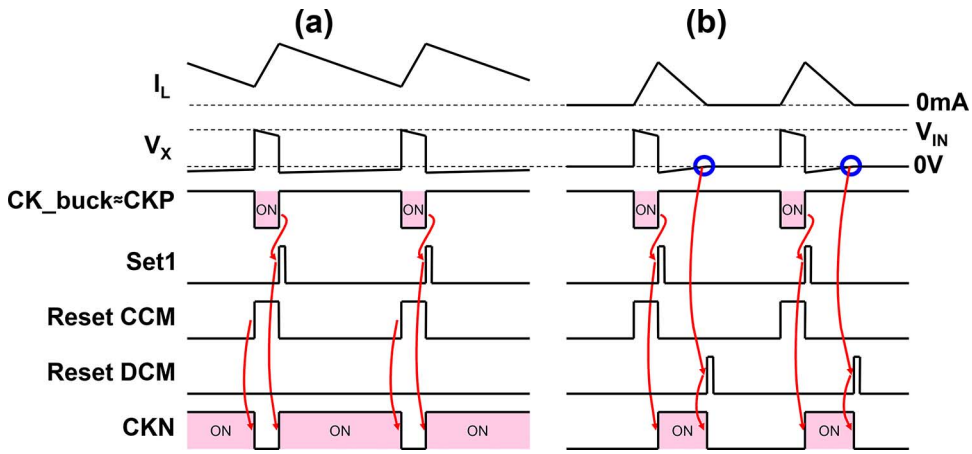


Fig. 6. Timing diagram of proposed automatic CCM/DCM controller with (a) CCM, (b) DCM operation.

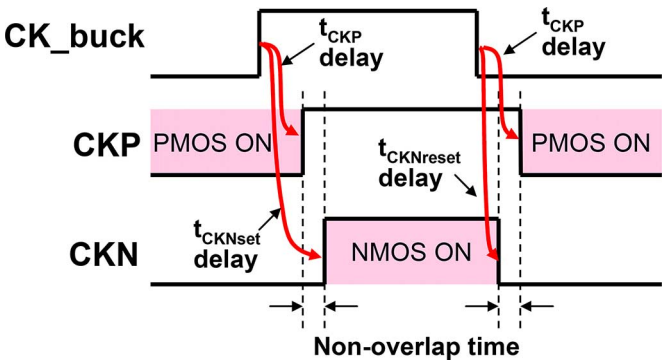


Fig. 7. Non-overlap time of proposed automatic CCM/DCM controller.

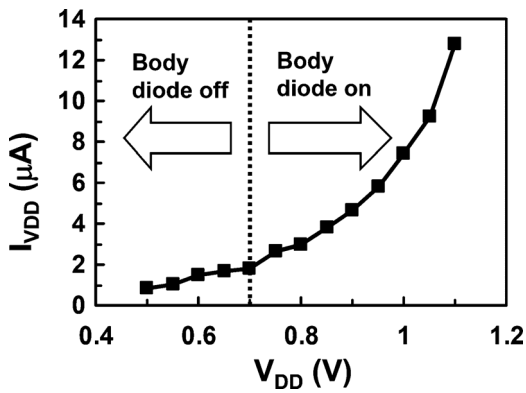


Fig. 9. Measured I_{VDD} of zero-crossing detector when forward body bias is enabled.

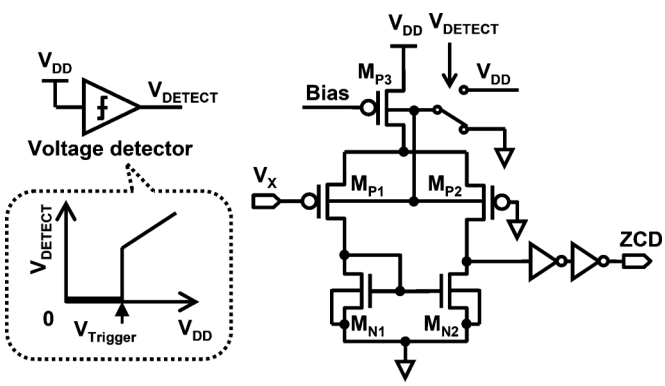


Fig. 8. Circuit diagram of proposed DMBB zero-crossing detector.

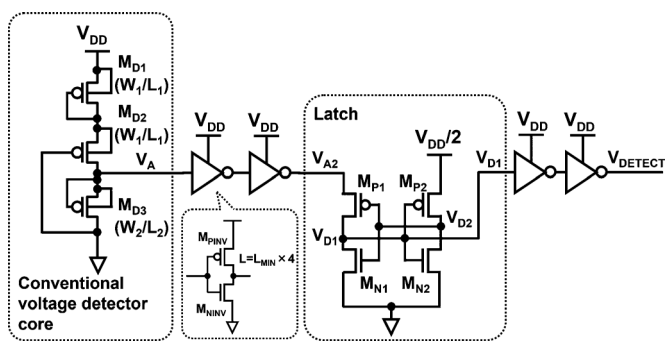


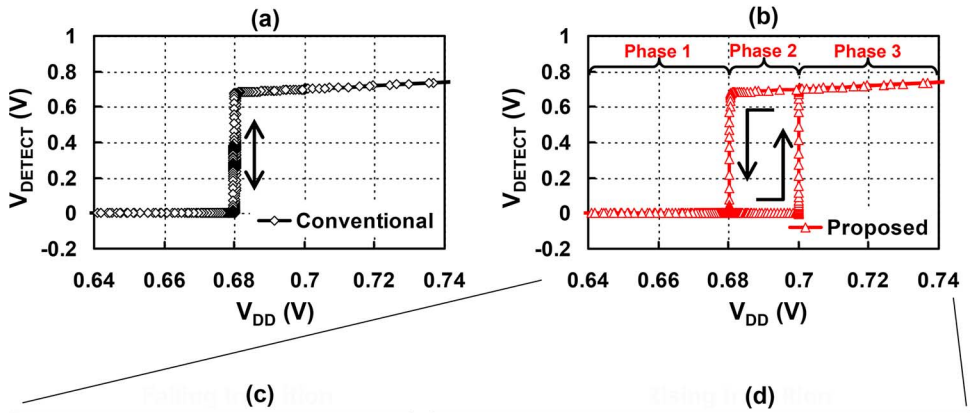
Fig. 10. Schematic of proposed ultra-low-power hysteresis voltage detector.

V_{DD}. The bodies of M_{P1-3} are connected to ground to enable the forward body bias, therefore reduce the threshold voltage of them.

However, such forward body bias is only applicable when V_{DD} is low, otherwise the body diode of PMOS would be turned on, and large forward current would flow through the diode. As shown in Fig. 9, I_{VDD} of the zero-crossing detector increases exponentially with V_{DD}. In order to avoid the large leak current from V_{DD}, forward body bias must be turned off when V_{DD} is larger than 0.7 V. An ultra-low-power voltage detector [18] is therefore required to switch body connection with regarding to different V_{DD}. $V_{Trigger}$ should be set to around 0.7 V in this design. Thus, when V_{DD} is lower than 0.7 V, the DMBB zero-crossing detector is forward body biased. In contrast, when V_{DD} is higher than 0.7 V, the detector is zero body biased. Therefore, the DMBB architecture achieves both a fast voltage detection operation at low V_{DD} and small body diode leak current at high V_{DD}.

D. Ultra-Low-Power Hysteresis Voltage Detector

To adaptively switch the body of the zero-crossing detector, an ultra-low-power hysteresis voltage detector is added. As shown in Fig. 10, the proposed circuit is constructed from a PMOS-based voltage detector core [18], inverter buffers and



(c)

		Phase 1 ⇦	Phase 2,3
V_{A2}		0	V_{DD}
V_{D1}		0	V_{DD}
V_{D2}		$V_{DD}/2$	0
V_{DETECT}		0	V_{DD}
V_{GS}	M_{P1}	$V_{DD}/2$ (off)	$-V_{DD}$ (on)
	M_{N1}	$V_{DD}/2$ (on)	0 (off)
	M_{P2}	$-V_{DD}/2$ (on)	$V_{DD}/2$ (off)
	M_{N2}	0 (off)	V_{DD} (on)

(d)

		Phase 1	⇨ Phase 2	⇨ Phase 3
V_{A2}		0	V_{DD}	V_{DD}
V_{D1}		0	0	V_{DD}
V_{D2}		$V_{DD}/2$	$V_{DD}/2$	0
V_{DETECT}		0	0	V_{DD}
V_{GS}	M_{P1}	$V_{DD}/2$ (off)	$-V_{DD}/2$ (on)	$-V_{DD}$ (on)
	M_{N1}	$V_{DD}/2$ (on)	$V_{DD}/2$ (on)	0 (off)
	M_{P2}	$-V_{DD}/2$ (on)	$-V_{DD}/2$ (on)	$V_{DD}/2$ (off)
	M_{N2}	0 (off)	0 (off)	V_{DD} (on)

Fig. 11. Simulated dependence of V_{DETECT} on V_{DD} in: (a) conventional voltage detector, (b) proposed voltage detector; and state analysis of proposed voltage detector in: (c) falling transition, (b) rising transition.

a latch. The detector core consists of three cascode PMOS transistors: M_{D1}, M_{D2}, and M_{D3}. M_{D1-3} are chosen to be pMOS transistors because pMOS has less process variation than nMOS. The upper side (M_{D1} and M_{D2}) are operating under sub-threshold region while the lower side (M_{D3}) is operating under cut-off region. V_A changes rapidly from low to high when the available drain current of upper side gets larger than off-current of M_{D3}. The inverter buffers are used to amplify the compared voltage signal V_A. During the transition state, when V_A changes from low to high, V_A is in the range from 0 to $V_{DD}/2$. Therefore, the length of the PMOS transistor in the first inverter (M_{PINV}) is designed with four times gate length than that of NMOS transistor to correctly detect the trigger voltage. Also after V_A changes from low to high, V_A is still lower than V_{DD}, and M_{PINV} cannot be fully turned off. By applying four times larger gate length, the leakage current after V_A goes high can be reduced.

The voltage detector in [18] provides only one trigger level. In order to avoid miss-detection caused by noise or disturbance around the trigger level, a hysteresis characteristic is required. A cross-coupled CMOS latch is added after the inverter buffers to realize hysteresis levels. The latch is composed of transistors M_{N1}, M_{N2}, M_{P1}, and M_{P2}, which use twice of the minimum channel length to reduce the leakage current. The source of M_{P2} is connected to $V_{DD}/2$ while source of M_{P1} is connected to V_{A2} to shift the level of trigger voltage in rising transition. Because the hysteresis voltage detector does not need a high operating speed, the Vdd/2 does not need to provide large current. Therefore it is generated by off-chip resistive voltage divider, and consumes only a few nA current. Also the Vdd/2 does not have to be very accurate, which alleviates the PVT variation requirement. The simulated dependence of V_{DETECT} on V_{DD} of conventional and proposed voltage detectors with rising and falling transition of V_{DD} are shown in Fig. 11(a) and (b). The DC operating points in each phase of Fig. 11(b) are shown in Fig. 11(c) and (d). When V_{DD} is decreasing (falling transition), there are two different operation phases: phase 1 and phase 2&3, as shown in Fig. 11(c). DC operation condition in phase 2 and phase 3 are the same. The trigger voltage of the proposed scheme is equal to the conventional voltage detector. When V_{A2} changes from V_{DD} to 0 V, V_{D1} is pushed to 0 V ignoring the voltage at V_{D2}, because V_{D1} is in the middle between V_{A2} to ground. Thus V_{DETECT} provides "low".

On the other hand, when V_{DD} is increasing (rising transition), there are three operation phases, as shown in Fig. 11(d). Phase 2 and phase 3 in rising transition have different dc operation condition to generate the hysteresis voltage levels. During phase 2 operation, $V_{A2} = V_{DD}$ and $V_{D2} = V_{DD}/2$, which means M_{P1} and M_{N1} are both operating under sub-threshold region and turned-on slightly. Since the current flowing through M_{P1} and M_{N1} are the same, V_{D1} is determined by R_{ds} ratio of transistors M_{P1} and M_{N1}. Initially, V_{D1} provides "low" because in the end of phase 1, V_{D1} is 0 V and V_{D2} is $V_{DD}/2$. Then V_{D1} increases as V_{DD} increases. When V_{D1} reaches a critical value, V_{D2} decreases because of voltage division caused by transistor M_{N2} and M_{P2}, and positive feedback in latch flips V_{D1} from low to high. The critical value of V_{D1} is determined by the size ratio between NMOS and PMOS transistors in latch circuit. In our design, the channel width of M_{P1} and M_{P2} is three times larger than that of M_{N1} and M_{N2} to generate 20 mV hysteresis.

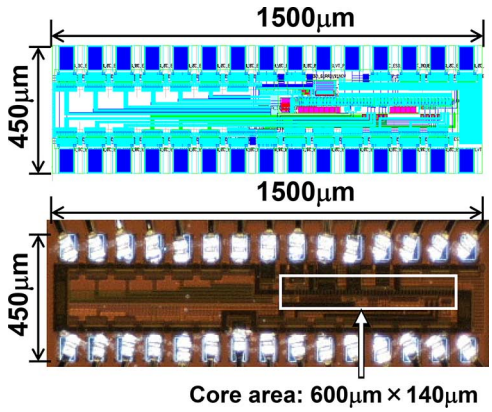


Fig. 12. Layout and die photo.

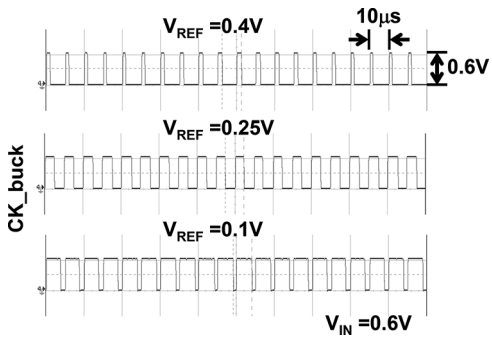


Fig. 13. Measured CK_buck waveforms of digital PWM controller with different V_{REF}.

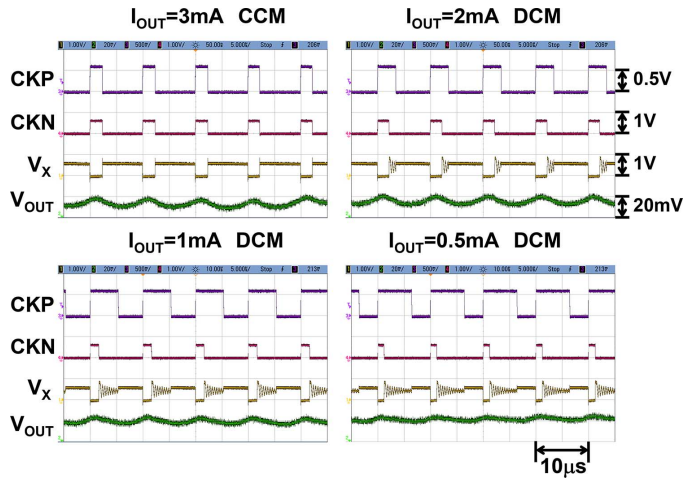


Fig. 14. Measured waveforms of buck converter in CCM and DCM at $V_{IN} = 0.6$ V and $V_{OUT} = 0.35$ V.

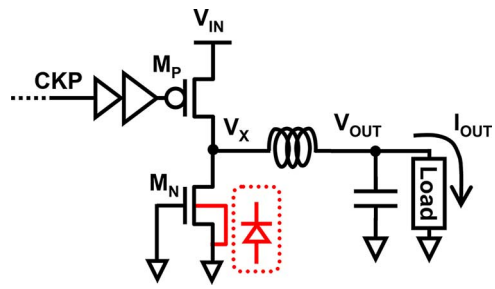


Fig. 15. Simplified circuit diagram of diode mode buck converter.

IV. Experimental Results

The proposed buck converter is fabricated with 40 nm CMOS process. Fig. 12 shows the layout and the chip microphotograph. The total area including test structure is 450 μm by 1050 μm. The active area is 0.084 mm^2.

Fig. 13 shows the measured output signals of the digital PWM controller, i.e., CK_buck, at different V_{REF}. It is observed that duty cycle of CK_buck changes proportionally as V_{REF} changes meaning successful pulse width modulation of the buck converter.

Fig. 14 shows the measured waveforms of the proposed buck converter at $V_{IN} = V_{DD} = 0.6$ V and $V_{OUT} = 0.35$ V with different output current (I_{OUT}). At I_{OUT} of 3 mA, the buck converter is in CCM operation, it can be seen from the fact that CKN is in the same shape with CKP. At I_{OUT} from 2 mA to 0.5 mA, CKN transits from V_{IN} to zero before CKP goes to zero, meaning M_N is turned off before M_P is turned on, and both M_N and M_P are turned off when I_L is zero. Therefore it is in DCM operation. The worst case output voltage ripple is 11 mV (peak-to-peak) at $I_{OUT} = 2$ mA.

For comparison purpose, a conventional diode-based nonsynchronous buck converter is also implemented and measured. The simplified schematic of the conventional diode mode buck converter is shown in Fig. 15. Fig. 16 shows the measured power efficiency of the diode mode converter and the proposed buck converter, with V_{IN} of 0.6 V. Efficiency of an ideal LDO is also shown in Fig. 16. It can be easily calculated as 83% and 58%, for V_{OUT} of 0.5 V and 0.35 V, respectively. The proposed buck converter has a higher efficiency than an ideal LDO. Compared with diode mode converter, the maximum efficiency improvement by the proposed buck converter is 3% and 15%, at V_{OUT} of 0.5 V and 0.35 V, respectively. That is because the diode mode converter suffers from diode reverse recovery loss, and diode conduction loss, especially when V_{OUT} is low, meaning duty cycle is small and diode conducts more often.

Fig. 17 shows the measured power efficiency of proposed buck converter with both CCM and DCM operation, and conventional one with only CCM operation. V_{IN} is set to 0.6 V, and V_{OUT} is set to 0.35 V and 0.5 V. When I_{OUT} is larger than 2 mA, both proposed and conventional buck converters are in CCM operation, therefore the same efficiency is achieved. In contrast, when I_{OUT} is less than 2 mA, the proposed buck converter is in DCM operation, therefore significant efficiency improvement is achieved. The power efficiency at I_{OUT} of 100 μA is improved by 20% and 9%, at V_{OUT} of 0.35 V and 0.5 V, respectively. The peak efficiency of 94% is achieved by the proposed buck converter at I_{OUT} of 2 mA, thanks to the proposed low-power CCM/DCM controller and the low-power digital PWM controller.

Table II shows the comparison with the published low-voltage buck converters. Compared with [11], [14] and [15], the proposed buck converter achieves higher peak efficiency and lower V_{IN} and V_{OUT}. While compared with [7],

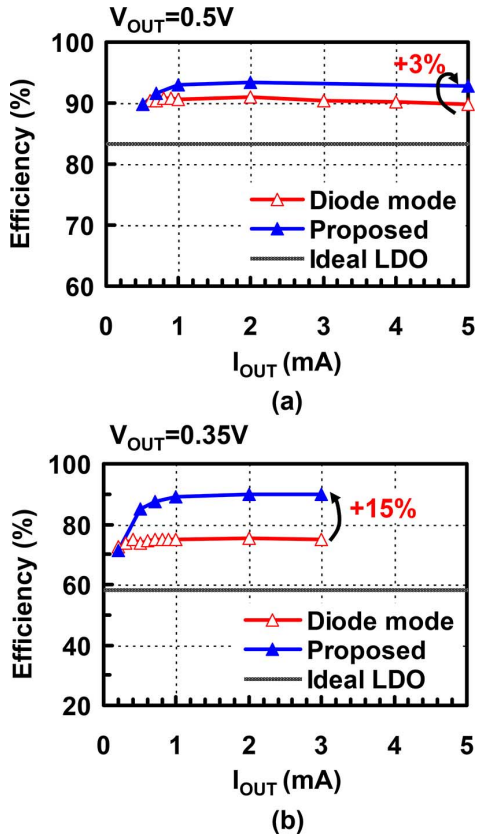


Fig. 16. Measured efficiency of proposed buck converter and diode mode buck converter with $V_{IN} = 0.6$ V, and (a) $V_{OUT} = 0.5$ V, (b) $V_{OUT} = 0.35$ V.

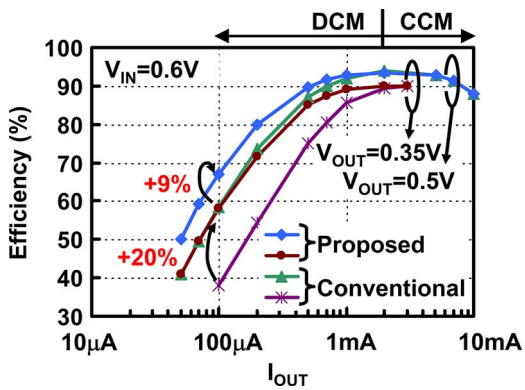


Fig. 17. Measured efficiency of proposed CCM/DCM buck converter and conventional CCM converter.

the proposed buck converter has wider V_{IN} range and smaller inductor value.

V. Conclusion

In this paper, a low-voltage low-power buck converter is proposed for wireless sensor network systems. A digital PWM controller is implemented for voltage regulation. An automatic CCM/DCM controller is proposed to adaptively select CCM or DCM operation, therefore improving the power efficiency of the buck converter. A low-voltage DMBB zero-crossing detector is proposed to enable DCM operation with both low supply voltage and normal supply voltage. An ultra-low-power hysteresis voltage detector is designed for body bias mode selection. By virtue of the low power controller, the proposed buck converter achieves a peak efficiency of 94% with an output current range of 50 μA to 10 mA. Thanks to the DCM operation, the efficiency at an output current of 100 μA is improved by 20% and 9%, with an output voltage of 0.35 V and 0.5 V, respectively.

TABLE II
Comparison With Published Low-Voltage Buck Converters

	[7] VLSI 2012	[11] ISSCC 2007	[14] JSSC 2011	[15] VLSI 2010	This work
V_{IN} (V)	0.45	1.2	2.8-4.2	1.8	0.6-1.1
V_{OUT} (V)	0.34-0.44	0.5	0.6-1.2	0.575	0.3-0.55
I_{OUT}	0.67μA-410μA	2μA-200μA	20μA-100mA	0.7μA-107μA	50μA-10mA
Peak efficiency	97%	86%	87.4%	90%	94%
L	47mH	2μH	10μH	-	220μH
Switching frequency	20kHz	-	2MHz	-	100kHz
Operating mode	CCM	DCM	CCM/DCM *external mode selection signal needed.	CCM/DCM *complex synchronous logic circuit needed.	CCM/DCM

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