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Design guidelines to achieve minimum energy operation for ultra low voltage tunneling FET logic circuits

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A tunneling field effect transistor (TFET) attracts attention, because TFET circuits can achieve better energy efficiency than conventional MOSFET circuits. Although design issues in ultra low voltage logic circuits, such as the minimum operatable voltage (V_{DDmin}), have been investigated for MOSFET's, V_{DDmin} for TFET's have not been discussed. In this paper, V_{DDmin} of TFET logic circuits is evaluated for the first time and a closed-form expression of V_{DDmin} is derived, which indicates that the within-die threshold voltage variation (σ_{VT}) strongly affects V_{DDmin}. In addition, since it is not clear how much the energy of the logic circuits is quantitatively reduced when both the subthreshold swing (S) and the power supply voltage are reduced, an analytical equation of the minimum energy of TFET logic circuits is also derived. From the derived equations, the design guideline is presented for the device engineers of TFET's that σ_{VT} should be reduced as S decreases.

1. Introduction

A tunneling field effect transistor (TFET) is drawing attention with the expectation that a TFET circuit provides better energy efficiency than a conventional MOSFET counterpart by reducing leakage in ultra low voltage domain.[1–5] Power dissipation of CMOS logic circuits (P) is expressed as

$$P = \alpha N C_0 V_{DD}^2 f_{CLK} + N I_{OFF} V_{DD}, \quad (1)$$

where V_{DD} is the supply voltage, α is an activity ratio, C_0 is an input capacitance of a logic gate, such as an inverter or a NAND gate, I_{OFF} is a leakage current of the logic gate, N is the total number of logic gates, and f_{CLK} is a clock frequency. Thus, power delay product, that is, energy of CMOS logic circuits (E) is given by

$$E = P \cdot T_{CLK} = \alpha N C_0 V_{DD}^2 + N I_{OFF} V_{DD} T_{CLK}, \quad (2)$$

where T_{CLK} is a clock period. T_{CLK} can be expressed as

$$T_{CLK} = L_{DP} \cdot K \frac{C_0 V_{DD}}{I_{ON}}, \quad (3)$$

where L_{DP} is the depth of the critical path, K is a delay fitting parameter,[6] and I_{ON} is ON current of the logic gate, which corresponds to the current to charge or discharge the load capacitance. Thus, Eq. (2) is rewritten by

$$E = \alpha N C_0 V_{DD}^2 + N I_{OFF} V_{DD} L_{DP} K \frac{C_0 V_{DD}}{I_{ON}}$$
$$= L_{DP} K \cdot N C_0 V_{DD}^2 \left(\frac{\alpha}{L_{DP} K} + \frac{I_{OFF}}{I_{ON}} \right). \quad (4)$$

If the circuit structure is identical, L_{DP}, α, and N are constant. Assuming that K does not depend on V_{DD}, the energy of CMOS logic circuits can be expressed in the standard notation as

$$E \propto C_0 V_{DD}^2 \left(\xi + \frac{I_{OFF}}{I_{ON}} \right), \quad (5)$$

where ξ ($= \alpha / L_{DP} K$) is an effective time ratio and normally around 10^{-3} for logic circuits.[7]

Figure 1 shows the energy of TFET and MOSFET logic circuits ($\xi = 10^{-3}$) calculated by Eq. (5). As shown in this figure, the energy has a minimum value at around 0.1 V for TFET and 0.31 V for MOSFET. This is because I_{OFF}/I_{ON} depends on V_{DD} and increases as V_{DD} is reduced. In the nominal V_{DD} region, I_{OFF}/I_{ON} is much smaller than ξ, and hence the energy decreases as V_{DD} is reduced. In the ultra low V_{DD} region, on the other hand, I_{OFF}/I_{ON} is larger than ξ, and hence the energy increases as V_{DD} is reduced. This means that the energy is minimized at a certain supply voltage, and here we define such voltage as V_{OPT} and the minimum energy as E_{OPT}. The closed-form expression of V_{OPT} will be derived in Sect. 4. In order to achieve the high energy efficiency, the circuit must be operated at $V_{DD} = V_{OPT}$.

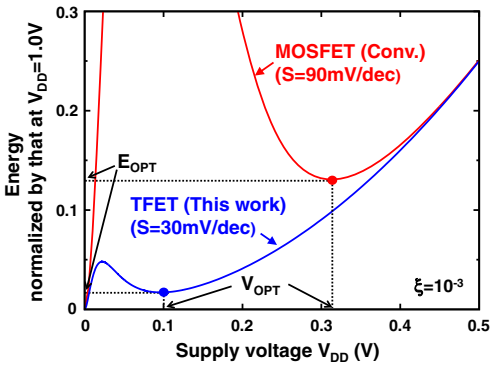

Fig. 1. (Color online) Energy dependence on supply voltage (V_{DD}) for TFET and MOSFET logic circuits.

As shown in Fig. 1, V_{OPT} of TFET logic circuits is much lower than that of MOSFET logic circuits. This is because V_{OPT} depends on I_{OFF}/I_{ON} in Eq. (5), and I_{OFF}/I_{ON} of TFET's is smaller than that of conventional MOSFET's at the same V_{DD} thanks to steeper S. It is not clear, however, how much V_{OPT} and E_{OPT} are quantitatively reduced when both the subthreshold swing (S) and V_{DD} are reduced. Therefore, in this paper, analytical equations of V_{OPT} and E_{OPT} for TFET logic circuits are proposed in Sect. 4. These equations show that V_{OPT} is proportional to S, and E_{OPT} is proportional to the square of S.

Such ultra low V_{DD} operation at V_{OPT} could cause functional errors. A minimum operatable voltage (V_{DDmin}) is the lowest voltage at which these functional errors do not occur.[8] If V_{DDmin} were higher than V_{OPT}, minimum energy

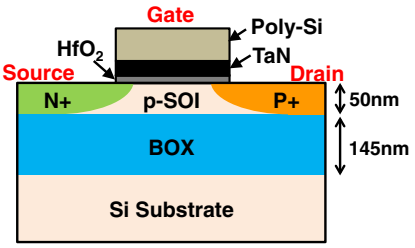

Fig. 2. (Color online) Cross-section of pTFET.

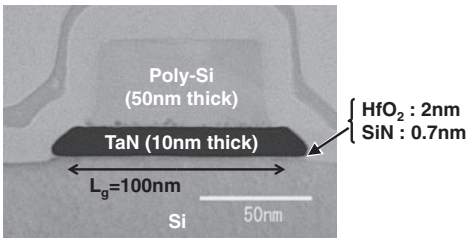

Fig. 3. Cross-sectional TEM image of pTFET.

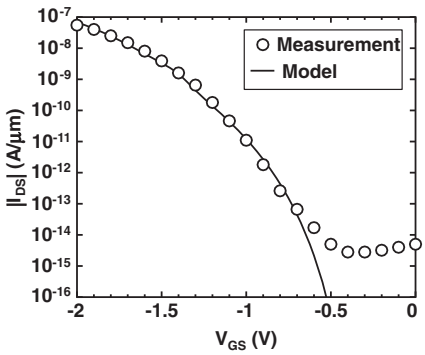

Fig. 4. Measured and simulated characteristics of pTFET.

operation could not be achieved. Especially V_{OPT} of TFET logic circuits is much lower than that of MOSFET logic circuits as shown in Fig. 1, and hence investigations on V_{DDmin} are essential for TFET logic circuits. Although variations in TFET devices have been analyzed in the previous works,[9,10] it is not clear how such variations affect V_{DDmin}. In this paper, V_{DDmin} of TFET logic circuits is investigated for the first time, and it is revealed that V_{DDmin} of TFET logic circuits can be modeled in the same manner as MOSFET logic circuits, which indicates that V_{DDmin} is proportional to the standard deviation of the within-die threshold voltage (V_{TH}) variations (σ_{VT}).

From the equations of V_{OPT} and V_{DDmin} derived in this paper for TFET logic circuits, this paper finally shows the design guideline for the device engineers of the steep S devices that σ_{VT} should be reduced in proportion to S.

The remainder of this paper is organized as follows. Section 2 explains the TFET model used in this paper. Using this model, V_{DDmin} of TFET logic circuits is investigated and the simulation results are shown in Sect. 3. Section 4 derives the condition that V_{TH} variation of TFET's must satisfy to achieve the minimum energy operation for TFET logic circuits and shows a guideline for the device engineers of the steep S devices. Finally, Sect. 5 concludes this paper.

2. TFET model used for simulation with V_{TH} variability

To perform TFET circuit investigation under V_{TH} variability, a device model is needed. A measured Si TFET device as an example is shown in Figs. 2 and 3. A compact model is elaborated and is implemented as a SPICE Verilog-A model, whose calculation result is shown in Fig. 4 and shows good agreement with the measurement.[11,12] Discrepancy in very low current region is due to the gate leakage but the region is not used in the simulations in this paper.

With the manufactured device described above, it is impossible to achieve steep-S feature at ultra low V_{DD} region and thus in the simulation below, a work function parameter is modified and Si is changed to Ge to enable low V_{DD} operations, since Ge-based TFET's can achieve larger ON currents.[13–15] The resultant I_{DS}–V_{DS} characteristics which are used in this paper are shown in Fig. 5. Esaki diode current component is included.

I_{DS}–V_{GS} characteristics in Figs. 5(c) and 5(d) show the cases when V_{TH} is shifted by ±30 mV through changing the work function parameter. The exact physical origin of the V_{TH} variation is not in focus here but rather the existence of the V_{TH} variation is important since V_{TH} changes the current exponentially, which in turn affects the circuit behavior strongly. The compact model, being different from a table model, enables the V_{TH} variability simulation.

3. Minimum operatable voltage of TFET logic circuits

In CMOS logic gates, there is a minimum operatable voltage, V_{DDmin}, below which a logic LSI stops operating. Although the previous work[8] has proposed the theoretical model of V_{DDmin} for conventional MOSFET logic circuits and verified the model with simulation and measurement results, it is not clear whether the model is applicable to TFET logic circuits. Thus, V_{DDmin} model is investigated for TFET logic circuits and verified with simulations in this section. It should be noted that V_{DDmin} determined by a logical failure due to setup and hold errors is not focused on in this paper.

I–V characteristics of MOSFET's in subthreshold region are written by[8]

$$I_{DS} = I_{M0} \exp\left(\frac{V_{GS} - V_{TH} + \eta V_{DS}}{S \cdot \log_{10} e}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right], \quad (6)$$

where I_{M0} is the current at $V_{DS} = V_{GS} = 0$ V, S is the subthreshold swing parameter, η is the DIBL coefficient and U_T is the thermal voltage. Actually, I–V characteristics of TFET's in low V_{DS} region differ from those of conventional MOSFET's shown in Eq. (6). In this paper, the following approximated expression of I–V characteristics of TFET's based on Eq. (6) is introduced for the ease of derivation of V_{DDmin} as

$$I_{DS} = I_{T0} \exp\left(\frac{V_{GS} - V_{TH}}{S \cdot \log_{10} e}\right)\left[1 - \exp\left(-\frac{V_{DS}}{m}\right)\right], \quad (7)$$

where I_{T0} is the current at $V_{DS} = V_{GS} = 0$ V, S is the average subthreshold swing parameter, and m is the saturation voltage constant, which corresponds to the thermal voltage (U_T) for MOSFET's.

Figure 6 shows I_{DS}–V_{GS} characteristics of TFET calculated by Eq. (7) and obtained by SPICE simulations with the

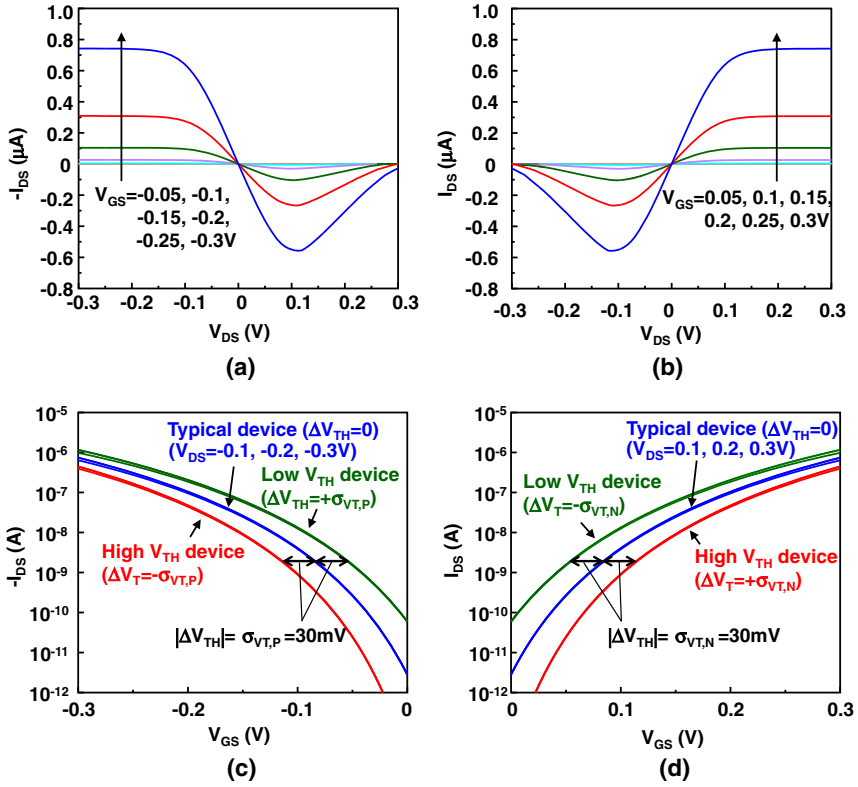

Fig. 5. (Color online) I–V characteristics of pTFET and nTFET: (a) I_{DS}–V_{DS} of pTFET, (b) I_{DS}–V_{DS} of nTFET, (c) I_{DS}–V_{GS} of pTFET, and (d) I_{DS}–V_{GS} of nTFET. ΔV_{TH} represents V_{TH} shift from center (typical) value caused by V_{TH} variation.

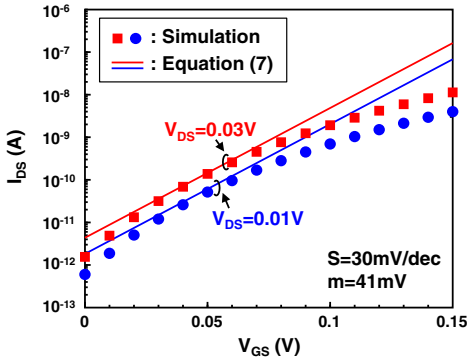

Fig. 6. (Color online) I_{DS}–V_{GS} characteristics of nTFET obtained by simulations with compact model described in Sect. 2. I_{DS}–V_{GS} characteristics calculated by Eq. (7) are also plotted.

compact model described in Sect. 2. Strictly speaking, S has voltage dependence in TFET as shown in Fig. 6. However, it is small at ultralow V_{DD}. Hence, in carrying out the theoretical calculation, S is approximated as an average over 0 and 0.1 V.

The closed-form expression of V_{DDmin} for MOSFET logic circuits has been derived from the subthreshold characteristics of MOSFET's shown in Eq. (6).[8] Based on this derivation, V_{DDmin} of TFET logic circuits can be derived from Eq. (7) as

$$V_{DDmin} = \sigma_{VT}\sqrt{\frac{\pi}{2}\ln N} + k \cdot S, \tag{8}$$

where N is the number of gates and k is the device-dependent parameter. σ_{VT} is defined as

$$\sigma_{VT} = \sqrt{\sigma_{VT,P}^2 + \sigma_{VT,N}^2}, \tag{9}$$

where $\sigma_{VT,P}$ and $\sigma_{VT,N}$ are standard deviations of the within-die V_{TH} variation of pTFET and nTFET, respectively, as shown in Figs. 5(c) and 5(d). In this paper, it is assumed that V_{TH} is normally distributed.

In order to evaluate the validity of Eq. (8), V_{DDmin}'s of TFET logic gates are also obtained by Monte Carlo SPICE simulations. These simulations comply with the procedure described in the previous work.[8]

Figure 7 illustrates V_{DDmin}'s of inverter chains obtained by Monte Carlo simulations and calculated by Eq. (8). V_{DDmin}'s calculated by Eq. (8) agrees with those obtained by the simulations. This coincidence of theory and simulation shows the validity of the approximation in Eq. (7). As shown in Fig. 7, V_{DDmin} of TFET logic circuits is proportional to the square-root of logarithm of the number of gates and its slope and y-intercept depend on σ_{VT} and S, respectively, which is the same conclusion drawn for a normal MOSFET case.[8] The derivation is based on inverters but it was shown that the expression works well with NAND's and NOR's.[8] It has been reported that the TFET drain current has temperature dependence but the major effect is on magnitude of the drain current and temperature dependence of S at low voltage region is small.[11,12]

In this section, V_{DDmin} of TFET logic circuits was investigated and we conclude that V_{DDmin} of TFET logic circuits can be modeled in the same manner as MOSFET's.

4. V_{TH} variation required for minimum energy operation

In this section, V_{OPT} and E_{OPT} expressions of MOSFET and

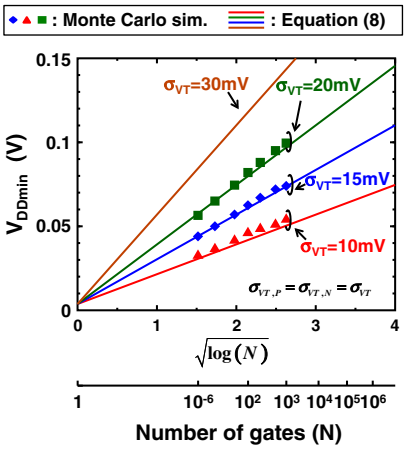

Fig. 7. (Color online) V_{DDmin}'s of TFET inverter chains obtained by Monte Carlo simulations and closed-form expression [Eq. (8)].

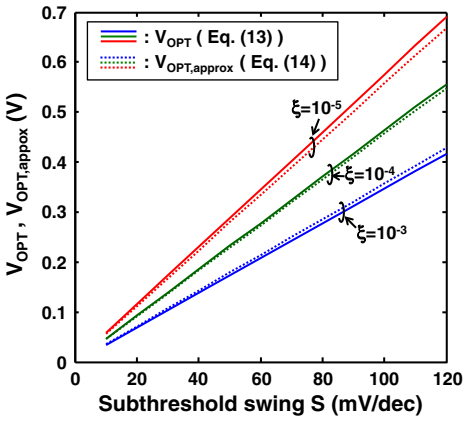

Fig. 8. (Color online) V_{OPT} obtained by Eq. (13) and its approximated value ($V_{OPT,approx}$) calculated by Eq. (14). $V_{OPT,approx}$ is a good approximation of V_{OPT}.

TFET logic circuits are analytically derived. From those expressions and V_{DDmin} expression described in Sect. 3, the condition that the within-die V_{TH} variation must satisfy to achieve the minim energy operation is derived. This will be a guideline for the device engineers of the steep S devices.

The energy of MOSFET circuits (E) is given from Eq. (5) by

$$E \propto C_0 V_{DD}^2 \left(\xi + \frac{I_{OFF}}{I_{ON}}\right) = C_0 V_{DD}^2 \left[\xi + \frac{I_{DS}(V_{GS}=0, V_{DS}=V_{DD})}{I_{DS}(V_{GS}=V_{DS}=V_{DD})}\right]. \quad (10)$$

In the subthreshold region, I–V characteristics of MOSFET's are given by Eq. (6). Therefore, the energy can be expressed as

$$E \propto C_0 V_{DD}^2 \left\{\xi + \exp\left[-\frac{(1+\eta)V_{DD}}{S \cdot \log_{10} e}\right]\right\}. \quad (11)$$

As shown in Fig. 1, the energy is minimized at $V_{DD} = V_{OPT}$. Thus, V_{OPT} satisfies the following equation:

$$\left.\frac{dE}{dV_{DD}}\right|_{V_{DD}=V_{OPT}} = 0. \quad (12)$$

Thus, V_{OPT} is derived as

$$V_{OPT} = S \cdot \frac{2 - W_{-1}(-2e^2\xi)}{(1+\eta)\ln 10}, \quad (13)$$

where $W_{-1}(x)$ is the lower branch of lambert W function. Although V_{OPT} has been derived in the previous work,[6] an approximate expression $V_{OPT,approx}$ of Eq. (13) is newly introduced in this paper to understand the dependence of V_{OPT} on ξ analytically as follows:

$$V_{OPT,approx} = S \cdot \frac{4(1-2e^2\xi) - \ln(2e^2\xi)}{(1+\eta)\ln 10}. \quad (14)$$

Figure 8 shows V_{OPT} and $V_{OPT,approx}$. The relative error ($|V_{OPT} - V_{OPT,approx}|/V_{OPT}$) is less than 3.2% under the condition of $10 < S < 120\,\text{mV/dec}$ and $10^{-3} < \xi < 10^{-5}$, which means $V_{OPT,approx}$ is a good approximation of V_{OPT}. It is not easy to understand the dependence of V_{OPT} on ξ in Eq. (13). However, Eq. (14) clearly indicates that V_{OPT} is reduced as ξ increases.

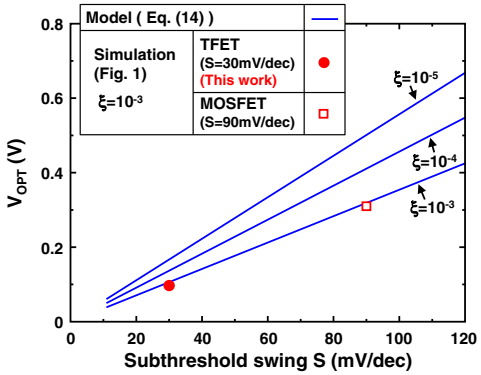

Fig. 9. (Color online) Dependence of V_{OPT} on subthreshold swing S.

Equation (14) suggests that V_{OPT} is proportional to S, that is, V_{OPT} is reduced as S decreases. Figure 9 shows V_{OPT} calculated by Eq. (14). V_{OPT}'s of MOSFET and TFET logic circuits obtained by SPICE simulations are also plotted. The simulated V_{OPT} of TFET circuits agrees with V_{OPT} calculated by Eq. (14), because I–V characteristics of TFET's can be expressed in the same manner as those of MOSFET's as shown in Eq. (7), which indicates that Eq. (14) is also applicable to TFET logic circuits.

The minimum energy E_{OPT} is expressed as

$$E_{OPT} = E(V_{DD} = V_{OPT}) \propto C_0 \cdot \xi \left[\frac{S}{(1+\eta)\ln 10}\right]^2 \frac{[2 - W_{-1}(-2e^2\xi)]^3}{-W_{-1}(-2e^2\xi)}. \quad (15)$$

Here, an approximate expression of E_{OPT} is also introduced to clarify the dependence of E_{OPT} on ξ as

$$E_{OPT,approx} \propto C_0 \cdot \xi \left[4.65 \frac{S}{(1+\eta)\ln 10}\right]^2 [-\ln(2e^2\xi)]. \quad (16)$$

Figure 10 shows E_{OPT} and $E_{OPT,approx}$. The relative error ($|E_{OPT} - E_{OPT,approx}|/E_{OPT}$) is less than 7.7% under the condition of $10 < S < 120\,\text{mV/dec}$ and $10^{-3} < \xi < 10^{-5}$, which means $E_{OPT,approx}$ is a good approximation of E_{OPT}. Equation (16) indicates that E_{OPT} is a quadratic function of S. S of the state-of-the-art MOSFET's is around 90 mV, whereas S of the TFET's used in this work is 30 mV. Equation (16) implies that the energy of TFET logic circuits can be reduced

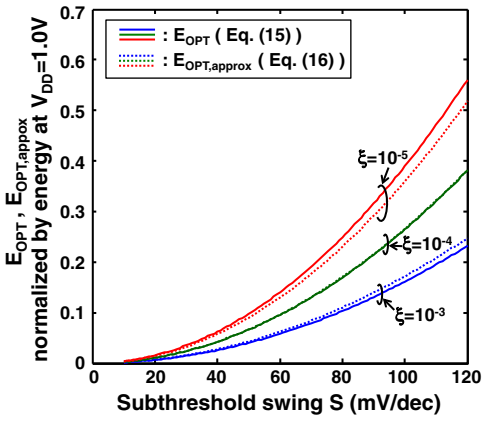

Fig. 10. (Color online) E_{OPT} obtained by Eq. (15) and its approximated value ($E_{OPT,approx}$) calculated by Eq. (16). $E_{OPT,approx}$ is a good approximation of E_{OPT}.

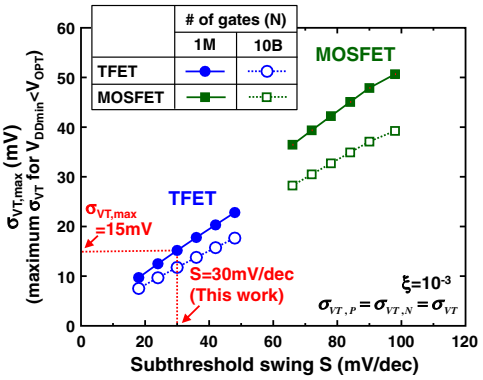

Fig. 11. (Color online) Dependence of $\sigma_{VT,max}$, which is the maximum σ_{VT} required for the correct operation at $V_{DD} = V_{OPT}$, on subthreshold swing S for logic circuits ($\xi = 10^{-3}$).

by 1/9 compared with MOSFET logic circuits if all the other parameters such as capacitances of TFET and MOSFET circuits (C_0) are identical.

V_{DDmin} could be an obstacle to achieve such energy reduction in TFET logic circuits. The rise in V_{DDmin} is caused by the increase in the within-die V_{TH} variation (σ_{VT}) as explained in Sect. 3, and hence we discuss here how small σ_{VT} should be controlled to achieve the minimum energy operation.

In order to achieve the minimum energy operation, circuits must be functional at V_{OPT}, that is, V_{DDmin} is less than V_{OPT} ($V_{DDmin} < V_{OPT}$). From Eqs. (8) and (13), σ_{VT} must satisfy the following condition:

$$\sigma_{VT} < \sigma_{VT,max} \propto \frac{S}{\sqrt{\ln N}}, \tag{17}$$

where $\sigma_{VT,max}$ is the maximum σ_{VT} required for the correct operation at $V_{DD} = V_{OPT}$. Figure 11 shows $\sigma_{VT,max}$ as a function of S for 1M and 10B gate logic circuits. In this figure, it is assumed that the strengths of pMOS and nMOS are perfectly balanced and η is 0.1 for MOSFET logic circuits. $\sigma_{VT,max}$ is proportional to S, as explained in Eq. (17), which means that V_{TH} variation (σ_{VT}) should be reduced as S becomes steeper. For 1M-gate logic circuits, σ_{VT} has to be controlled within 15 mV to achieve operation at V_{OPT} of 0.1 V. It should be noted that the methodology described here is applicable to the other TFET cases where S is different.

5. Conclusions

In this paper, the design guideline for the device engineers of the steep subthreshold swing (S) devices was presented. The energy of TFET logic circuits decreases as the supply voltage (V_{DD}) is reduced, and the energy becomes minimum at $V_{DD} = V_{OPT}$. Such reduction of V_{DD} is limited by the minimum operatable voltage (V_{DDmin}), because the logic gates with less than V_{DDmin} have functional errors. Therefore, in this paper, analytical equations of V_{DDmin} and the minimum energy (E_{OPT}) of TFET logic circuits at $V_{DD} = V_{OPT}$ were proposed. By using the proposed equations, it was clarified for the first time that V_{DDmin} is proportional to the standard deviation of the within-die threshold voltage variations (σ_{VT}), V_{OPT} is proportional to S, and E_{OPT} is proportional to the square of S. For example, when the conventional MOSFET's with S of 90 mV/dec are replaced with TFET's with S of 30 mV/dec and both σ_{VT} and V_{DD} of TFET are reduced to 1/3 of those of the conventional MOSFET, E_{OPT} of TFET is reduced to 1/9 of that of the conventional MOSFET, if all the other parameters are assumed to be the same between the conventional MOSFET and TFET. Therefore, we concluded that σ_{VT} of TFET's should be reduced in proportion to S.

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