Optimal Design to Maximize Efficiency of Single-Inductor Multiple-Output Buck Converters in Discontinuous Conduction Mode for IoT Applications

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***Abstract*—To clarify the design guide of single-inductor multiple-output (SIMO) buck converters in discontinuous conduction mode (DCM) targeted for small-size and low-power IoT applications, equations of optimal design parameters (transistor size, inductance, and switching frequency) to maximize the power conversion efficiency are derived for the first time. The analytical optimal designs are verified with SPICE simulations. The maximum efficiency of SIMO DCM buck converters is lower than that of conventional single-inductor single-output (SISO) DCM buck converters, because the power loss due to the energy distribution switches is added. The efficiency degradation is analytically explained for the first time.**

Keywords—buck converter; discontinuous conduction mode; single-inductor multiple-output

I. INTRODUCTION

In the applications of Internet of Things (IoT), tiny and energy efficient IoT nodes are required for physical data collection. The requirements for power-management ICs are the multiple output voltages, small output current (μA – mA), and small size. Figs. 1 (a) and 2 show a conventional single-inductor single-output (SISO) buck converter and a single-inductor multiple-output (SIMO) buck converter, respectively. Instead of the SISO buck converter in continuous conduction mode (CCM), the SIMO buck converter in discontinuous conduction mode (DCM) is an excellent candidate to meet the requirements for IoT, because the SIMO buck converter can provide multiple output voltages using only one inductor and DCM is better suited for the small output current. In DCM, the inductor current (I_L) is intermittently zero within each switching cycle as shown in Fig. 1 (b). The design guide to maximize the power conversion efficiency of SISO and SIMO DCM buck converters, however, is not reported, though that of the SISO CCM buck converter is reported in [1]. In addition, the efficiency degradation of the SIMO DCM buck converter over the SISO DCM buck converter is not theoretically clarified.

Therefore, in this paper, the optimal designs of transistor size, inductance, and switching frequency to maximize the power conversion efficiency of both SISO and SIMO DCM buck converters are proposed, and the analytical optimal designs are verified with SPICE simulations. Then, the maximum efficiency of SISO and SIMO DCM buck converters are compared and analyzed.

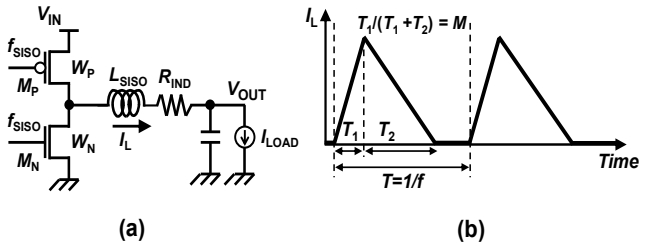

Fig. 1. Single-inductor single-output (SISO) buck converter. (a) Circuit. (b) Inductor current waveform in DCM.

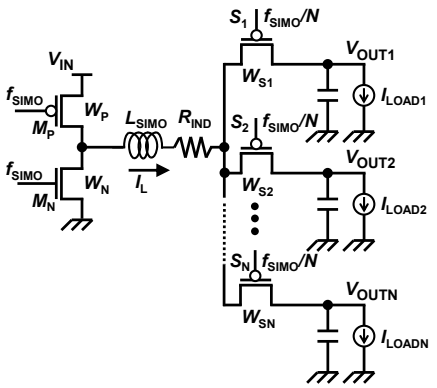

Fig. 2. Single-inductor multiple-output (SIMO) buck converter.

II. OPTIMAL DESIGN OF SISO DCM BUCK CONVERTER

To obtain the optimal design of the SISO DCM buck converter in Fig. 1 (a), the optimal design of the SISO CCM buck converter in [1] is expanded. In the section, equations (12) - (18) are newly proposed in this paper, while equations (1) - (11) are similar to [1]. The effective ON resistance (R_{EFF}) and effective switching capacitance (C_{EFF}) of the power transistors (M_P and M_N in Fig. 1 (a)) are as follows.

$$R_{EFF} = \frac{R_N}{W_N}(1-M) + \frac{R_P}{W_P}M \quad (1)$$

$$C_{EFF} = W_N C_N + W_P C_P \quad (2)$$

where W_N, W_P, R_N, R_P, and C_N, C_P are the gate widths, ON resistance per unit gate width, and the switched capacitance per unit gate width of nMOS (M_N) and pMOS (M_P), respectively. M (= V_{OUT}/V_{IN}) is the conversion ratio, where V_{IN}

and V_{OUT} are input and output voltages, respectively. By minimizing C_{EFF} at constant $R_{EFF,}$ the optimal gate width ratio ($\alpha_{OPT} = W_P/ W_N$) is determined as follows.

$$\alpha_{OPT} = \frac{W_P}{W_N} = \sqrt{\frac{MR_P C_N}{(1-M)R_N C_P}} \quad (3)$$

Here, the total gate width ($W_{TOTAL} = W_N + W_P$) is defined. By substituting (3) into (1) and (2), each of R_{EFF} and C_{EFF} is a function of W_{TOTAL} as follows.

$$R_{EFF} = \frac{R_{AVE}}{W_{TOTAL}} \quad (4)$$

$$R_{AVE} = (1+\alpha_{OPT})\left[(1-M)R_N + \frac{MR_P}{\alpha_{OPT}}\right] \quad (5)$$

$$C_{EFF} = W_{TOTAL} C_{AVE} \quad (6)$$

$$C_{AVE} = \frac{C_N + \alpha_{OPT} C_P}{1+\alpha_{OPT}} \quad (7)$$

The power loss ($P_{LOSS,SISO}$) in a buck converter consists of three kinds of loss: the switching loss ($P_{CAP,SISO}$), the resistive loss ($P_{RES,SISO}$) of M_N and M_P, and the resistive loss ($P_{IND,SISO}$) of the inductor [1].

$$P_{LOSS,SISO} = P_{CAP,SISO} + P_{RES,SISO} + P_{IND,SISO} \quad (8)$$

where

$$P_{CAP,SISO} = f_{SISO} C_{EFF} V_{IN}^2 = f_{SISO} W_{TOTAL} C_{AVE} V_{IN}^2 \quad (9)$$

$$P_{RES,SISO} = R_{EFF} I_{RMS,SISO}^2 = \frac{R_{AVE}}{W_{TOTAL}} I_{RMS,SISO}^2 \quad (10)$$

$$P_{IND,SISO} = R_{IND} I_{RMS,SISO}^2 = \frac{L_{SISO}}{\tau_L} I_{RMS,SISO}^2 \quad (11)$$

$$I_{RMS,SISO}^2 = \frac{2}{3} I_{LOAD} \sqrt{\frac{2V_{IN} M(1-M) I_{LOAD}}{f_{SISO} L_{SISO}}} \quad (12)$$

As shown in Fig. 1 (a), f_{SISO}, L_{SISO}, R_{IND}, I_{LOAD} are the switching frequency, the inductance, the parasitic resistance of the inductor, and the load current, respectively. τ_L is the figure of merit of an inductor technology [1-2] and $I_{RMS,SISO}$ is the effective value of I_L. The difference of this work from [1] is the discontinuous I_L shown in Fig. 1 (b) and (12).

In the design of the SISO DCM buck converter, three design parameters (W_{TOTAL}, L_{SISO}, f_{SISO}) are available. To maximize the power conversion efficiency, $P_{LOSS,SISO}$ should be minimized by setting the derivatives with respect to each parameter to zero [1]. Then the optimal parameters are derived as follows.

$$W_{TOTAL,OPT} = W_{SISO} \quad (13)$$

$$L_{SISO,OPT} = \frac{R_{AVE}\tau_L}{W_{SISO}} \quad (14)$$

$$f_{SISO,OPT} = \frac{2I_{LOAD}}{W_{SISO} V_{IN}} \sqrt[3]{\frac{M(1-M)R_{AVE}}{9\tau_L C_{AVE}^2}} \quad (15)$$

W_{SISO} is an arbitrary parameter (total gate width). In the optimal design, $P_{CAP,SISO} = P_{RES,SISO} = P_{IND,SISO}$, and the minimum $P_{LOSS,SISO}$ ($P_{LOSS,SISO,MIN}$), a newly defined loss ratio ($LR_{SISO,MIN}$), and the maximum efficiency ($\eta_{SISO,MAX}$) are shown as follows.

$$P_{LOSS,SISO,MIN} = V_{IN} I_{LOAD} \sqrt[3]{\frac{24R_{AVE}C_{AVE}M(1-M)}{\tau_L}} \quad (16)$$

$$LR_{SISO,MIN} = \frac{P_{LOSS,SISO,MIN}}{P_{OUT}} = \sqrt[3]{\frac{24R_{AVE}C_{AVE}(1-M)}{\tau_L M^2}} \quad (17)$$

$$\eta_{SISO,MAX} = \frac{1}{1+\sqrt[3]{\frac{24R_{AVE}C_{AVE}(1-M)}{\tau_L M^2}}} \quad (18)$$

III. Optimal Design of SIMO DCM Buck Converter

In this section, the optimal design of the SIMO DCM buck converter with N outputs in Fig. 2 is derived. Then, the analytical optimal designs are verified with SPICE simulations. In this paper, the time-multiplexing control [3-4] shown in Fig. 3 is used for the SIMO DCM buck converter, because the cross regulation between outputs is very small.

A. Analysis of Optimal Design

To simplify the analysis and to understand the essence of the SIMO DCM buck converter, N outputs in Fig. 2 are assumed to be equal. Specifically, $V_{OUT1} = V_{OUT2} = \ldots = V_{OUTN} = V_{OUT}$, $I_{LOAD1} = I_{LOAD2} = \ldots = I_{LOADN} = I_{LOAD}$, and $W_{S1} = W_{S2} = \ldots = W_{SN} = W_S$. In this assumption, the circuit in Fig. 2 can be transformed to the circuit in Fig. 4. Compared to the circuit of the SISO DCM buck converter in Fig. 1 (a), an energy distribution switch (S) is added and the load current increases N times. The power loss ($P_{LOSS,SIMO}$) is represented as follows.

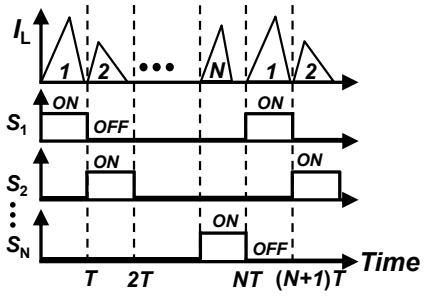

Fig. 3. Waveforms of SIMO DCM buck converter.

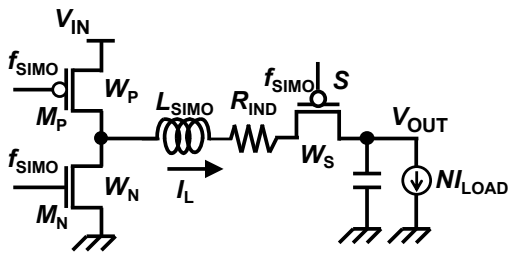

Fig. 4. Equivalent circuit of SIMO DCM buck converter with equal outputs.

$$P_{\mathrm{LOSS,SIMO}} = P_{\mathrm{CAP,SIMO}} + P_{\mathrm{RES,SIMO}} + P_{\mathrm{IND,SIMO}} \quad (19)$$

where

$$P_{\mathrm{CAP,SIMO}} = f_{\mathrm{SIMO}} W_{\mathrm{TOTAL}} C_{\mathrm{AVE}} {V_{\mathrm{IN}}}^2 + f_{\mathrm{SIMO}} W_{\mathrm{S}} C_{\mathrm{P}} {V_{\mathrm{IN}}}^2 \quad (20)$$

$$P_{\mathrm{RES,SIMO}} = \frac{R_{\mathrm{AVE}}}{W_{\mathrm{TOTAL}}} {I_{\mathrm{RMS,SIMO}}}^2 + \frac{R_{\mathrm{S}}}{W_{\mathrm{S}}} {I_{\mathrm{RMS,SIMO}}}^2 \quad (21)$$

$$P_{\mathrm{IND,SIMO}} = R_{\mathrm{IND}} {I_{\mathrm{RMS,SIMO}}}^2 = \frac{L_{\mathrm{SIMO}}}{\tau_{\mathrm{L}}} {I_{\mathrm{RMS,SIMO}}}^2 \quad (22)$$

$${I_{\mathrm{RMS,SIMO}}}^2 = \frac{2}{3}\left(NI_{\mathrm{LOAD}}\right)\sqrt{\frac{2V_{\mathrm{IN}}M\left(1-M\right)NI_{\mathrm{LOAD}}}{f_{\mathrm{SIMO}}L_{\mathrm{SIMO}}}} \quad (23)$$

$$R_{\mathrm{S}} = R_{\mathrm{P}}\frac{V_{\mathrm{IN}} - V_{\mathrm{TH}}}{MV_{\mathrm{IN}} - V_{\mathrm{TH}}} \quad (24)$$

W_{S} is the gate width of S, R_{S} is ON resistance of S per unit gate width, and V_{TH} is the threshold voltage of S. R_{S} instead of R_{P} is added, because the gate-source voltages of M_{P} and S are different in Fig. 4. In (20) and (21), the switching loss and resistive loss due to S are added. In the design of the SIMO DCM buck converter, four design parameters (W_{TOTAL}, W_{S}, L_{SIMO}, f_{SIMO}) are available. Compared with the previous section, W_{S} is newly added. The optimal design parameters are derived as follows.

$$W_{\mathrm{TOTAL,OPT}} = W_{\mathrm{SIMO}} \quad (25)$$

$$W_{\mathrm{S,OPT}} = \sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{AVE}}}{R_{\mathrm{AVE}}C_{\mathrm{P}}}}W_{\mathrm{SIMO}} \quad (26)$$

$$L_{\mathrm{SIMO,OPT}} = \frac{R_{\mathrm{AVE}}\tau_{\mathrm{L}}}{W_{\mathrm{SIMO}}}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right) \quad (27)$$

$$f_{\mathrm{SIMO,OPT}} = \frac{2NI_{\mathrm{LOAD}}}{V_{\mathrm{IN}}W_{\mathrm{SIMO}}}\sqrt[3]{\frac{M\left(1-M\right)}{9\tau_{\mathrm{L}}{C_{\mathrm{AVE}}}^2}}\Bigg/\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right) \quad (28)$$

W_{SIMO} is an arbitrary parameter (total gate width). In the optimal design, $P_{\mathrm{CAP,SIMO}} = P_{\mathrm{RES,SIMO}} = P_{\mathrm{IND,SIMO}}$, and the minimum $P_{\mathrm{LOSS,SIMO}}$ ($P_{\mathrm{LOSS,SIMO,MIN}}$), the loss ratio ($LR_{\mathrm{SIMO,MIN}}$), and the maximum efficiency ($\eta_{\mathrm{SIMO,MAX}}$) are shown as follows

$$P_{\mathrm{LOSS,SIMO,MIN}} = V_{\mathrm{IN}}\left(NI_{\mathrm{LOAD}}\right) \times \sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}M\left(1-M\right)}{\tau_{\mathrm{L}}}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2} \quad (29)$$

$$LR_{\mathrm{SIMO,MIN}} = \frac{P_{\mathrm{LOSS,SIMO,MIN}}}{P_{\mathrm{OUT}}} = \sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2} \quad (30)$$

$$\eta_{\mathrm{SIMO,MAX}} = \frac{1}{1+\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2}} \quad (31)$$

Table I summarizes the derived equations. Similar to the SISO DCM buck converter, the optimal design for SISO DCM buck converter has one degree of freedom (W_{SIMO}). When $R_{\mathrm{S}} = 0$, (27) – (31) are equal to (14) – (18), respectively, which is reasonable.

B. Verification with SPICE Simulations

To check the validity of the derived equations in this paper, the optimal design of a SIMO DCM buck converter with two outputs in Fig. 2 is performed using 1.8V, 180nm CMOS process and the analytically derived $P_{\mathrm{LOSS,SIMO}}$ is compared with SPICE simulations. Fig. 5 shows the calculated and SPICE simulated $P_{\mathrm{LOSS,SIMO}}$. In Figs. 5 (a) –(d), one of the four design parameters (W_{TOTAL}, W_{S}, L_{SIMO}, f_{SIMO}) are varied, respectively, and all the other parameters are optimum values shown in Table II. The calculated results are consistent with the SPICE simulated results, which shows the validity of the equations in this paper. The minimum $P_{\mathrm{LOSS,SIMO}}$ in each Figs. 5 (a) –(d) are identical, which is the evidence of the minimum loss (= maximum efficiency) design.

TABLE I SUMMARY OF EQUATIONS FOR BUCK CONVERTERS.

	[1]	This Work	
Operation mode	**CCM**	**DCM**	
Topology	**SISO**	**SISO**	**SIMO**
$W_{\mathrm{TOTAL,OPT}}$	$\frac{R_{\mathrm{AVE}}I_{\mathrm{LOAD}}}{V_{\mathrm{IN}}}\sqrt[3]{\frac{8\tau_{\mathrm{L}}}{3R_{\mathrm{AVE}}C_{\mathrm{AVE}}M\left(1-M\right)}}$	W_{SISO} (13)	W_{SIMO} (25)
L_{OPT}	$\frac{V_{\mathrm{IN}}}{2I_{\mathrm{LOAD}}}\sqrt[3]{3R_{\mathrm{AVE}}C_{\mathrm{AVE}}{\tau_{\mathrm{L}}}^2M\left(1-M\right)}$	$\frac{R_{\mathrm{AVE}}\tau_{\mathrm{L}}}{W_{\mathrm{SISO}}}$ (14)	$\frac{R_{\mathrm{AVE}}\tau_{\mathrm{L}}}{W_{\mathrm{SIMO}}}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)$ (27)
f_{OPT}	$\sqrt[3]{\frac{M^2\left(1-M\right)^2}{3R_{\mathrm{AVE}}C_{\mathrm{AVE}}{\tau_{\mathrm{L}}}^2}}$	$\frac{2I_{\mathrm{LOAD}}}{W_{\mathrm{SISO}}V_{\mathrm{IN}}}\sqrt[3]{\frac{M\left(1-M\right)R_{\mathrm{AVE}}}{9\tau_{\mathrm{L}}{C_{\mathrm{AVE}}}^2}}$ (15)	$\frac{2NI_{\mathrm{LOAD}}}{W_{\mathrm{SIMO}}V_{\mathrm{IN}}}\sqrt[3]{\frac{M\left(1-M\right)R_{\mathrm{AVE}}}{9\tau_{\mathrm{L}}{C_{\mathrm{AVE}}}^2}}\Bigg/\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)$ (28)
$W_{\mathrm{S,OPT}}$			$\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{AVE}}}{R_{\mathrm{AVE}}C_{\mathrm{P}}}}W_{\mathrm{SIMO}}$ (26)
$P_{\mathrm{LOSS,MIN}}$	$V_{\mathrm{IN}}I_{\mathrm{LOAD}}\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}M\left(1-M\right)}{\tau_{\mathrm{L}}}}$	$V_{\mathrm{IN}}I_{\mathrm{LOAD}}\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}M\left(1-M\right)}{\tau_{\mathrm{L}}}}$ (16)	$V_{\mathrm{IN}}\left(NI_{\mathrm{LOAD}}\right)\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}M\left(1-M\right)}{\tau_{\mathrm{L}}}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2}$ (29)
$\frac{P_{\mathrm{LOSS,MIN}}}{P_{\mathrm{OUT}}}$	$\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}}$	$\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}}$ (17)	$\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2}$ (30)
$\eta_{\mathrm{MAX}} = \frac{1}{1+\frac{P_{\mathrm{LOSS,MIN}}}{P_{\mathrm{OUT}}}}$	$\frac{1}{1+\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}}}$	$\frac{1}{1+\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}}}$ (18)	$\frac{1}{1+\sqrt[3]{\frac{24R_{\mathrm{AVE}}C_{\mathrm{AVE}}\left(1-M\right)}{\tau_{\mathrm{L}}M^2}\left(1+\sqrt{\frac{R_{\mathrm{S}}C_{\mathrm{P}}}{R_{\mathrm{AVE}}C_{\mathrm{AVE}}}}\right)^2}}$ (31)

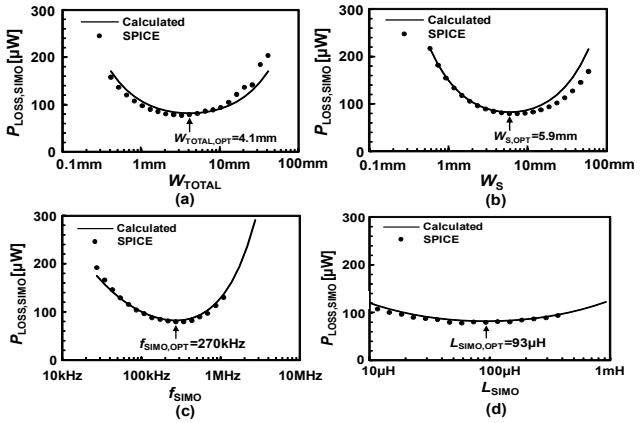

Fig. 5. Calculated and SPICE simulated $P_{LOSS,SIMO}$. In (a) –(d), one of four design parameters (W_{TOTAL}, W_S, L_{SIMO}, f_{SIMO}) are varied, respectively.

TABLE II PARAMETERS USED IN FIG. 5

M	0.5	τ_L	38 [μH/Ω]
V_{IN}	1.8 [V]	I_{LOAD}	1.0 [mA]
V_{OUT}	0.9 [V]	α_{OPT}	1.9
R_N	900 [Ω•μm]	$W_{TOTAL,OPT}$	4.1 [mm]
R_P	3600 [Ω•μm]	$W_{S,OPT}$	5.9 [mm]
C_N	2.8 [fF/μm]	$f_{SIMO,OPT}$	270 [kHz]
C_P	3.2 [fF/um]	$L_{SIMO,OPT}$	93 [μH]
R_S	8600 [Ω•μm]	$\sqrt{\frac{R_S C_P}{R_{AVE} C_{AVE}}}$	1.5
R_{AVE}	4000 [Ω•μm]	$\left(1+\sqrt{\frac{R_S C_P}{R_{AVE} C_{AVE}}}\right)^{\frac{2}{3}}$	1.8
C_{AVE}	3.0 [fF/μm]		

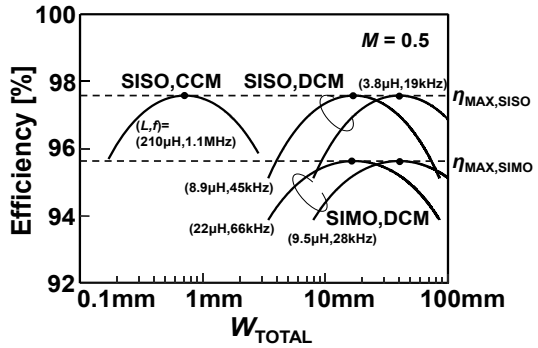

Fig. 6. Calculated W_{TOTAL} dependence of efficiency of SISO CCM, SISO DCM, and SIMO DCM buck converters.

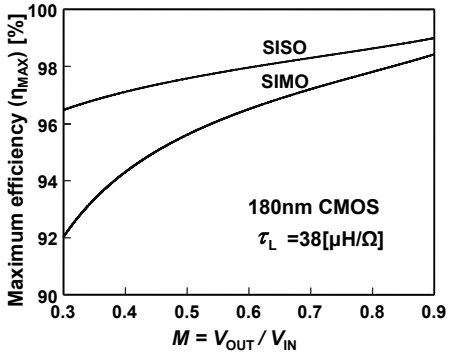

Fig. 7. Calculated M dependence of η_{MAX} of SISO and SIMO DCM buck converters.

IV. COMPARISON OF MAXIMUM EFFICIENCY OF SISO AND SIMO DCM BUCK CONVERTERS

Fig. 6 shows the calculated W_{TOTAL} dependence of the efficiency of SISO CCM, SISO DCM, and SIMO DCM buck converters. Parameters except W_{TOTAL}, L, and f are common as shown in Table II among the converters. In SISO CCM, the optimal W_{TOTAL} is uniquely determined, while the optimal W_{TOTAL} of SISO DCM and SIMO DCM has one degree of freedom. η_{MAX} of SISO CCM, however, is equal to η_{MAX} of SISO DCM as shown in Table I. η_{MAX} of SIMO DCM is lower than η_{MAX} of SISO DCM as shown in (18) and (31). Fig. 7 shows the calculated M dependence of η_{MAX} of SISO and SIMO DCM buck converters using (18) and (31). Parameters except M are similar to Table II. When M is increased from 0.3 to 0.9, the efficiency difference between SISO and SIMO decreases from 4.5% to 0.6%. Direct comparison of (18) and (31) results in a complicated equation, while comparison of (17) and (30) results in a simple equation as follows.

$$RLR = \frac{LR_{SIMO,MIN}}{LR_{SISO,MIN}} = \left(1+\sqrt{\frac{R_S C_P}{R_{AVE} C_{AVE}}}\right)^{\frac{2}{3}} \quad (32)$$

The ratio of the loss ratio (RLR) is a function of M and transistor-related parameters and does not depend on inductor-related parameters. The efficiency degradation between SISO and SIMO is universally explained by RLR. RLR is 2.4, 1.8, and 1.6 at M = 0.3, 0.5, and 0.9, respectively in 1.8V, 180-nm CMOS process. RLR decreases as M is increased, because S in Fig. 4 is pMOS and R_S decreases.

V. CONCLUSIONS

The design guides to maximize the power conversion efficiency of both SISO and SIMO DCM buck converters are proposed as shown in Table I. In the conventional SISO CCM buck converter, the optimal design parameters are uniquely determined, while the optimal design parameters in the SISO and SIMO DCM buck converters are not unique and have some flexibility. The maximum efficiency of the SIMO DCM buck converter is lower than that of the SISO DCM buck converter. The efficiency degradation mechanism is universally explained by the proposed RLR in (32).

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