A 39.25MHz 278dB-FOM 19μW LDO-Free Stacked-Amplifier Crystal Oscillator (SAXO) Operating at I/O Voltage

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The target of this work is to develop a low-power 39.25MHz crystal oscillator (XO) with low phase noise for RF applications and to achieve the highest FOM in XO’s. To reduce the supply current at a constant negative resistance (R\textsubscript{n}) in the XO, a stacked-amplifier crystal oscillator (SAXO) operating at I/O voltage is proposed, eliminating the need for a Low-Dropout Regulator (LDO). By stacking 4 amplifiers, the supply current is reduced by 91%. The developed 3.3V, 39.25MHz SAXO with 4-stacked amplifiers in 65nm CMOS consumes 19μW and has a phase noise of -139dB/Hz at 1kHz offset, thereby achieving a state-of-the-art FOM of 278dB.

Figure 5.7.1 (a) shows a conventional XO. The XO is often designed as an I/O cell and operates at I/O voltage (V\textsubscript{DD/O}) (e.g. 3.3V [1]), because the XO starts its operation first within an RF SoC. In contrast, the peak-to-peak oscillation amplitude (V\textsubscript{pp}) of the XO should be less than a certain voltage (e.g. 0.8V) determined by a drive level (e.g. 10pW) specified in a datasheet of quartz crystals. The operation beyond the specified drive level will lead to an inaccurate output frequency. Therefore, a large voltage difference between V\textsubscript{DD/O} and V\textsubscript{XO} (e.g. 3.3V - 0.8V = 2.5V) exists. As shown in Figure 5.7.1(a), in the conventional XO, the voltage difference is dropped across an LDO and a current source. Therefore, in this paper, we focus on the wasted LDO voltage drop and propose a new circuit topology effectively utilizing the voltage drop with the stacked amplifiers.

Figure 5.7.1(b) shows a proposed SAXO. Compared with Fig. 5.7.1(a), the CMOS inverter amplifier in Fig. 5.7.1(a) is replaced with N-stacked CMOS inverter amplifiers, and the LDO in Fig. 5.7.1(a) is removed. To enable the stacking, each amplifier includes two coupling capacitors (C\textsubscript{C1}, C\textsubscript{C2}) and two decoupling capacitors (C\textsubscript{D1}, C\textsubscript{D2}) as shown in Figure 5.7.1(b). The coupling capacitors in the lowest stage are removed to provide a common mode level in Out. Thus, the output frequency of the XO should be less than a certain voltage (e.g. 0.8V) determined by the drive level (e.g. 10pW) specified in a datasheet of quartz crystals. The operation beyond the specified drive level will lead to an inaccurate output frequency. Therefore, a large voltage difference between V\textsubscript{DD/O} and V\textsubscript{XO} (e.g. 3.3V - 0.8V = 2.5V) exists. As shown in Figure 5.7.1(a), in the conventional XO, the voltage difference is dropped across an LDO and a current source. Therefore, in this paper, we focus on the wasted LDO voltage drop and propose a new circuit topology effectively utilizing the voltage drop with the stacked amplifiers.

A drawback of the LDF for the phase noise reduction is slow start-up time (t\textsubscript{START-UP}) of the XO, because the RC time constant of the LDO with a cutoff frequency of 12Hz is 14ms, which is longer than a typical t\textsubscript{START-UP} of an XO (< 4ms). To reduce t\textsubscript{START-UP}, the LDO is disabled during the start-up. Figure 5.7.5 shows measured start-up waveforms enabling and disabling the LDF during the start-up in the proposed SAXO. As shown in Fig. 5.7.3(a), Amp\textsubscript{en} is an enable signal for both the constant-g\textsubscript{m} bias generator and the stacked-amplifiers, and LPF\textsubscript{en} is an enable signal for the LPF. In Fig. 5.7.5(a), both Amp\textsubscript{en} and LPF\textsubscript{en} are simultaneously turned on and t\textsubscript{START-UP} is 62ms. In contrast, in Fig. 5.7.5(b), t\textsubscript{START-UP} is 3.9ms, because the LDF is disabled during the start-up and the LDF is enabled after the start-up. The delayed turn-on of LPF\textsubscript{en} does not affect the waveform of Out. Thus, by disabling the LDF during the start-up, t\textsubscript{START-UP} is reduced from 62ms to 3.9ms, i.e. by 94%.

Figure 5.7.6 shows a comparison with previously published XO’s [2-5]. By stacking 4 amplifiers, the proposed 3.3V, 39.25MHz, 19μW LDO-free SAXO in 65nm CMOS consumes the lowest supply current of 5.8μA including that of 1.5μA in the constant-g\textsubscript{m} bias generator. The phase noise at 1kHz offset is -139dB/Hz, thereby achieving the highest FOM of 278dB. The measured frequency variation due to temperature variation is within ±7.7ppm from -30°C to 80°C at V\textsubscript{DD/O} = 3.3V. The measured frequency variation due to V\textsubscript{DD/O} variation is within 0.07ppm/V from 2.97V to 3.63V at 25°C. The measured supply-current variation due to temperature variation is within ±17% from -30°C to 80°C at V\textsubscript{DD/O} = 3.3V. The measured supply-current variation due to V\textsubscript{DD/O} variation is within 1% from 2.97V to 3.63V at 25°C.

Figure 5.7.7 shows a die micrograph of the proposed SAXO fabricated in 65nm CMOS. The core area is 8820μm² with a size of 420μm by 210μm.

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References:
Figure 5.7.1: (a) Conventional XO. (b) Proposed stacked-amplifier XO (SAXO).

Figure 5.7.2: Simulated $I_{DD}$ dependence of negative resistance ($R_N$) with various $N$.

Figure 5.7.3: (a) Circuit schematic of the SAXO. (b) & (c) Simulated $V_{DD(I/O)}$ dependence of $R_N$ variations without and with current source (CS).

Figure 5.7.4: Measured phase noise without and with the LPF in the SAXO.

Figure 5.7.5: Measured start-up waveforms in the SAXO. (a) Enabling LPF. (b) Disabling LPF during start-up.

Figure 5.7.6: Comparison with previously published XO’s [2-5].
Figure 5.7.7: Die micrograph of the SAXO fabricated in 65nm CMOS.