5.7 A 39.25MHz 278dB-FOM 19μW LDO-Free Stacked-Amplifier Crystal Oscillator (SAXO) Operating at I/O Voltage

Shunta Iguchi, Takayasu Sakurai, Makoto Takamiya

University of Tokyo, Tokyo, Japan

The target of this work is to develop a low-power 39.25MHz crystal oscillator (XO) with low phase noise for RF applications and to achieve the highest FOM in XO's. To reduce the supply current at a constant negative resistance (R_N) in the XO, a stacked-amplifier crystal oscillator (SAXO) operating at I/O voltage is proposed, eliminating the need for a Low-Dropout Regulator (LDO). By stacking 4 amplifiers, the supply current is reduced by 91%. The developed 3.3V, 39.25MHz SAXO with 4-stacked amplifiers in 65nm CMOS consumes 19μW and has a phase noise of -139dBc/Hz at 1kHz offset, thereby achieving a state-of-the-art FOM of 278dB.

Figure 5.7.1 (a) shows a conventional XO. The XO is often designed as an I/O cell and operates at I/O voltage ($V_{DD(I/O)}$) (e.g. 3.3V [1]), because the XO starts its operation first within an RF SoC. In contrast, the peak-to-peak oscillation amplitude (V_{XO}) of the XO should be less than a certain voltage (e.g. 0.8V) determined by a drive level (e.g. 10μW) specified in a datasheet of quartz crystals. The operation beyond the specified drive level will lead to an inaccurate output frequency. Therefore, a large voltage difference between $V_{DD(I/O)}$ and V_{XO} (e.g. 3.3V - 0.8V = 2.5V) exists. As shown in Fig. 5.7.1(a), in the conventional XO, the voltage difference is dropped across an LDO and a current source. Therefore, in this paper, we focus on the wasted LDO voltage drop and propose a new circuit topology effectively utilizing the voltage drop with the stacked amplifiers.

Figure 5.7.1(b) shows a proposed SAXO. Compared with Fig. 5.7.1(a), the CMOS inverter amplifier in Fig. 5.7.1(a) is replaced with N-stacked CMOS inverter amplifiers, and the LDO in Fig. 5.7.1(a) is removed. To enable the stacking, each amplifier includes two coupling capacitors (C_{C1}, C_{C2}) and two decoupling capacitors (C_{D1}, C_{D2}) as shown in Fig. 5.7.1(b). The coupling capacitors in the lowest stage are removed to provide a common mode level in Out. R_N of the XO is determined by $g_{m(TOTAL)}$ as shown in Fig. 5.7.1. To achieve the same R_N as the conventional XO in Fig. 5.7.1(a), g_m of each amplifier in the SAXO equals to g_{m0}/N. When the transistor size of each amplifier in Figs. 5.7.1(a) and (b) are the same and ideal MOSFET's in the saturation region are assumed, the gate overdrive (V_{GS} - V_{TH}) of the SAXO is 1/N of that of the conventional XO, and the supply current (I_{DD}) and the power consumption of the SAXO is $1/N^2$ of that of the conventional XO. In our implementation, N is 4 at $V_{DD(I/O)}$ = 3.3V considering the PVT variations, and $1/N^2$ equals to 1/16.

Figure 5.7.2 shows SPICE-simulated I_{DD} dependence of R_N with various N. R_N is proportional to N, because $g_{m(TOTAL)}$ is proportional to N. At the target R_N of 50Ω, I_{DD} of the proposed SAXO (N = 4) is reduced to 9% (= 1/11) of that of the conventional XO (N = 1).

Figure 5.7.3 (a) shows a detailed circuit schematic of the proposed LDO-free SAXO in 65nm CMOS. A start-up circuit for a constant-g_m bias generator is not shown in Fig. 5.7.3(a) for simplicity. Off-chip components are a 39.25MHz quartz crystal (DSX221G) and two capacitors (C_1, C_2) corresponding to the load capacitance of 8pF. Both 1.2V core transistors and 3.3V I/O transistors are used for the 3.3V operation, because the XO design using only I/O transistors increases the power consumption. On top of the stacked amplifiers, a current source (CS) (M_4) for a constant-g_m biasing is added to achieve robust operation to PVT variations, because the stacked amplifiers in the SAXO are sensitive to PVT variations due to the reduced gate overdrive. Figures 5.7.3(b) and (c) show SPICE-simulated $V_{DD(I/O)}$ dependence of R_N variations without and with the CS for 5 process corners at 25°C. Without the CS, the R_N variation is -24% to +6%. In contrast, with the CS, the R_N variation is reduced to -3% to +4% because the constant-g_m bias generator is a supply-voltage-insensitive current reference.

A drawback of the CS for the constant-g_m biasing is the degradation of the phase noise of the XO, because the flicker noise of transistors in the constant-g_m bias generator shown in Fig. 5.7.3 (a) modulates the power supply voltage of the stacked-amplifiers. To suppress the effect of the flicker noise, a lowpass filter (LPF) using an active resistor (M_3) and an amplified capacitor (C_{LPF}) using the Miller effect is added. The area-efficient LPF with M_3 and C_{LPF} achieves a cutoff frequency of 12Hz. The active resistor of 27MΩ with a size of 1800μm² is achieved with a multiplication of R_{BIAS} (= 80kΩ) by $(W/L)_{M1}$ / $(W/L)_{M3}$. 500pF is achieved with a multiplication of C_{LPF} (= 50pF) by the gain (≈ 10) of M_4. Figure 5.7.4 shows measured phase noise without and with the LPF in the proposed SAXO. By adding the LPF, the phase noise at 1kHz offset is reduced from -122dBc/Hz to -139dBc/Hz, which indicates 17dB noise reduction.

A drawback of the LPF for the phase noise reduction is slow start-up time ($t_{START-UP}$) of the XO, because the RC time constant of the LPF with a cutoff frequency of 12Hz is 14ms, which is longer than a typical $t_{START-UP}$ of an XO (< 4ms). To reduce $t_{START-UP}$, the LPF is disabled during the start-up. Figure 5.7.5 shows measured start-up waveforms enabling and disabling the LPF during the start-up in the proposed SAXO. As shown in Fig. 5.7.3(a), Amp_en is an enable signal for both the constant-g_m bias generator and the stacked-amplifiers, and LPF_en is an enable signal for the LPF. In Fig. 5.7.5(a), both Amp_en and LPF_en are simultaneously turned on and $t_{START-UP}$ is 62ms. In contrast, in Fig. 5.7.5(b), $t_{START-UP}$ is 3.9ms, because the LPF is disabled during the start-up and the LPF is enabled after the start-up. The delayed turn-on of LPF_en does not affect the waveform of Out. Thus, by disabling the LPF during the start-up, $t_{START-UP}$ is reduced from 62ms to 3.9ms, i. e. by 94%.

Figure 5.7.6 shows a comparison with previously published XO's [2-5]. By stacking 4 amplifiers, the proposed 3.3V, 39.25MHz, 19μW LDO-free SAXO in 65nm CMOS consumes the lowest supply current of 5.8μA including that of 1.5μA in the constant-g_m bias generator. The phase noise at 1kHz offset is -139dBc/Hz, thereby achieving the highest FOM of 278dB. The measured frequency variation due to temperature variation is within ±7.7ppm from -30°C to 80°C at $V_{DD(I/O)}$ = 3.3V. The measured frequency variation due to $V_{DD(I/O)}$ variation is within 0.07ppm/V from 2.97V to 3.63V at 25°C. The measured supply-current variation due to temperature variation is within ±17% from -30°C to 80°C at $V_{DD(I/O)}$ = 3.3V. The measured supply-current variation due to $V_{DD(I/O)}$ variation is within 7.1%/V from 2.97V to 3.63V at 25°C.

Figure 5.7.7 shows a die micrograph of the proposed SAXO fabricated in 65nm CMOS. The core area is 88200μm² with a size of 420μm by 210μm.

Acknowledgment:
The authors thank Yoshiaki Yoshihara, Yusuke Niki, and Ryuichi Fujimoto of Toshiba Corporation for technical discussions and Ren Shidachi of the University of Tokyo for measurement support. This work is partly supported by STARC. Shunta Iguchi is supported by JSPS through the Program for Leading Graduate Schools (MERIT).

References:

[1] Data sheet of TC35667, Toshiba, [Online].
[2] J. Lin, "A Low-Phase-Noise 0.004ppm/step DCXO with Guaranteed Monotonicity in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 418-419, Feb. 2005.
[3] Y. Chang, J. Leete, Z. Zhou, M. Vadipour, Y. Chang, and H. Darabi, "A Differential Digitally Controlled Crystal Oscillator with a 14-bit Tuning Resolution and Sine Wave Outputs for Cellular Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 421-434, Feb. 2012.
[4] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and M. Takamiya, "93% Power Reduction by Automatic Self Power Gating (ASPG) and Multistage Inverter for Negative Resistance (MINR) in 0.7V, 9.2μW, 39MHz Crystal Oscillator," *IEEE Symp. VLSI Circuits*, pp. C142-C143, June 2013.
[5] D. Griffith, J. Murdock, P. Røine, and T. Murphy, "A 37μW Dual-Mode Crystal Oscillator for Single-Crystal Radios," *ISSCC Dig. Tech. Papers*, pp. 104-105, Feb. 2015.
[6] D. Griffith, F. Dülger, G. Feygin, A. Mohieldin, and P. Vallur, "A 65nm CMOS DCXO System for Generating 38.4MHz and a Real Time Clock from a Single Crystal in 0.09mm²," *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 321-324, May 2010.

 978-1-4673-9467-3/16/$31.00

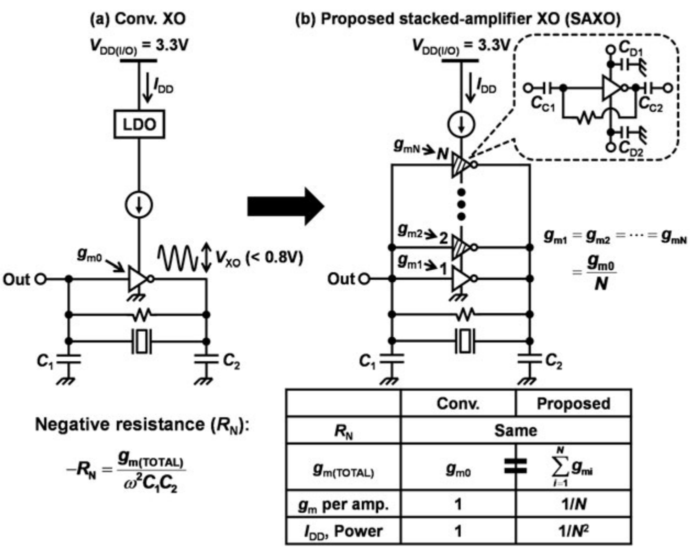

Figure 5.7.1: (a) Conventional XO. (b) Proposed stacked-amplifier XO (SAXO).

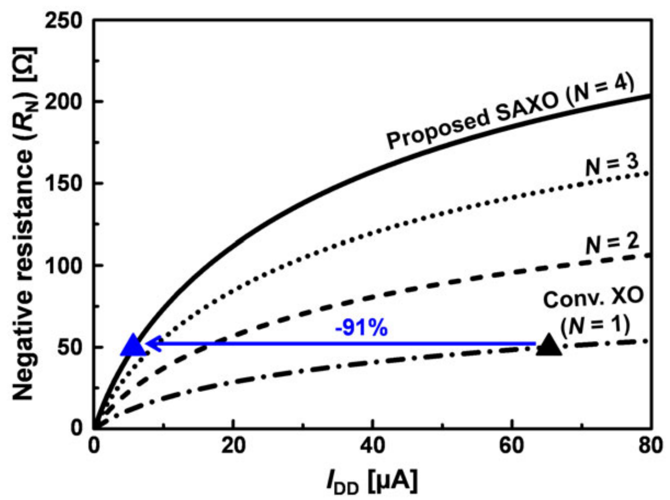

Figure 5.7.2: Simulated I_{DD} dependence of negative resistance (R_N) with various N.

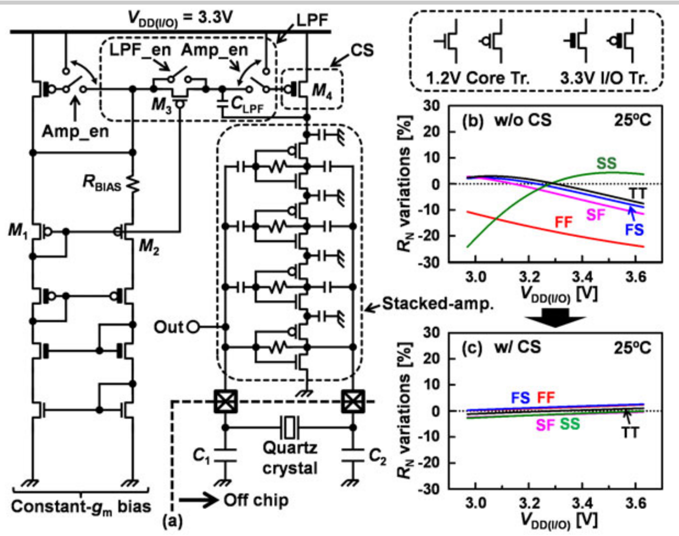

Figure 5.7.3: (a) Circuit schematic of the SAXO. (b) & (c) Simulated $V_{DD(I/O)}$ dependence of R_N variations without and with current source (CS).

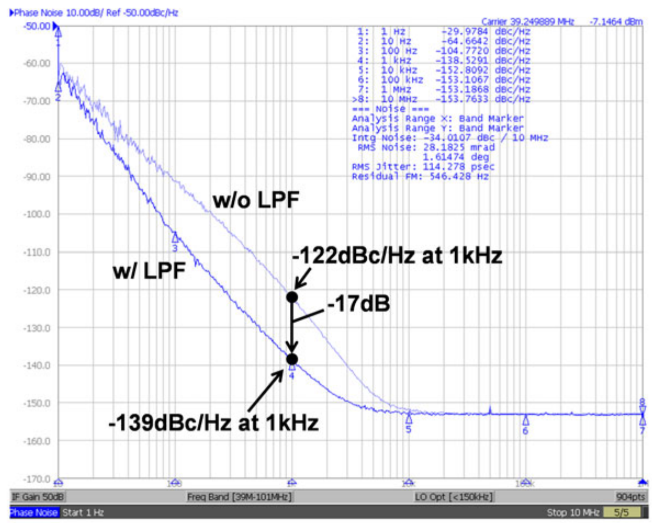

Figure 5.7.4: Measured phase noise without and with the LPF in the SAXO.

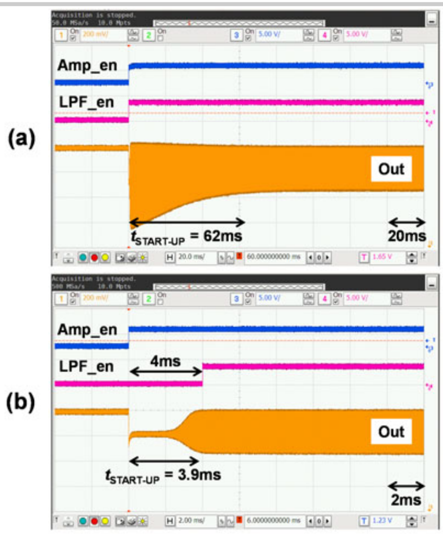

Figure 5.7.5: Measured start-up waveforms in the SAXO. (a) Enabling LPF. (b) Disabling LPF during start-up.

	[2]	[3]	[4]		[5]		This work
Frequency [MHz]	26	26	39.25		24		39.25
CMOS process [nm]	90	65	40		65		65
Supply voltage [V]	1.4	1.8	0.7		NA		3.3
Current [μA]	2143	1200	99	13	318(1)	26(1)	5.8
Power [μW]	3000	2160	69	9.2	445	37	19
Temp. range [°C]	-30 to 85	NA	NA		-40 to 90		-30 to 80
Frequency variation over temp. [ppm]	±7	NA	NA		±8	±13	±7.7
Frequency variation with voltage [ppm/V]	0.5	NA	25.1	120	6.9	9.0	0.07(2)
Phase noise @1kHz offset [dBc/Hz]	-140	-136	-120	-70	NA	NA	-139
FOM(3) [dB]	254	251	253	212	NA	NA	278
Die area [μm²]	180,000	150,000	60,500		130,000		88,200
Start-up time [ms]	2.5	3.2	0.259	NA	NA	NA	3.9

(1) Estimated with the supply voltage of 1.4V from [6] written by same author
(2) Supply voltage range of 2.97 to 3.63V
(3) FOM = (Oscillation frequency)² / (Power x Phase noise x (Offset frequency)²)

Figure 5.7.6: Comparison with previously published XO's [2-5].

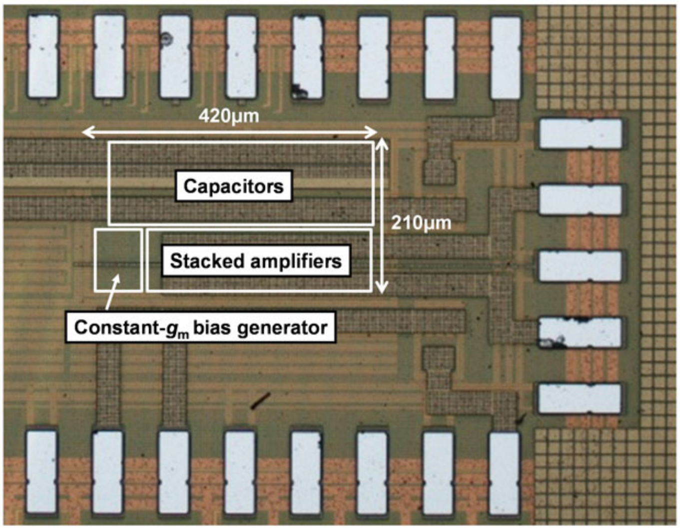

Figure 5.7.7: Die micrograph of the SAXO fabricated in 65nm CMOS.

978-1-4673-9467-3/16/$31.00