Variation-Tolerant Quick-Start-Up CMOS Crystal Oscillator With Chirp Injection and Negative Resistance Booster

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***Abstract*—This paper presents a variation-tolerant quick-start-up 39.25 MHz crystal oscillator and a theoretical analysis of a proposed chirp injector (CI) and negative resistance booster (NRB) for the quick start up. A new analysis of the theoretical minimum start-up time provides a new criterion for evaluating the start-up time in crystal oscillators. The calculated theoretical minimum start-up time at 39.25 MHz is $11.1\ \mu s$. A new analysis of the proposed CI and NRB clarifies the validity of the universal optimum control method. It explains the reason why the proposed CI and NRB reduce the start-up time and its variation. The proposed crystal oscillator with the proposed CI and NRB exhibits a start-up time of 158 μs at 39.25 MHz. The variation of the start-up time variations is $\pm 13\%$ over the supply voltage range of 1.2–1.8 V and $\pm 7\%$ over the temperature range of -30 to 125 °C. The power consumption of the crystal oscillator in the steady state is 181 μW with a phase noise of $-147\ \mathrm{dBc/Hz}$ at 1 kHz offset frequency, which corresponds to a figure of merit (FoM) of 276 dB.**

***Index Terms*—Chirp injection, crystal oscillator, negative resistance booster (NRB), quartz crystal, quick start up, variation tolerant.**

I. Introduction

FOR almost 100 years since their invention by Nicolson [1] and Cady [2] in the 1920s, crystal oscillators have been one of the key components in radio-frequency (RF) transceivers and digital circuits for generating an accurate and precise clock. RF transceivers should regulate the transmission frequency in accordance with wireless specifications (e.g., Bluetooth [3] and Wi-Fi [4]) because the adjacent-channel interference degrades the sensitivity of wireless receivers. For instance, the specifications of Bluetooth specify that the variation of the transmission frequency should be less than ± 75 kHz at a 2.4 GHz carrier frequency. The total frequency variation, including those of the reference clock generator, phase-lock-loop (PLL), and clock distribution circuits, has to be less than ± 31 ppm. It is difficult for on-chip CMOS oscillators to meet this requirement because the typical frequency variation caused by temperature fluctuations is more than $\pm 0.1\%$ ($= 1000$ ppm) [5], [6]. A study of a CMOS oscillator with on-chip heaters achieved ± 115 ppm frequency variation [7]; however, the large area of $1.04\ \mathrm{mm}^2$ and power consumption of 2.9 mW make it difficult to implement such an oscillator in a highly integrated system on chip (SoC). The frequency variation of crystal oscillators with an AT-cut quartz crystal is less than ± 100 ppm [8], [9], owing to the ultra-high Q factor ($>10,000$) of the quartz crystal. The stable and reliable characteristics of the quartz crystal have made crystal oscillators the *de facto* standard for reference clock generators in wireless communications.

Intermittent operation between the standby mode and the active mode in wireless transceivers is a key technique in reducing the power consumption because RF front-end circuits (e.g., power amplifiers and low-noise amplifiers) consume large amounts of power in the active mode. In the standby mode, the RF front-end circuits are disabled to reduce the power consumption. The crystal oscillator specifies the start-up time from the standby mode to the active mode because the start-up time of the crystal oscillator is the longest among the circuits in an RF SoC. The start-up times of the other circuit blocks such as the low dropout (LDO) [10], [11] and PLL[1] [12] are typically less than 10 μs. Most crystal oscillators with a frequency of 10 MHz order settle in 1–4 ms [13]–[18]. The slow start up of the crystal oscillator increases the system latency even when the start-up energy is not decreased by quick-start-up techniques.

To reduce the start-up time of crystal oscillators, several quick-start-up techniques [19]–[24] have been reported. It has been suggested that the start-up time would be greatly reduced from 4 ms to 50 μs by using a constant-frequency injector (CFI) [19]–[21] if the injection frequency accurately matched the resonant frequency (f_0) of the quartz crystal. A fine digital calibration [20] can be performed to calibrate the injection frequency; however, such a calibration requires an accurate and complex feedback loop including temperature sensors and voltage sensors. Additionally, some calibration techniques require a memory circuit to restore the calibration data. The power and area overheads are the drawbacks of the calibration techniques.

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[1]The settling time is about 100 times the period in the reference clock. The typical settling time is 2.5 μs (= 100 × 25 ns) for a 39.25 MHz reference clock.

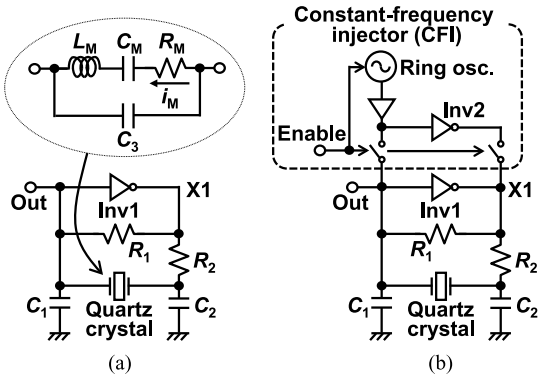

Fig. 1. Schematic of (a) Pierce crystal oscillator and (b) same oscillator with a conventional CFI.

The technique of automatic level control (ALC) [22] can reduce the start-up time to 300 μs because a bias current generator and amplitude detector can boost the negative resistance in the initial state. The reduction ratio of the start-up time is limited by the voltage headroom of the current sources in the feedback loop. In this technique, it is difficult to reduce the start-up time to more than four times less than the intrinsic start-up time of 1–4 ms. To achieve a stable and quick start up, even with fluctuations in the temperature and supply voltage, a crystal oscillator with a chirp injector (CI) [23] and a negative resistance booster (NRB) [24] was reported in 2014 [23]. This paper reports a new analysis of the theoretical minimum start-up time, which can be used to develop new criteria to evaluate the start-up time in crystal oscillators. Additionally, an analysis of the CI and NRB is used to derive a universal optimum control method for a variation-tolerant crystal oscillator with a CI and NRB.

II. Analysis of Theoretical Minimum Start-Up Time

To clarify the theoretical minimum start-up time in crystal oscillators, a theoretical analysis of the start-up time is given in this section. Analysis and discussion for a conventional CFI [19]–[21] are given because the CFI is a prospective mean of achieving the theoretical minimum start-up time, although it is difficult to integrate, owing to fluctuations in the temperature and supply voltage.

A. Start-Up Time in Pierce Crystal Oscillator

Pierce crystal oscillators [25], [26], can be used in many applications owing to their low power and low phase noise (PN). In other types of oscillator with single-pin structures [27], [28], the large parasitic capacitance in parallel with the quartz crystal increases the power and PN. Fig. 1(a) and (b) shows a schematic of a Pierce crystal oscillator and one with a CFI, respectively. $L_{\rm M}$, $C_{\rm M}$, and $R_{\rm M}$ are the motional inductor, capacitor, and resistor in the quartz crystal, respectively. C_1 is the gate-to-ground capacitor, C_2 is the drain-to-ground capacitor, C_3 is the parallel parasitic capacitor in the quartz crystal, R_1 is the feedback resistor, R_2 is the series resistor at the output of the inverter, Inv1 is the CMOS inverter used for steady-state operation, and $i_{\rm M}$ $(= |i_{\rm M}|\sin\omega t)$ is the current in the node containing $L_{\rm M}$, $C_{\rm M}$, and $R_{\rm M}$. According to theoretical studies [29], [30], the start-up time ($t_{\rm STARTUP}$) in a Pierce crystal oscillator is given by

$$t_{\rm STARTUP} = -\frac{2L_{\rm M}}{R_{\rm M} - |R_{\rm N}|} \ln\left(\frac{0.9\omega_{\rm OSC} C_{\rm T} V_{\rm DD}}{|i_{\rm M}(0)|}\right). \quad (1)$$

Assuming that $R_2 = 0$ for conciseness, where $\omega_{\rm OSC}$ is the oscillation angular frequency, $V_{\rm DD}$ is the supply voltage, $|i_{\rm M}(0)|$ is the amplitude of $i_{\rm M}$ in the initial state, and $R_{\rm N}$ and $C_{\rm T}$ are the negative resistance and load capacitance, respectively, given by

$$R_{\rm N} = -\frac{g_{\rm m} C_1 C_2}{(g_{\rm m} C_3)^2 + {\omega_{\rm OSC}}^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2} \quad (2)$$

$$C_{\rm T} = \frac{C_1 C_2}{C_1 + C_2} + C_3 \quad (3)$$

where $g_{\rm m}$ is the equivalent transconductance of the CMOS inverter. Equation (1) indicates that the start-up time is determined only by $|i_{\rm M}(0)|$ and $|R_{\rm N}|$ because the other parameters ($C_{\rm T}$, $L_{\rm M}$, $\omega_{\rm OSC}$, $R_{\rm M}$, and $V_{\rm DD}$) are determined by the target specifications and the quartz crystal.

In this study, the start-up time is defined as the time at which $|i_{\rm M}|$ reaches 0.9 times the amplitude in the steady state. Note that the oscillation amplitude and start-up time should be measured at the gate voltage because the gate voltage (Out) is proportional to $i_{\rm M}$. On the other hand, the drain voltage ($X1$) is not suitable for the measurement because the waveform is clipped and distorted by the nonlinearity of transistors. In this discussion of the definition of the start-up time, it is necessary to verify the consistency of the analysis and measurement results. A real-time measurement of the frequency error would be the most accurate way to define the start-up time; however, it failed to measure the small frequency deviation (< 100 ppm) during the start up even with a 40 GSa/s digital storage oscilloscope (Agilent DSO81204A) using the jitter analysis option owing to the resolution and noise of the oscilloscope. The real-time measurement of the frequency error is not available in the usual testing environment. Owing to this limitation, the oscillation amplitude is the only available and observable quantity for defining the start-up time of the crystal oscillator. Several studies [29]–[31] discussed the definition of the start-up time and defined it in terms of the oscillation amplitude. In [31], the start-up time is defined as the time at which $|i_{\rm M}|$ reaches 0.9 times the amplitude in the steady state for three reasons.

1) The threshold at 90% amplitude is used for the transition of the pulse in digital circuits and many items of measurement equipment support this threshold.
2) The drive level $(= |i_{\rm M}|^2 \times R_{\rm M}/2)$ in a quartz crystal at 90% amplitude is stable and satisfies a specified level in a datasheet.
3) The frequency error at 90% amplitude is negligibly small. A calculation in [31] gave a frequency error of 1.1 ppm at 90% amplitude.

Additionally, a simulation result for a quartz crystal at 39.25 MHz [32], as used in this study, shows that the frequency

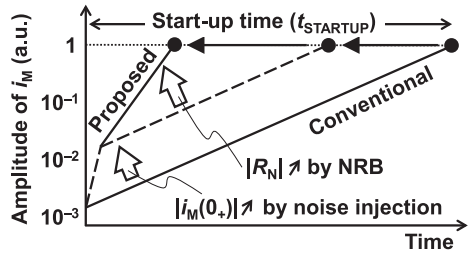

Fig. 2. Strategy to reduce the start-up time of a crystal oscillator by noise injection and the use of an NRB. Temporarily increasing $|i_{\rm M}(0_+)|$ and $|R_{\rm N}|$ reduces the start-up time.

error is within 10 ppm at 90% amplitude. The frequency error at 90% amplitude should be acceptable for a wireless specification [3]. In this paper, the threshold is defined as 90% amplitude for the above reasons.

Fig. 2 shows the strategy used to reduce the start-up time, assuming that the period of noise injection ($t_{\rm NOISE}$) is negligibly small. The values of $|i_{\rm M}(0_+)|$ and $|R_{\rm N}|$ correspond to the y-intercept ($\approx y$-value at $t = t_{\rm NOISE}$) and gradient of the lines in Fig. 2, respectively. To reduce the start-up time in this study, $|i_{\rm M}(0_+)|$ is first increased by noise injection, which shifts the line vertically upward. After that, $|R_{\rm N}|$ is increased by employing the NRB, which increases the gradient of the line.

B. Analysis of Theoretical Minimum Start-Up Time

Under the ideal condition without any variations, an ultrahigh-accurate CFI can achieve the theoretical minimum start-up time because the y-intercept in Fig. 2 is directly shifted to the steady-state amplitude by the CFI. On the other hand, the rate of the amplitude increase of $i_{\rm M}$ by time does not increase significantly when the NRB excessively boosts the negative resistance owing to the capacitance of C_3 in the quartz crystal; therefore, the NRB cannot achieve the theoretical minimum. The differential rectangular signals from the ring oscillator charge up the resonator in the quartz crystal, and $R_{\rm M}$ limits the minimum start-up time. The effect of R_2 is ignored for simplicity because the cutoff frequency (> 1 GHz) of the low-pass filter of R_2 and C_2 is sufficiently higher than the oscillation frequency. The transient of $i_{\rm M}$ is calculated by solving the differential equation

$$\frac{4V_{\rm DD}}{\pi}\sin\omega t = L_{\rm M}\frac{di_{\rm M}}{dt} + R_{\rm M}i_{\rm M} + \frac{1}{C_{\rm M}}\int i_{\rm M}dt. \quad (4)$$

Assuming that the harmonics of the rectangular signals are negligible. The differential rectangular signal is given as $4V_{\rm DD}/\pi$ from the Fourier series at the fundamental frequency.

At $\omega = \omega_0 \approx \omega_{\rm OSC}$, where ω_0 is the series resonant frequency of the quartz crystal. The transient of $|i_{\rm M}|$ is given by

$$|i_{\rm M}| = \frac{4V_{\rm DD}}{\pi R_{\rm M}}\left(1 - e^{-\frac{R_{\rm M}}{2L_{\rm M}}t}\right). \quad (5)$$

Equation (5) is calculated with the assumption of $i_{\rm M}(0) = 0$ for simplicity. In many cases, $i_{\rm M}(0)$ is negligibly small because $i_{\rm M}(0)$ is determined by the thermal noise in the circuit. In a Pierce crystal oscillator with a CMOS inverter, the amplitude of the gate-to-ground voltage ($|V_{\rm G}|$) in the steady state is approximately $V_{\rm DD}/2$. According to [33] and the definition of the start up, $|i_{\rm M}|$ at the start up ($|i_{\rm M}|_{\rm STARTUP}$) is given by

$$|i_{\rm M}|_{\rm STARTUP} = 0.45\omega_{\rm OSC}V_{\rm DD}\left(C_1 + 2C_3\right). \quad (6)$$

Assuming $C_1 = C_2$ for conciseness. By equating (5) and (6) as

$$\frac{4V_{\rm DD}}{\pi R_{\rm M}}\left(1 - e^{-\frac{R_{\rm M}}{2L_{\rm M}}t}\right) = 0.45\omega_{\rm OSC}V_{\rm DD}\left(C_1 + 2C_3\right). \quad (7)$$

The theoretical minimum start-up time ($t_{\rm STARTUP\_MIN}$) for a 39.25 MHz quartz crystal [32] is obtained as follows:

$$t_{\rm STARTUP\_MIN} \approx -\frac{2L_{\rm M}}{R_{\rm M}}\ln\left[1 - 0.35\omega_{\rm OSC}R_{\rm M}\left(C_1 + 2C_3\right)\right] = 11.1\ \mu{\rm s}. \quad (8)$$

The theoretical minimum start-up time of 11.1 μs is 14.2 times shorter than the shortest start-up time in a state-of-the-art oscillator [23]. This implies that the upcoming techniques could achieve a much shorter start-up time (e.g., less than 100 μs) in crystal oscillators with frequency of 10 MHz order. A CFI is not practical because the worst-case start-up time specifies the effective start-up time for the whole system. Both a short start-up time and small variations of the start-up time are important factors from the viewpoint of system design.

III. Chirp Injection and NRB

A. Overview of Crystal Oscillator With CI and NRB

Fig. 3(a) and (b) shows a schematic of a crystal oscillator with the proposed CI and one with the proposed CI and NRB, respectively. The CI consists of a chirp generator to generate a chirp-modulated signal that sweeps the frequency from a high frequency ($f_{\rm H}$) to a low frequency ($f_{\rm L}$). In the frequency range, the chirp-modulated signal is equivalent to a wide-band signal and is used to cover variations in the process, supply voltage, and temperature (PVT). The CI instantaneously charges up the resonator when the injection frequency matches the series resonant frequency of the resonator. The specifications (e.g., temperature range, reliability, and yield) of the system specify the sweep range between $f_{\rm H}$ and $f_{\rm L}$. In this study, $f_{\rm H}$ and $f_{\rm L}$ are determined to be $2f_{\rm OSC}$ and $0.5f_{\rm OSC}$ by simulation, respectively, where $f_{\rm OSC}$ is the oscillation frequency in the crystal oscillator. Fig. 4 shows a schematic of the chirp generator, which consists of a voltage-controlled oscillator (VCO) and a sweep circuit. The control voltage ($V_{\rm CNT}$), which is swept by a discharge circuit consisting of $C_{\rm CNT}$ and $R_{\rm CNT}$, controls the frequency of the VCO. When an enable trigger (CI_en) transits from a low state to a high state, $V_{\rm CNT}$ changes from $V_{\rm DD}$ to 0 V. The sweep speed and period ($t_{\rm CI}$) are controlled by the values of $C_{\rm CNT}$ and $R_{\rm CNT}$.

A digitally controlled NRB sets an auxiliary inverter (Inv3) at an appropriate gate width for the minimum start-up time. A control signal (NRB_en) controls the transient timing between the boost mode and the steady state. $|R_{\rm N}|$ temporarily increases with a large gate width during an enabled period ($t_{\rm NRB}$). Fig. 5

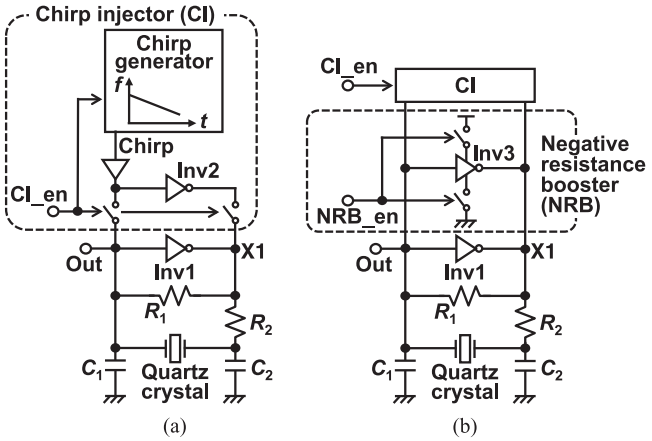

Fig. 3. Schematic of a crystal oscillator (a) with the proposed CI and (b) with the proposed CI and NRB.

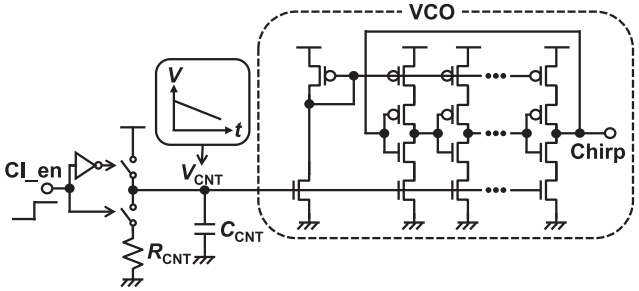

Fig. 4. Detailed schematic of the chirp generator consisting of a VCO and a sweep circuit.

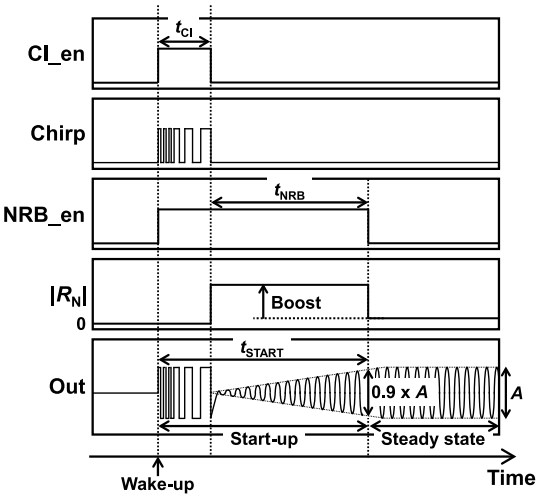

Fig. 5. Timing chart for the crystal oscillator with the proposed CI and NRB. The NRB boosts $|R_{\rm N}|$ during the period denoted by $t_{\rm NRB}$ because the transistors in Inv3 are in the linear region during the period denoted by $t_{\rm CI}$. In this study, the start-up time is determined as that when the oscillation amplitude reaches 0.9 times the peak-to-peak amplitude (A) in the steady state.

shows a timing chart for the crystal oscillator with the CI and NRB. First, a wake-up signal pulls up both CI_en and NRB_en. While CI_en is high, the signal at chirp excites Out and $X1$. After that, the NRB with Inv3 increases $|R_{\rm N}|$ during the period denoted by $t_{\rm NRB}$ in Fig. 5. Finally, the NRB disables the $|R_{\rm N}|$ boost when the oscillation amplitude in Out reaches

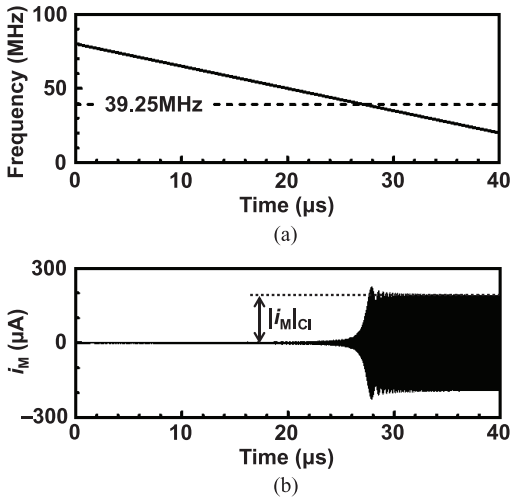

Fig. 6. Simulated time dependences of (a) frequency in the proposed CI and (b) $i_{\rm M}$.

90% of that in the steady state. By disabling the NRB during the steady-state operation, the power consumption and parasitic capacitance in the NRB can be negligible in the steady state.

A large $|i_{\rm M}(0)|$ and $|R_{\rm N}|$ reduce the start-up time as shown by (1). The proposed CI reduces the start-up time and its variation because the chirp-modulated signal instantaneously charges up the resonator at the target frequency of 39.25 MHz even in the case of fluctuations in the temperature and supply voltage. The new digitally controlled NRB also reduces the start-up time by providing an appropriate gate width to minimize the start-up time. Section III-B provides details of the control and theoretical analysis carried out to minimize the start-up time.

B. Analysis for the Optimum Control of CI and NRB

This section provides the analysis for the optimum control and capability of the CI and NRB with scaling of the operation frequency. First, the time-domain expression for a chirp-modulated signal is given by

$$f(t) = \sin\left(\omega_1 t + \frac{\omega_2 - \omega_1}{2T} t^2\right) \tag{9}$$

where ω_1, ω_2, and T are the starting angular frequency, the final angular frequency, and the time period in chirp modulation, respectively. Using (9), CI charges up the resonator in accordance with the differential equation

$$\frac{4V_{\rm DD}}{\pi} \sin\left(\omega_1 t + \frac{\omega_2 - \omega_1}{2t_{\rm CI}} t^2\right) = L_{\rm M}\frac{di_{\rm M}}{dt} + R_{\rm M} i_{\rm M} + \frac{1}{C_{\rm M}}\int i_{\rm M} dt. \tag{10}$$

Figure. 6(a) and (b), respectively, shows the simulated injection frequency and the transient of $i_{\rm M}$ corresponding to (10). The simulation result and (10) match when the driver in the CI can drive the load capacitors (C_1 and C_2) with rail-to-rail swing. If the drive strength is insufficient, the energy charged by the CI decreases owing to the small amplitude of the swing. In this work, the driver is designed with sufficient drive strength

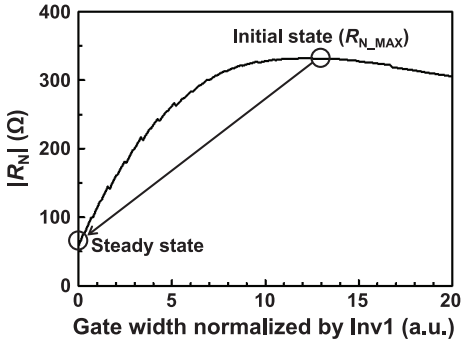

Fig. 7. Simulated gate width dependence of $|R_{\rm N}|$ normalized by the gate width of Inv1.

to drive a heavy capacitive load ($C_1 > 12$ pF). The amplitude of $i_{\rm M}$ rapidly increases when the injection frequency matches f_0. By solving (10) for $i_{\rm M}$ assuming that the Q factor (Q) of the quartz crystal is sufficiently larger than one, the final amplitude of $i_{\rm M}$ ($|i_{\rm M}|_{\rm CI}$) at $t = t_{\rm CI}$ is given by

$$|i_{\rm M}|_{\rm CI} = \frac{4V_{\rm DD}}{L_{\rm M}}\sqrt{\frac{t_{\rm CI}}{2\pi\,|\omega_2-\omega_1|}} = \frac{4\omega_0 C_{\rm M} V_{\rm DD}}{\sqrt{2\pi S}} \tag{11}$$

where $S = |\omega_2 - \omega_1|/\omega_0^2 t_{\rm CI}$, which is the slope factor normalized by ω_0. Equation (11) is derived in Appendix A. When the oscillation frequency is scaled with a fixed S, (11) indicates that $|i_{\rm M}|_{\rm CI}$ is proportional to ω_0 because $C_{\rm M}$ and $V_{\rm DD}$ do not vary with frequency scaling. Temperature-compensated oscillators should achieve a small S and a short start-up time because the sweep range in the CI is determined by the frequency variation of the VCO for noise injection. Additionally, the sweep direction ($\omega_{\rm H} \to \omega_{\rm L}$ or $\omega_{\rm L} \to \omega_{\rm H}$) does not affect $|i_{\rm M}|_{\rm CI}$ and the start-up time when Q is sufficiently larger than one.

Fig. 7 shows the gate width dependence of $|R_{\rm N}|$ normalized by the gate width of Inv1. The NRB configures the gate width of Inv3 to achieve a maximum $|R_{\rm N}|$ ($|R_{\rm N}|_{\rm MAX}$) in the interval $t_{\rm CI} < t < t_{\rm STARTUP}$. In the initial state, the optimum gate width takes a value of $|R_{\rm N}|_{\rm MAX}$ given by

$$|R_{\rm N}|_{\rm MAX} = \frac{r_{\rm O} C_1}{2C_3\left(1+\sqrt{1+\omega_0{}^2 r_{\rm O}{}^2 C_1{}^2}\right)} \tag{12}$$

where $r_{\rm O}$ is an equivalent output resistance in the NRB. Equation (12) is derived in Appendix B. When $r_{\rm O}$ is sufficiently large, (12) is approximated to

$$|R_{\rm N}|_{\rm MAX} \approx \frac{1}{2\omega_0 C_3}. \tag{13}$$

Equation (13) is a well-known expression for long-channel transistors introduced by [34]. To reduce the start-up time, careful PCB design and a layout to ensure a small C_3 are required because a large C_3 reduces $|R_{\rm N}|_{\rm MAX}$. Using (13), $|R_{\rm N}|_{\rm MAX}$, and $R_{\rm M} = 1/\omega_0 Q C_{\rm M}$, the time dependence of $|i_{\rm M}|$ ($|i_{\rm M}|_{\rm NRB}$) in the interval $t_{\rm CI} < t < t_{\rm STARTUP}$ is given and approximated by

$$|i_{\rm M}|_{\rm NRB} = |i_{\rm M}(0)|\, e^{-\frac{R_{\rm M}-|R_{\rm N}|_{\rm MAX}}{2L_{\rm M}}t} \approx |i_{\rm M}(0)|\, e^{\frac{1-2/Q}{4C_3/C_{\rm M}}\omega_0 t}. \tag{14}$$

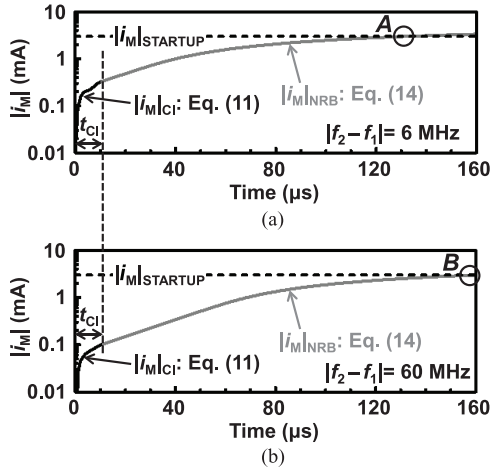

Fig. 8. Simulated time dependences of $|i_{\rm M}|$ with sweep ranges of (a) 6 MHz and (b) 60 MHz. The transients of $|i_{\rm M}|_{\rm CI}$ shown by a black line and $|i_{\rm M}|_{\rm NRB}$ shown by a gray line become tangents at a universal $t_{\rm CI}$. Points A and B denote the start-up times for $|f_2 - f_1|$ of 6 and 60 MHz, where f_1 and f_2 denote the starting frequency and final frequency, respectively. A small S with $|f_2 - f_1|$ of 6 MHz achieves a shorter start-up time than that with $|f_2 - f_1|$ of 60 MHz.

The detailed derivation of (14) by Laplace transformation is shown in [29] and involves considerable mathematical manipulation. On the other hand, (14) is easily derived from (5) with the substitution $R_{\rm M} \to R_{\rm M} - |R_{\rm N}|_{\rm MAX}$. The first term on the right-hand side of (5) is negligible because the first term, corresponding to the steady-state amplitude and amplitude saturation in linear circuit analysis, is about 100 times larger than $|i_{\rm M}|_{\rm STARTUP}$ in (6). During the start up of the crystal oscillator, the effect of the amplitude saturation expressed by the first term on the right-hand side of (5) is negligibly small. $|i_{\rm M}(0)|$ is the equivalent amplitude of $i_{\rm M}$ at $t = 0$ and is used for mathematical manipulation. Here, $|i_{\rm M}(0)|$ has no physical meaning because the initial value of $|i_{\rm M}|$ for the NRB is determined by the CI as shown by (11). Equation (14) indicates that $|i_{\rm M}|_{\rm NRB}$ is proportional to $\exp(\omega_0)$ in the case of frequency scaling because Q, C_3, and $C_{\rm M}$ are not scaled parameters.

The optimum $t_{\rm CI}$ ($t_{\rm CI\_OPT}$) for switching from the CI to the NRB is a tangent point between the two lines given by (11) and (14). By differentiating (11) and (14), $t_{\rm CI\_OPT}$ is given by

$$t_{\rm CI\_OPT} = -\frac{L_{\rm M}}{R_{\rm M}-|R_{\rm N}|_{\rm MAX}} \approx \frac{2C_3}{\omega_{\rm OSC} C_{\rm M}\,(1-2/Q)} \propto \frac{1}{\omega_{\rm OSC}}. \tag{15}$$

Assuming that $\omega_{\rm OSC} \approx \omega_0$. Equation (15) is derived in Appendix C. Using (15), S is expressed by

$$\begin{aligned} S &= C_{\rm M}\,|\omega_2-\omega_1|\,(|R_{\rm N}|_{\rm MAX} - R_{\rm M}) \\ &\approx \frac{|\omega_2-\omega_1|}{\omega_{\rm OSC}}\frac{C_{\rm M}\,(1-2/Q)}{2C_3}. \end{aligned} \tag{16}$$

Equation (16) implies that S is determined by the frequency error ($= |\omega_2 - \omega_1|/\omega_{\rm OSC}$) of the VCO due to PVT variations. Interestingly, $t_{\rm CI\_OPT}$ is a universal parameter for an arbitrary S. This indicates that circuit designers can specify $t_{\rm CI}$ for the CI regardless of the variation and sweep range of the VCO. Fig. 8(a) and (b) shows simulated time dependences of $|i_{\rm M}|$ with sweep ranges of 6 and 60 MHz, respectively. The transients of $|i_{\rm M}|$ switch from $|i_{\rm M}|_{\rm CI}$ to $|i_{\rm M}|_{\rm NRB}$ at a universal

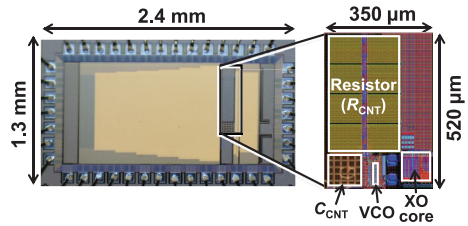

Fig. 9. Die micrograph and layout fabricated in 180 nm CMOS process.

$t_{\mathrm{CI\_OPT}}$ of 12.5 µs, corresponding to the tangent point, even with different sweep ranges. From (1), (11), (13), and (15), the start-up time ($t_{\mathrm{START\_OPT}}$) when using the CI and NRB is given by

$$t_{\mathrm{STARTUP\_OPT}} = t_{\mathrm{CI\_OPT}} \left[\ln \left(\frac{{C_{\mathrm{T}}}^2}{{C_{\mathrm{M}}}^2} S \right) - 0.15 \right] \propto \frac{1}{\omega_{\mathrm{OSC}}}. \quad (17)$$

Equation (17) is derived in Appendix D and verifies that $t_{\mathrm{START\_OPT}}$ does not depend on g_{m} in Inv1 and Inv3. The relative sweep range of the VCO (proportional to S) is the only variable parameter for the circuit designer at a target frequency. When an accurate oscillator (e.g., relaxation oscillator) for the CI is available, a small S can be used to minimize the start-up time because a small S increases $|i_{\mathrm{M}}|_{\mathrm{CI}}$. A comparison of the start-up time with different S is shown in Fig. 8. S in Fig. 8(a) is 10 times smaller than that in Fig. 8(b). The smaller S achieves a shorter start-up time because $|i_{\mathrm{M}}|_{\mathrm{CI}}$ is closer to the steady state ($\approx |i_{\mathrm{M}}|_{\mathrm{STARTUP}}$) than that with the larger S. Reducing S is the only way to reduce the start-up time from the viewpoint of circuit design; otherwise, a quartz crystal with small C_3 and C_{T} is required. Additionally, S (proportional to $|\omega_2 - \omega_1|/\omega_{\mathrm{OSC}}$) does not change significantly with PVT variations because the variation of the delay in the transistors changes ω_1, ω_2, and ω_{OSC} by the same ratio. The variations of R_{CNT} and C_{CNT} should also be considered. Assuming $\pm 40\%$ variations of the RC product (approximately inversely proportional to S), the variation of the start-up time calculated with (17) is less than $\pm 7\%$ because the variation of S is scaled down by $\ln(S)$. That is why the start-up time in the proposed crystal oscillator with the CI and NRB does not change significantly with PVT variations.

Finally, noted that the approximated expressions in (13)–(17) are effective for long-channel transistors. If short-channel transistors are used, the exact expressions should be adopted for circuit optimization. Additionally, $|R_{\mathrm{N}}|$ in the exact expressions should be estimated by simulation owing to the inaccuracy in the modeling of r_{O} [35].

IV. Measurement Results and Discussion

To demonstrate and verify the quick-start-up operation, the proposed crystal oscillator with the CI and NRB is implemented as shown in Fig. 3(b); additionally, the previous CFI shown in Fig. 1(b) is also implemented in the same die to evaluate the effects of the proposed CI and NRB. Fig. 9 shows the die micrograph and the layout, which was fabricated in a 180 nm CMOS process. Electrostatic discharge (ESD) is implemented with a body diode between the drain and well of the transistors. The transistor-based structure can be simulated by SPICE simulations without additional device simulations in technology computer-aided design (TCAD). The target oscillation frequency of the quartz crystal is 39.25 MHz with a load capacitance (C_{T}) of 8 pF [32]. The passive components (e.g., R_1, R_2, C_1, C_2, and the quartz crystal) are implemented on an FR4 PCB. To compensate the parasitic capacitors on the PCB, the values of C_1 and C_2 are carefully chosen. The test chip is directly mounted on the PCB with an electrically conductive epoxy. The bare chip and PCB are connected by bonding wires.

TABLE I
Design Parameters and Performance Summary

Oscillation frequency	39.25 MHz
CMOS process	180 nm
Supply voltage	1.5 V
Core area	0.12 mm^2
R_1, R_2, R_{M}	500 kΩ, 10 Ω, 10 Ω
C_1, C_2, C_3	12 pF, 12 pF, 2 pF
C_{M}, L_{M}	4.1039 fF, 4.0084 mH
Power consumption (P_{STEADY})	181 µW
Phase noise at 1 kHz	–147 dBc/Hz
Frequency variation (1.2 to 1.8 V) at 25 °C	±0.6 ppm
Frequency variation (–10 to 60 °C) at 1.5 V	±5.5 ppm
Start-up energy	349 nJ
Start-up time (t_{START}) at 1.5 V, 25 °C	158 µs
t_{START} variation (1.2 to 1.8 V) at 25 °C	±13%
t_{START} variation (–30 to 125 °C) at 1.5 V	±7%

Table I shows the design parameters and a summary of the performance of the proposed crystal oscillator. The start-up time and power consumption without the CI and NRB are 2.1 ms and 181 µW, respectively. These values are comparable to those in other works [13]–[18] without quick-start-up techniques. In the proposed crystal oscillator, 8 bit digitally controlled gate widths in Inv1 and Inv3 are used to configure the negative resistances in the steady-state and boost mode to obtain an oscillation allowance of more than five [36] and $R_{\mathrm{N\_MAX}}$, respectively. The series resistance (R_2) reduces the injection power into the quartz crystal and prevents overtone oscillation due to the parasitic inductors on the PCB.

The measured injection time dependence of the start-up time with the previous CFI is shown in Fig. 10. To verify the consistency of the analysis in Section II, an arbitrary function generator (Tektronix AFG 3251) accurately regulates the injection frequency within a variation of ±1 ppm. A tristate buffer in the CFI is used to vary the injection time within 0−15 µs. The minimum measured start-up time is 12.8 µs. This result verifies that the discussion on the theoretical minimum start-up time is valid.

Fig. 11 shows the measured injection frequency dependence of the start-up time with the previous CFI. The CFI injects a constant-frequency signal for an injection time of 40 µs.

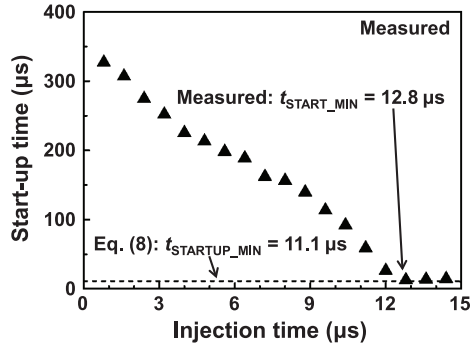

Fig. 10. Measured injection time dependence of the start-up time with the previous CFI. In this measurement, an arbitrary function generator (Tektronix AFG 3251) generates an accurate injection signal to achieve good matching between the injection frequency and the resonance frequency of the quartz crystal. The measurement result verifies that the theoretical analysis in Section II is valid.

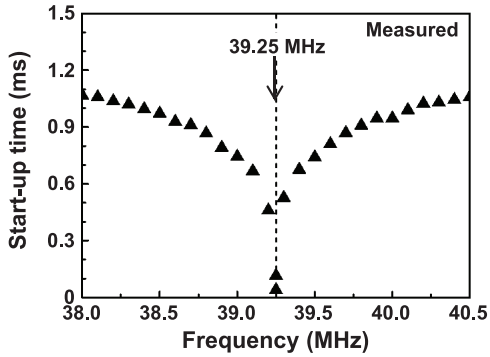

Fig. 11. Measured frequency dependence of the start-up time with the previous CFI. To input an accurate injection frequency for the quartz crystal, an arbitrary function generator (Tektronix AFG 3251) injects the injection signal for an injection time of 40 µs. The variation of the start-up time is caused by the frequency error of the ring oscillator.

The measured start-up time with the CFI varies within 40–1067 µs depending on the injection frequency, which varies in the range 38.0–40.5 MHz. The measured frequency variation of the embedded ring oscillator in the CFI is $\pm 9\%$ over the temperature range of -30 to 125 °C at the supply voltage of 1.5 V. The start-up time in the case of 0.1% variation varies within $40-500$ µs. A crystal oscillator [21] with 0.25% variation using a temperature-compensated RC oscillator achieves a shorter start-up time; however, this implies that a variation of 0.25% causes the start-up time to vary.

Measured time dependences of the chirp frequency in the chirp generator are shown in Fig. 12. To compensate the effect of the parasitic capacitances on the PCB, the target $t_{\rm CI}$ is set to 40 µs using (15). The design target of the initial frequency at a typical corner is 80 MHz. The chirp frequency crosses the oscillation frequency of the crystal oscillator over the best and worst corners in the test chip. The measured oscillation frequency in the VCO is 16% lower than the simulated frequency owing to model mismatches and process variations. This test chip matches the case of a slow transistor model in a process design kit (PDK). This verifies that the chirp frequency crosses 39.25 MHz even in the worst case ($= 1.35$ V, 125 °C, slow device).

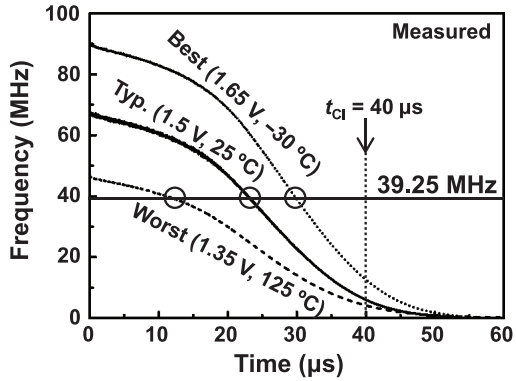

Fig. 12. Measured time dependences of the frequency in the proposed CI at three corners. All lines cross the target frequency of 39.25 MHz once before $t_{\rm CI} = 40$ µs.

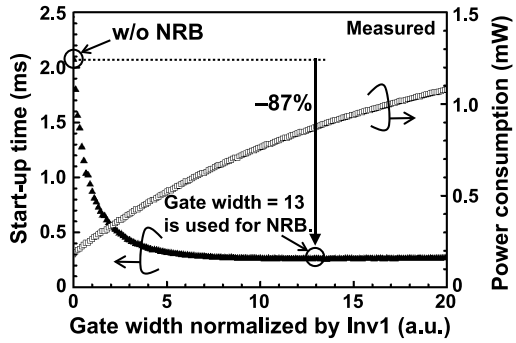

Fig. 13. Measured gate width dependences of the start-up time and the power consumption of the proposed NRB in the steady state with infinite $t_{\rm NRB}$. The gate width for the NRB is normalized by that of Inv1.

Fig. 13 shows the measured gate width dependences of the start-up time and the power consumption of the NRB in the steady state with a disabled CI and infinite $t_{\rm NRB}$. The gate width for the NRB is normalized by that of Inv1. With increasing the gate width, $|R_{\rm N}|$ increases and the start-up time decreases at the cost of increasing the power consumption. The NRB in the proposed crystal oscillator uses a normalized gate width of 13, corresponding to the maximum $|R_{\rm N}|$, which minimizes the start-up time because the aim of this study is to clarify the theoretical limitation of the start-up time with the CI and NRB. Additionally, the slow start-up time increases the system latency from the standby mode to the active mode in an RF SoC. If the start-up energy is the most important factor for the system, the optimum gate width will be smaller than the gate width used in this paper because the start-up time at a gate width of 5–10 is not significantly larger than the minimum start-up time. The optimum gate width should be determined from the total start-up energy and the latency in the whole system. In this case, the start-up time is reduced by 87%, while the power consumption increases by a factor of 4.9. In the measurements, the NRB is disabled at the time that the gate voltage at Inv1 reaches 0.9 times the amplitude in the steady state. A comparator or Schmitt trigger could be used to detect and disable the NRB depending on the oscillation amplitude. The optimum gate width is determined as the gate width corresponding to the maximum $|R_{\rm N}|$, which minimizes the start-up time of the crystal oscillator.

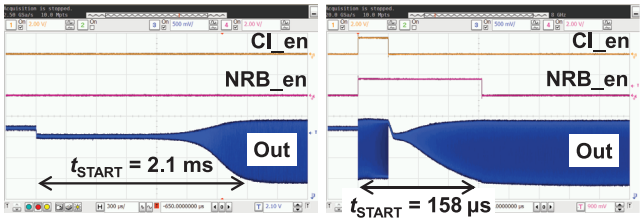

Fig. 14. Measured start-up waveforms for (a) conventional Pierce crystal oscillator in Fig. 1(a) and (b) proposed Pierce crystal oscillator with the CI and NRB in Fig. 3(b). The proposed CI and NRB reduce the start-up time from 2.1 ms to 158 µs at a temperature of 25 °C and supply voltage of 1.5 V.

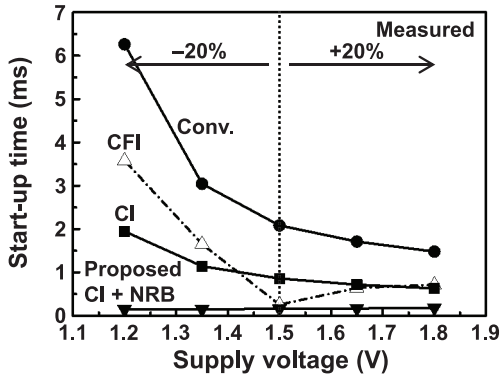

Fig. 15. Measured supply voltage dependences of the start-up time in four types of crystal oscillator. The start-up times without any quick-start-up technique, with the CFI, with the CI, and with the CI and NRB are compared.

The measured start-up waveform of the crystal oscillator without the CI and NRB is shown in Fig. 14(a). Fig. 14(b) shows the start-up waveform with the proposed CI and NRB. By combining the CI and NRB, the start-up time is reduced by 92% from 2.1 ms to 158 µs at a temperature of 25 °C and supply voltage of 1.5 V. Note that the proposed CI and NRB give an additional step response and frequency deviation when they are turned OFF. The frequency transient induced by the NRB is of most concern for the proposed crystal oscillator because the NRB is turned OFF last. The NRB varies the oscillation frequency because it uses a 13 times larger inverter than that for a steady state to increase the negative resistance. The parasitic capacitance in the NRB reduces the oscillation frequency to within 5 ppm. A frequency transient of within 5 ppm resulting from the step response of the disabled signal is acceptable for a wireless specification [3]. Additionally, no fluctuations or glitches due to the CI and NRB are observed in the transition from the boost mode to the steady state using a high-speed digital storage oscilloscope (Agilent DSO91294A). These results verify that the proposed technique can reduce the start-up time without introducing critical frequency deviations.

Fig. 15 shows measured supply voltage dependences of the start-up time in four types of crystal oscillator at a temperature of 25 °C. The supply voltage is varied by ±20% from the typical value of 1.5 V to evaluate the variation of the start-up time. The variation of the start-up time in the conventional CFI is much larger than that in the proposed CI because the calibrated frequency in the ring oscillator at the supply voltage of 1.5 V

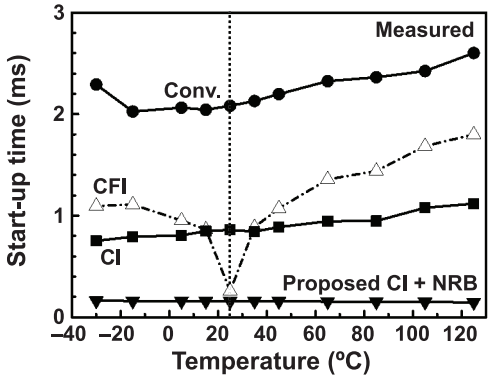

Fig. 16. Measured temperature dependences of the start-up time in the four types of crystal oscillator. The start-up times without any quick-start-up technique, with the CFI, with the CI, and with the CI and NRB are compared.

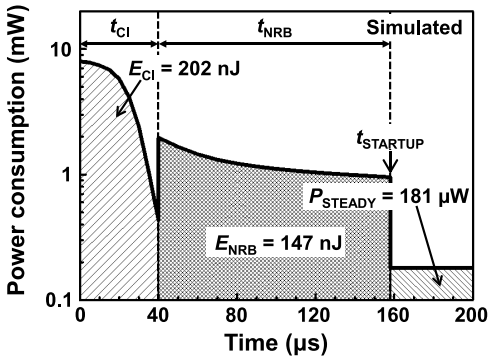

Fig. 17. Simulated start-up energy in the crystal oscillator with the proposed CI and NRB. E_{CI}, E_{NRB}, and P_{STEADY} are the start-up energy in the period denoted by t_{CI}, the start-up energy in the period denoted by t_{NRB}, and the power consumption in the steady state, respectively. The start-up energy is reduced from 380 to 349 nJ.

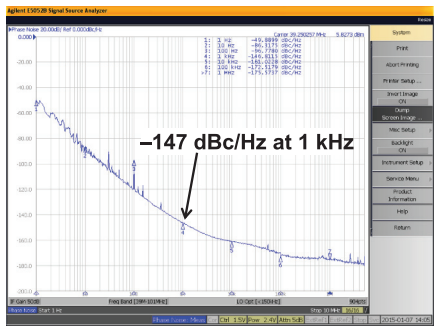

Fig. 18. Measured PN of the crystal oscillator in the steady state.

varies owing to the supply voltage variation. The CI is more variation tolerant than the CFI because the slope factor variation in the CI is smaller than that of the oscillation frequency. Additionally, the start-up time is reduced by the proposed NRB. In the crystal oscillator with the CI and NRB, the measured start-up times with ±20% supply voltage variation are within 145–179 µs, corresponding to a relative variation of ±13%.

Fig. 16 shows measured temperature dependences of the start-up time in the four types of crystal oscillator at a supply voltage of 1.5 V. The temperature is varied within −30 to 125 °C. The temperature dependences are similar to

TABLE II
COMPARISON WITH PREVIOUS WORKS

	[13]	[17]	[18]	[21]	[38]		This work [23]
Frequency (MHz)	26	38.4	26	24	39.25		39.25
Process (nm)	90	65	65	N/A	40		180
Supply voltage (V)	1.4	1.4	1.2	3.0	0.7		1.5
Core power (μW)	3000	4900	1440	N/A	69	9.2	181
Phase noise (dBc/Hz at1 kHz)	–140	–135	–136	N/A	–120	–70	–147
FoM (dB)	254	250	253	N/A	253	212	276
Start-up time (μs)	2500	1250	3200	150	259	N/A	158
PVT-variation-tolerant t_{START}	No	No	No	N/A	No	No	Yes

those in Fig. 15. The start-up times for temperatures in the range of -30 to $125\ ^{\circ}\mathrm{C}$ are 147–162 μs, corresponding to a relative variation of $\pm 7\%$.

The minimum start-up time is mainly limited by the frequency variation of the VCO and the nonlinearity of the transistors. The large frequency error of the VCO requires a broad sweep of $\omega_2 - \omega_1$ and a large S. Additionally, the nonlinearity of the transistors gradually reduces the negative resistance and the gradient of $|i_{\mathrm{M}}|_{\mathrm{NRB}}$ in Fig. 8. An increase in the start-up time of 60 μs caused by the nonlinearity would limit the minimum start-up time in this design.

The simulated start-up energy in the crystal oscillator with the CI and NRB is shown in Fig. 17. E_{CI}, E_{NRB}, and P_{STEADY} are the start-up energy in the period denoted by t_{CI}, the start-up energy in the period denoted by t_{NRB}, and the power consumption in the steady state, respectively. Note that E_{CI} and E_{NRB} are carefully calculated by block-level simulations because a full-blown circuit simulation with CI and NRB is not practical owing to the very long simulation period.[2]

Specifically, a transient simulation with both oscillator core and digital circuits requires an incredibly long period. This is one of the issues in crystal oscillator design even with state-of-the-art simulators [37]. On the other hand, the measurement of the start-up energy is also difficult because of the limited time resolution ($>100\,\mu\mathrm{s}$) for the current measurement with a dc power supply (ADCMT 6240A). The start-up energy with the CI and NRB is 349 nJ during the start-up time of $158\,\mu\mathrm{s}$, compared with 380 nJ during the start-up time of 2.1 ms without any quick-start-up technique. The proposed crystal oscillator has a smaller start-up energy than the crystal oscillator without the CI and NRB.

Fig. 18 shows the measured PN of the proposed crystal oscillator in the steady state. The measured PN at 1 kHz offset frequency is -147 dBc/Hz, comparable to that in previous works. A carefully designed PCB layout with a small C_3 is important to reduce the PN and power consumption. The measurement result verifies that the quick-start-up technique does not increase the PN because the CI and NRB are not active in the steady state.

[2]In many cases, a full-blown transient simulation for a crystal oscillator takes more than one week because the time step should be short for an ultrahigh-Q resonator.

A summary of the performance of the proposed crystal oscillator and a comparison with those in previous works [13], [17], [18], [21], [38] are shown in Tables I and II, respectively. The frequency variations resulting from fluctuations in the temperature and supply voltage are ± 5.5 and ± 0.6 ppm, respectively. These values satisfy the typical requirement of less than ± 31 ppm for a Bluetooth transceiver [3]. The crystal oscillator does not exceed the maximum drive level ($= 200\,\mu\mathrm{W}$) of a quartz crystal [32], defined as $|i_{\mathrm{M}}|^2 \times R_{\mathrm{M}}/2$, even with the NRB. The transient of $|i_{\mathrm{M}}|$ in Fig. 8 shows this consistency. The proposed crystal oscillator has a start-up time of 158 μs with a variation-tolerant design. The power consumption in the steady state is 181 μW with a PN of $-147\,\mathrm{dBc/Hz}$ at 1 kHz offset frequency (f_{OFFSET}). The corresponding figure of merit (FoM) [12] is 276 dB, where the FoM is defined as

$$\mathrm{FoM} = \frac{{f_{\mathrm{OSC}}}^2}{P_{\mathrm{STEADY}} \times \mathrm{PN} \times {f_{\mathrm{OFFSET}}}^2}. \tag{18}$$

V. CONCLUSION

A variation-tolerant quick-start-up 39.25 MHz crystal oscillator with a CI and NRB was presented. This is the first report of a variation-tolerant quick-start-up crystal oscillator. The proposed CI and NRB reduce the start-up time and its variation by using a variation-tolerant chirp-modulated signal and a maximum negative resistance. To clarify the theoretical limit of the start-up time in crystal oscillators, this paper presented a new analysis of the theoretical minimum start-up time and obtained a value of $11.1\,\mu\mathrm{s}$ for a 39.25 MHz quartz crystal. A discussion on the optimum control for the proposed CI and NRB gave the reason why the proposed CI and NRB reduce the start-up time and its variation by introducing a slope factor (S). The proposed universal optimum control method automatically specifies the circuit design, which depends on the quartz crystal and its frequency. The proposed crystal oscillator exhibits a start-up time of 158 μs at 39.25 MHz with a variation of $\pm 13\%$ over the supply voltage range of 1.2–1.8 V. The power consumption and PN at 1 kHz offset frequency are 181 μW and $-147\,\mathrm{dBc/Hz}$, respectively.

APPENDIX A
DERIVATION OF (11)

In this appendix, (11) is derived. Equation (11) is derived by solving the differential equation of (10). First, the left-hand side of (10) is transformed to

$$\begin{aligned} V &= \frac{4V_{\mathrm{DD}}}{\pi}\sin\left(\omega_1 t + \frac{\omega_2-\omega_1}{2t_{\mathrm{CI}}}t^2\right) \\ &= \frac{4V_{\mathrm{DD}}}{\pi}\sin\left({\omega'}_1 t' + \frac{{\omega'}_2-{\omega'}_1}{2{t'}_{\mathrm{CI}}}{t'}^2\right) \end{aligned} \tag{A1}$$

with the normalized expressions

$$t' = \frac{t}{\sqrt{L_{\mathrm{M}}C_{\mathrm{M}}}} \tag{A2}$$

$$\omega' = \omega\sqrt{L_{\mathrm{M}}C_{\mathrm{M}}} \tag{A3}$$

$${t'}_{\mathrm{CI}} = \frac{t_{\mathrm{CI}}}{\sqrt{L_{\mathrm{M}}C_{\mathrm{M}}}}. \tag{A4}$$

Equation (A1) is differentiated with respect to t' as

$$\frac{dV}{dt'} = \frac{4V_{\mathrm{DD}}}{\pi}\left({\omega'}_1 + \frac{{\omega'}_2-{\omega'}_1}{{t'}_{\mathrm{CI}}}t'\right)\cos\left({\omega'}_1 t' + \frac{{\omega'}_2-{\omega'}_1}{2{t'}_{\mathrm{CI}}}{t'}^2\right). \tag{A5}$$

The substitution of ${\omega'}_1 \to 0$ and ${\omega'}_2 \to {\omega'}_2 - {\omega'}_1$ simplifies (A5) to

$$\frac{dV}{dt'} = \frac{4V_{\mathrm{DD}}}{\pi}\left(\frac{{\omega'}_2-{\omega'}_1}{{t'}_{\mathrm{CI}}}t'\right)\cos\left(\frac{{\omega'}_2-{\omega'}_1}{2{t'}_{\mathrm{CI}}}{t'}^2\right) \tag{A6}$$

where a normalized slope factor (S) is defined as

$$S = \frac{\omega_2-\omega_1}{t_{\mathrm{CI}}} \times L_{\mathrm{M}}C_{\mathrm{M}} = \frac{{\omega'}_2-{\omega'}_1}{{t'}_{\mathrm{CI}}}. \tag{A7}$$

By introducing the slope factor into (A6), the derivative of the left-hand side of (10) becomes

$$\frac{dV}{dt'} = \frac{4V_{\mathrm{DD}}St'}{\pi}\cos\left(\frac{S}{2}{t'}^2\right). \tag{A8}$$

The derivative of the right-hand side of (10)

$$\frac{dV}{dt} = L_{\mathrm{M}}\frac{d^2i_{\mathrm{M}}}{dt^2} + R_{\mathrm{M}}\frac{di_{\mathrm{M}}}{dt} + \frac{i_{\mathrm{M}}}{C_{\mathrm{M}}} \tag{A9}$$

is transformed by (A2) to

$$\frac{d^2i_{\mathrm{M}}}{dt'^2} + R_{\mathrm{M}}\sqrt{\frac{C_{\mathrm{M}}}{L_{\mathrm{M}}}}\frac{di_{\mathrm{M}}}{dt'} + i_{\mathrm{M}} = \sqrt{\frac{C_{\mathrm{M}}}{L_{\mathrm{M}}}}\frac{dV}{dt'}. \tag{A10}$$

By substituting (A8) into (A10), (10) becomes

$$\frac{d^2i_{\mathrm{M}}}{dt'^2} + R_{\mathrm{M}}\sqrt{\frac{C_{\mathrm{M}}}{L_{\mathrm{M}}}}\frac{di_{\mathrm{M}}}{dt'} + i_{\mathrm{M}} = \sqrt{\frac{C_{\mathrm{M}}}{L_{\mathrm{M}}}}\frac{4V_{\mathrm{DD}}St'}{\pi}\cos\left(\frac{S}{2}{t'}^2\right). \tag{A11}$$

Equation (A11) is simplified to

$$\frac{d^2{i'}_{\mathrm{M}}}{dt'^2} + \frac{1}{Q}\frac{d{i'}_{\mathrm{M}}}{dt'} + {i'}_{\mathrm{M}} = St'\cos\left(\frac{S}{2}{t'}^2\right) \tag{A12}$$

with the normalized expression

$${i'}_{\mathrm{M}} = \frac{\pi}{4V_{\mathrm{DD}}}\sqrt{\frac{L_{\mathrm{M}}}{C_{\mathrm{M}}}}i_{\mathrm{M}}. \tag{A13}$$

When Q is sufficiently larger than one, (A12) is approximated to

$$\frac{d^2{i'}_{\mathrm{M}}}{dt'^2} + {i'}_{\mathrm{M}} \approx St'\cos\left(\frac{S}{2}{t'}^2\right). \tag{A14}$$

The normalized final amplitude ($|{i'}_{\mathrm{M}}|_{\mathrm{CI}}$) is calculated by solving (A14) with respect to t'. However, the complete expression for the solution of (A14) is too complex to describe here because it includes many Fresnel integrals. $|{i'}_{\mathrm{M}}|_{\mathrm{CI}}$ corresponding to the amplitude of the solution at infinite t' is given by

$$|{i'}_{\mathrm{M}}|_{\mathrm{CI}} = \sqrt{\frac{\pi}{2S}}. \tag{A15}$$

Finally, (11) is derived as

$$|i_{\mathrm{M}}|_{\mathrm{CI}} = \frac{4\omega_0 C_{\mathrm{M}}V_{\mathrm{DD}}}{\sqrt{2\pi S}} \tag{A16}$$

by substituting (A13) into (A15).

APPENDIX B
DERIVATION OF (12)

In this appendix, (12) is derived. When the effect of an equivalent output resistance (r_{O}) in the inverter is assumed, the negative resistance is given as

$$|R_{\mathrm{N}}| = \frac{{r_{\mathrm{O}}C_1}^2}{\frac{{C_1}^2(1+\omega_0{}^2{r_{\mathrm{O}}}^2{C_1}^2)}{g_{\mathrm{m}}r_{\mathrm{O}}-1} + 2C_1C_3 + {C_3}^2(g_{\mathrm{m}}r_{\mathrm{O}}-1)} \tag{B1}$$

with $C_1 = C_2$. Here, the function $f(g_{\mathrm{m}}) = |R_{\mathrm{N}}|$ is defined. The derivative of $f(g_{\mathrm{m}})$ with respect to g_{m} is equated to zero

$$f'(g_{\mathrm{m}}) = 0 \tag{B2}$$

to calculate the maximum value of $|R_{\mathrm{N}}|$. Then, the solution of (B2) corresponding to the optimum value of g_{m} ($g_{\mathrm{m\_OPT}}$) for the NRB is given by

$$g_{\mathrm{m\_OPT}} = \frac{C_3 + C_1\sqrt{1+\omega^2{r_{\mathrm{O}}}^2{C_1}^2}}{r_{\mathrm{O}}C_3}. \tag{B3}$$

By substituting (B3) into (B1), the maximum value of the negative resistance ($|R_{\mathrm{N}}|_{\mathrm{MAX}}$) is obtained as

$$|R_{\mathrm{N}}|_{\mathrm{MAX}} = \frac{r_{\mathrm{O}}C_1}{2C_3\left(1+\sqrt{1+\omega_0{}^2{r_{\mathrm{O}}}^2{C_1}^2}\right)}. \tag{B4}$$

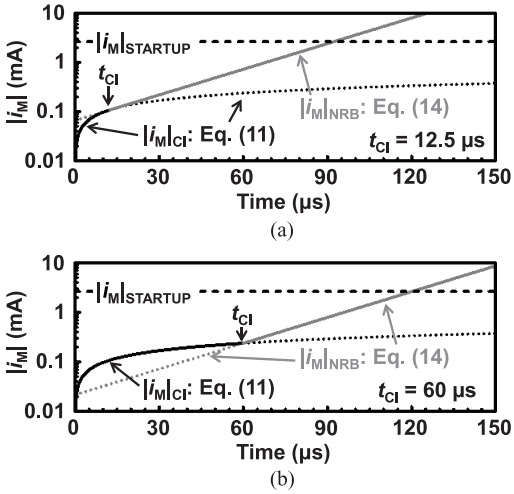

Fig. 19. Time dependences of $|i_{\rm M}|$ with $t_{\rm CI}$ of (a) 12.5 µs and (b) 60 µs calculated using (11) and (14) with $|f_2 - f_1| = 60$ MHz. The shortest start-up time is achieved at $t_{\rm CI}$ of 12.5 µs, corresponding to the tangent point of two lines.

Appendix C
Derivation of (15)

In this appendix, (15) is derived. First, it is verified that the optimum $t_{\rm CI}$ ($t_{\rm CI\_OPT}$) is determined at a tangent point between the two lines given by (11) and (14). Fig. 19(a) and (b) shows the time dependences of $|i_{\rm M}|$ with $t_{\rm CI}$ of 12.5 and 60 µs calculated using (11) and (14) with $|f_2 - f_1| = 60$ MHz. The calculated dependences verify that the start-up time is minimized at $t_{\rm CI}$ of 12.5 µs, corresponding to the tangent point because $|i_{\rm M}(0)|$ in (14) becomes the maximum value at $t_{\rm CI}$ of 12.5 µs. Note that (11) in Fig. 19 does not include the effect of the nonlinearity of the transistors and that the calculated start-up time is shorter than that in Fig. 8. The start-up time in Fig. 19(a) corresponds to that calculated by extrapolating $|i_{\rm M}|_{\rm NRB}$ in Fig. 8(b).

The tangent point is derived from (11) and (14) using this finding. To find the optimum $t_{\rm CI}$, $|i_{\rm M}(0)|$ is calculated by equating (11) and (14) as follows:

$$\frac{4V_{\rm DD}}{L_{\rm M}}\sqrt{\frac{t}{2\pi\left|\omega_2-\omega_1\right|}} = \left|i_{\rm M}\left(0\right)\right| e^{-\frac{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}{2L_{\rm M}}t} \tag{C1}$$

$$\left|i_{\rm M}\left(0\right)\right| = \frac{4V_{\rm DD}}{L_{\rm M}}\sqrt{\frac{t}{2\pi\left|\omega_2-\omega_1\right|}}e^{\frac{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}{2L_{\rm M}}t}. \tag{C2}$$

To derive the tangent point, the derivatives of (11) and (14) with respect to t are calculated as

$$\frac{d\left|i_{\rm M}\right|_{\rm CI}}{dt} = \frac{2V_{\rm DD}}{L_{\rm M}}\frac{1}{\sqrt{2\pi t\left|\omega_2-\omega_1\right|}} \tag{C3}$$

$$\frac{d\left|i_{\rm M}\right|_{\rm NRB}}{dt} = -\frac{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}{2L_{\rm M}}\left|i_{\rm M}\left(0\right)\right| e^{-\frac{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}{2L_{\rm M}}t}. \tag{C4}$$

Equation (C4) is simplified by substituting (C2) into (C4) to give

$$\frac{d\left|i_{\rm M}\right|_{\rm NRB}}{dt} = -\frac{2V_{\rm DD}}{{L_{\rm M}}^2}\left(R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}\right)\sqrt{\frac{t}{2\pi\left|\omega_2-\omega_1\right|}}. \tag{C5}$$

By equating (C3) and (C5), the optimum $t_{\rm CI}$ ($t_{\rm CI\_OPT}$) corresponding the tangent point between the two lines given by (11) and (14) is derived as

$$t_{\rm CI\_OPT} = -\frac{L_{\rm M}}{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}. \tag{C6}$$

Appendix D
Derivation of (17)

In this appendix, (17) is derived. Equations (11) and (14) are equated at $t = t_{\rm CI\_OPT}$ as

$$\frac{4\omega_0 C_{\rm M}V_{\rm DD}}{\sqrt{2\pi S}} = \left|i_{\rm M}\left(0\right)\right| e^{-\frac{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}{2L_{\rm M}}\left(-\frac{L_{\rm M}}{R_{\rm M}-\left|R_{\rm N}\right|_{\rm MAX}}\right)}. \tag{D1}$$

Then, $|i_{\rm M}(0)|$ is given by

$$\left|i_{\rm M}\left(0\right)\right| = \frac{4\omega_0 C_{\rm M}V_{\rm DD}}{\sqrt{2\pi eS}}. \tag{D2}$$

Substituting (D2) into (1) and using (15), the start-up time is derived as

$$\begin{aligned} t_{\rm STARTUP} &= -\frac{2L_{\rm M}}{R_{\rm M}-\left|R_{\rm N}\right|}\ln\left(\frac{0.9\omega_{\rm OSC}C_{\rm T}V_{\rm DD}}{\left|i_{\rm M}\left(0\right)\right|}\right) \\ &= 2t_{\rm CI\_OPT}\ln\left(\frac{0.9C_{\rm T}\sqrt{2\pi eS}}{4C_{\rm M}}\right) \\ &= t_{\rm CI\_OPT}\left[\ln\left(\frac{C_{\rm T}^2}{C_{\rm M}^2}S\right)+\ln\left(\frac{0.9^2\times 2\pi e}{4^2}\right)\right] \\ &\approx t_{\rm CI\_OPT}\left[\ln\left(\frac{C_{\rm T}^2}{C_{\rm M}^2}S\right)-0.15\right]. \end{aligned} \tag{D3}$$

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