20-ns Short-Circuit Detection Scheme with High Variation-Tolerance based on Analog Delay Multiplier Circuit for Advanced IGBTs

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***Abstract*— Advanced IGBTs need to be shut off when a short circuit occurs within less than 0.5-µs as the current density of IGBTs increases. In this paper, a circuit design and the measurement results are described for an IC chip which enables the short-circuit detection within 20-ns. The circuit detects the short-circuit condition by checking the existence of a plateau in a gate drive waveform. The proposed scheme can provide much higher variation-tolerance compared with the conventional scheme by introducing adaptive threshold-time determination. This adaptive feature is realized for the first time using a novel analog delay multiplier circuit. The chip was fabricated in 0.18-µm TSMC high-voltage CMOS technology. The measurements are carried out and the short-circuit detection operation is successfully verified even though the gate driving waveform slope is varied 10 times. The slope variation is cased possibly due to the variation of the gate drive current and/or the gate capacitance (C_{GE}+C_{GC}). Added to the benefits described above, it does not need any special off-chip component such as an IGBT with a Kelvin emitter, a parasitic inductor, and an inherently slow current monitor. Thus, it can be applicable to a wide range of power circuits with advanced IGBTs.**

Keywords—IGBT; short-circuit detection; analog delay multiplier;

I. Introduction

A short-circuit detector (SCD) for IGBTs whose typical configuration is shown in Fig. 1(a) has been pursued extensively but most of the proposals were slow and can't meet the need for the future advanced IGBTs which demands less than 0.5-µs detection delay. In the figure, VG is generated by dividing VGE using resistors and monitored by the SCD. A relatively fast SCD was previously reported based on the existence of a Miller plateau in a gate waveform when short-circuit does not occur, which achieved 1-µs detection delay [4]. The detection scheme is shown in Fig. 1(b). In this scheme, V_{REF}, above the Miller plateau voltage, V_{Miller}, is preset. The time when V_G crosses V_{REF}, is signified as t_{cross}. If t_{cross} is earlier than a certain preset threshold time, $t_{threshold}$, that is, tcross falls in the red Fail region, the short-circuit condition is met and the short-circuit flag, V_{SHORT}, is asserted. On the other hand, if t_{cross} falls in the green Safe region, V_{SHORT} is negated. This scheme works fine as far as there is no variability in the V_G slope.

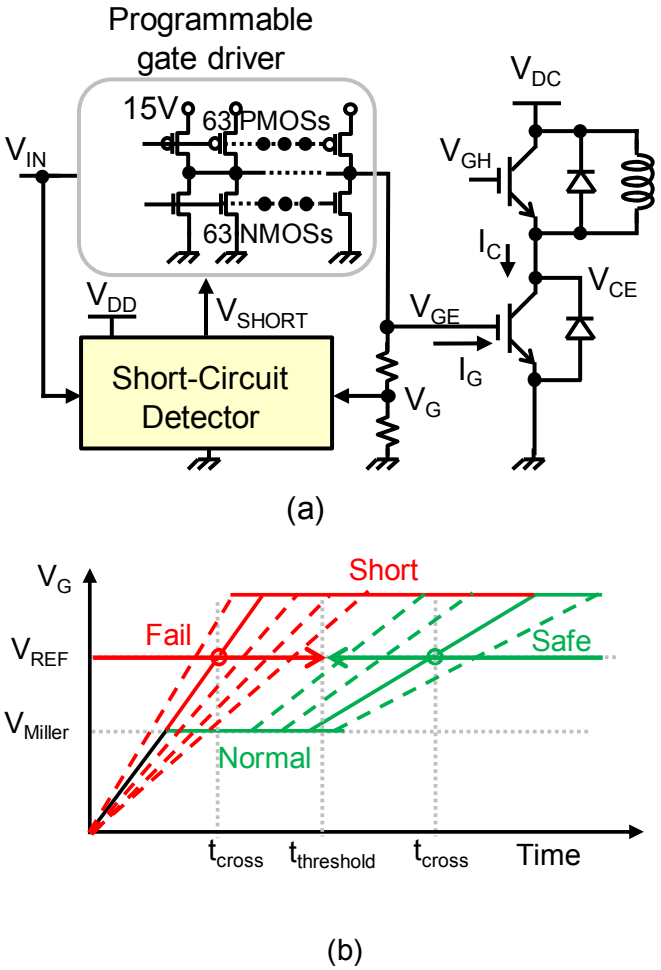

Fig. 1 (a) Example of short-circuit detector setup and (b) conventional short-circuit detection scheme

II. Proposed Variation-Tolerant Scheme

Suppose that there is a V_G slope variation as shown in Fig. 2(a) due to the IGBT gate capacitance variation and/or the gate turn-on current variation. If $t_{threshold}$ is preset as shown in

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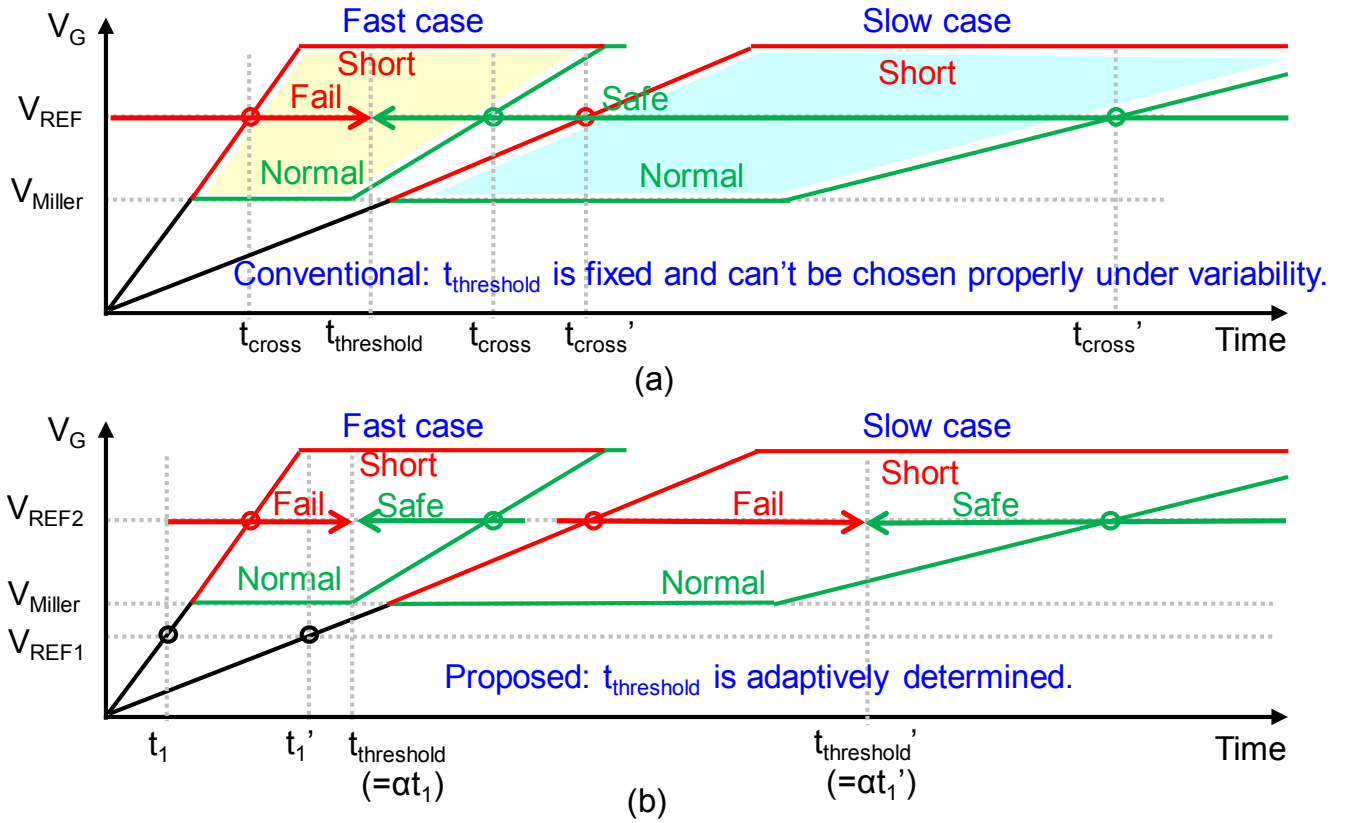

Fig. 2 (a) Conventional and (b) proposed SCD operation concept with V_G slope variation

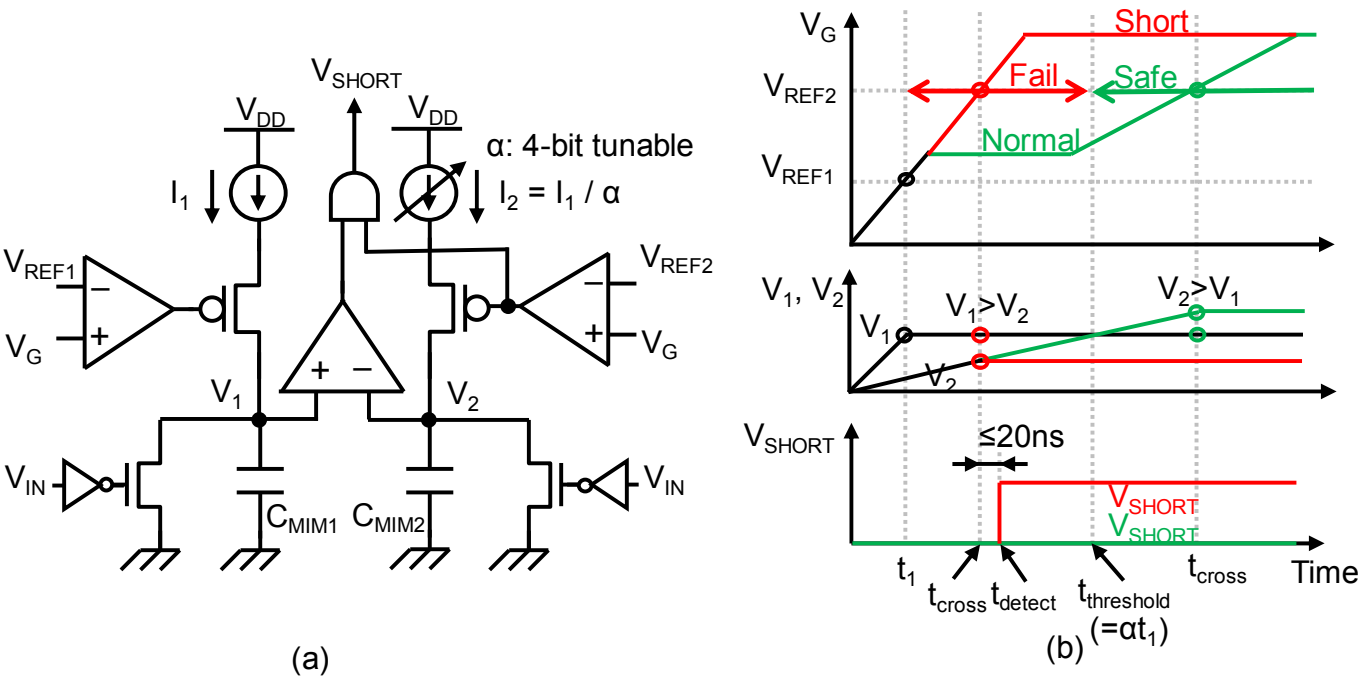

Fig. 3 (a) Circuit diagram of proposed scheme and (b) operation waveforms

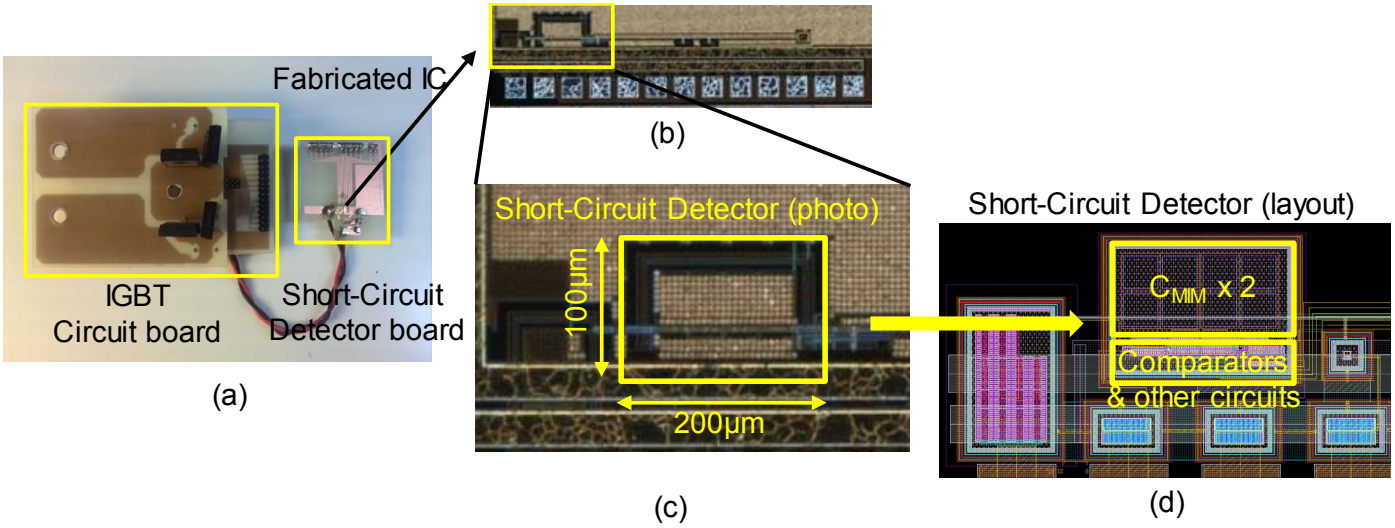

Fig. 4 (a) Test board, (b) chip with pad photo, (c) photo of chip main part and (d) layout of chip main part

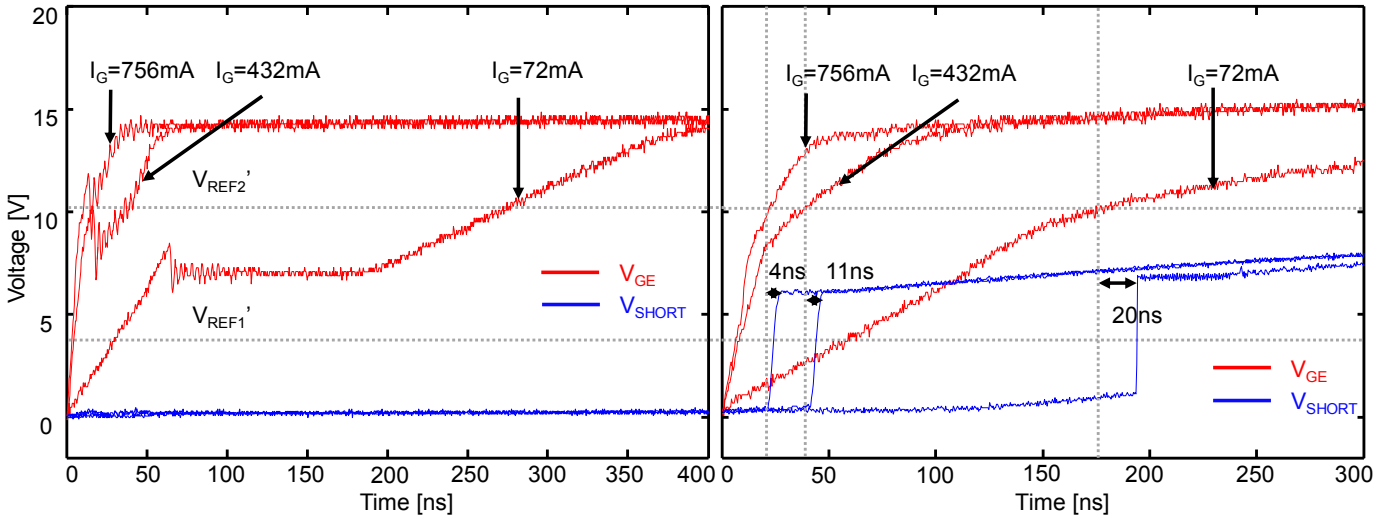

Fig. 5 Measured V_G and V_{SHORT} waveforms for (a) normal case and (b) short-circuit case

the figure, V_{SHORT} is always negated for the slow case since t_{cross}' always falls into the green Safe region. If $t_{threshold}$ is preset at much later time, it is proper for the slow case while it is unacceptable for the fast case. Since there is no overlap between the yellow region and the sky blue region, it is impossible to choose a proper $t_{threshold}$ in this conventional scheme. Even if the V_G slope variation is not that large, the conventional scheme suffers from small margins. In order to cope with this problem, $t_{threshold}$ is adaptively determined in the proposed scheme as is conceptually shown in Fig. 2(b). A certain voltage, V_{REF1}, is preset below V_{Miller}. The time when V_G crosses V_{REF1} is signified as t_1. $t_{threshold}$ is set as αt_1 where the multiplier α is digitally tunable from 1 to 16 using 4-bit control signals. When V_G is slow, t_1 is large and $t_{threshold}$ ($=\alpha t_1$) is also large. On the other hand, when V_G is fast, t_1 is small and $t_{threshold}$ ($=\alpha t_1$) is also small adaptively. In this way, $t_{threshold}$ is properly determined in a self-aligned manner even if the V_G slope has variability as shown in Fig. 2(b).

The circuit to realize the above-mentioned concept is shown in Fig. 3(a) together with the operation waveforms in Fig. 3(b). When V_{IN} turns on, the MIM capacitors, C_{MIM1} and C_{MIM2}, start to be charged by I_1 and I_1/α, respectively. C_{MIM1} stops to be charged when V_G crosses V_{REF1}, that is, at t_1. C_{MIM2} stops to be charged when V_G crosses V_{REF2}, that is, at t_{cross}. At t_{cross}, V_1 and V_2 are compared. If $V_1 > V_2$, V_{SHORT} is asserted. On the contrary, if $V_1 < V_2$, V_{SHORT} is negated. The threshold time corresponds to the condition that $V_1 = V_2$, and thus $t_{threshold}$ is calculated to be αt_1. In this way, the required adaptivity of $t_{threshold}$ is implemented. This novel analog delay multiplier circuit using two capacitors multiplies t_1 by α to generate $t_{threshold}$.

TABLE I: Comparison among Short-Circuit Detection Schemes

Reference	[1]	[2]	[3]	[4]	[5]	This work
Detection delay	2-μs	1.5-μs	3-μs	1-μs	50-ns	20-ns
Additional components	V_{CE} sensor	No	Kelvin emitter	No	Kelvin emitter	No
Variation tolerance	NA	NA	NA	NA	NA	>10x V_G slope (I_G: 72mA~756mA)

III. Measurement Results

The test board photo, the IC photo and the IC layout are shown in Fig. 4. A double pulse test circuit is built with Si IGBT (IRG7PH46UPbF) and SiC diode (C4D10120D) as depicted in Fig.1, which is driven by a programmable driver IC with 64-level current resolution and 40-ns minimum time step [6]. A single pulse test is employed for the short-circuit condition. Although only low side was measured here, the SCD is easily applied for the high side with proper high-voltage isolators. V_{DC} is set to 50V in order for the short-circuit current to be not so high. The fabricated chip is covered with dummy metal patterns and as a result, the circuit pattern is not clearly visible. Thus, layout of the circuit is also shown in Fig. 4(d).

Fig. 5 shows the measured waveforms without and with the short circuit. If there is no short circuit, the Miller plateau is present and V_{SHORT} is negated, while when a short circuit exists, V_{GE} and V_G are rising sharply without the Miller plateau and V_{SHORT} is asserted. The circuit successfully functions over wide range of I_G variation from 72mA through 756mA, which corresponds to more than 10 times the V_G slope variation. The maximum measured short-circuit detection delay is 20ns.

IV. Conclusions

A novel short-circuit detection scheme is proposed. The circuit is designed and fabricated using widely used high-voltage CMOS technology. The measurement shows 20-ns detection delay and 10 times V_G slope tolerance.

TABLE I shows the comparison of this work with other short-circuit detection schemes. It is seen from the table that the proposed circuit is demonstrated to provide the fastest and the most robust short-circuit detection scheme without additional off-chip components. Consequently, the scheme can be widely applicable to the power circuits with IGBTs for the future.

Acknowledgment

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