Automatic Optimization of IGBT Gate Driving Waveform Using Simulated Annealing for Programmable Gate Driver IC

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***Abstract*—Optimizing the gate driving waveform of power devices for energy loss and noise per switching has been attracting attention. This paper proposes a systematic method to automatically optimize the gate waveform by dynamically combining real measurements and software optimization loop based on simulated annealing algorithm. The method is applied to the turn-on and turn-off process of an IGBT double pulse test setup. A gate driving waveform with four time segments is employed for the optimization, which is realized by a help of a programmable gate driver IC. The machine-based optimization finishes within one and half hours and with the resultant optimized waveform, 59% energy loss decrease and 57% voltage overshoot reduction are achieved for the case of the IGBT turn-off compared with a simple single-step gate driving waveform.**

Keywords—IGBT; Gate driver; Automatic optimization; Simulated annealing; insert (key words)

I. INTRODUCTION

Gate driving waveform optimization of power devices for reducing energy loss without inducing large current or voltage overshoot has been attracting attention [1-9]. Recently for this purpose, a programmable gate driver IC has been developed [4], which enables to generate almost arbitrary waveforms for the gate voltage by changing the number of driving NMOSFETs and PMOSFETs at a certain time step. It can drive various power devices such as power MOSFETs, Si IGBTs and SiC MOSFETs. The optimization of the gate waveform, however, has to be conducted manually by human because of inaccurate IGBT simulation model and the parasitic components.Thus finding satisfactory waveforms takes days of time and the search space is very limited. Although the optimization strategies were presented in previous publications, the exact optimization depends on the board design, the systems design and the component parts, and thus quantitatively identifying the optimized waveform for a specific case still needs much effort. Moreover, as the freedom of the gate waveform control goes up, the optimization process is getting increasingly difficult. This paper reports an automatic optimization of the gate waveform by dynamically combining real measurements and software optimization loop to cope with the inherently time-consuming and costly optimization process.

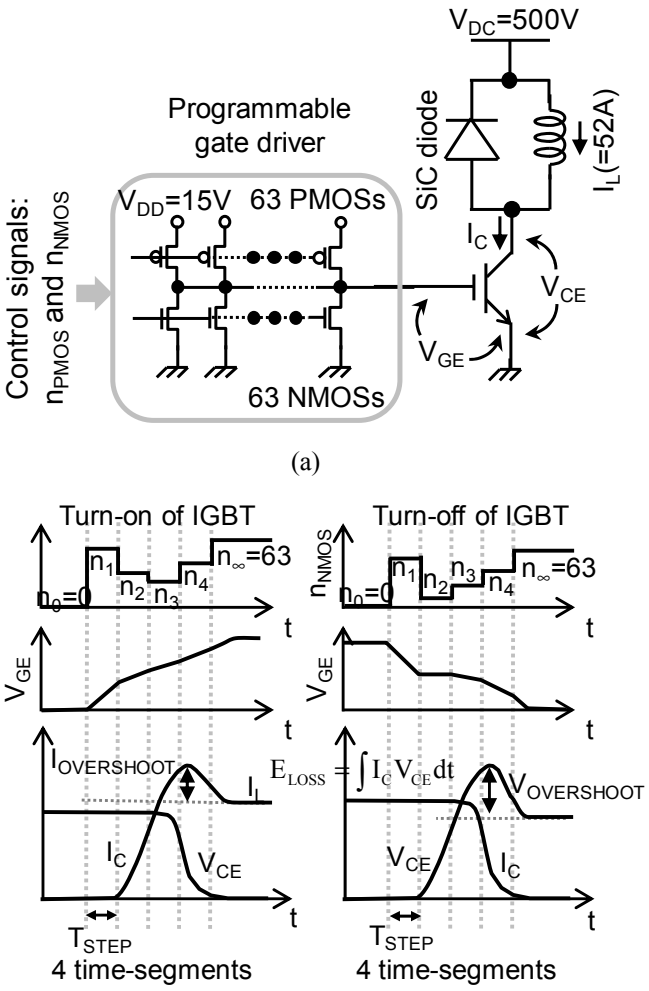

Fig. 1 (a) Circuit diagram and (b) waveform sketches used for IGBT gate driving waveform optimization

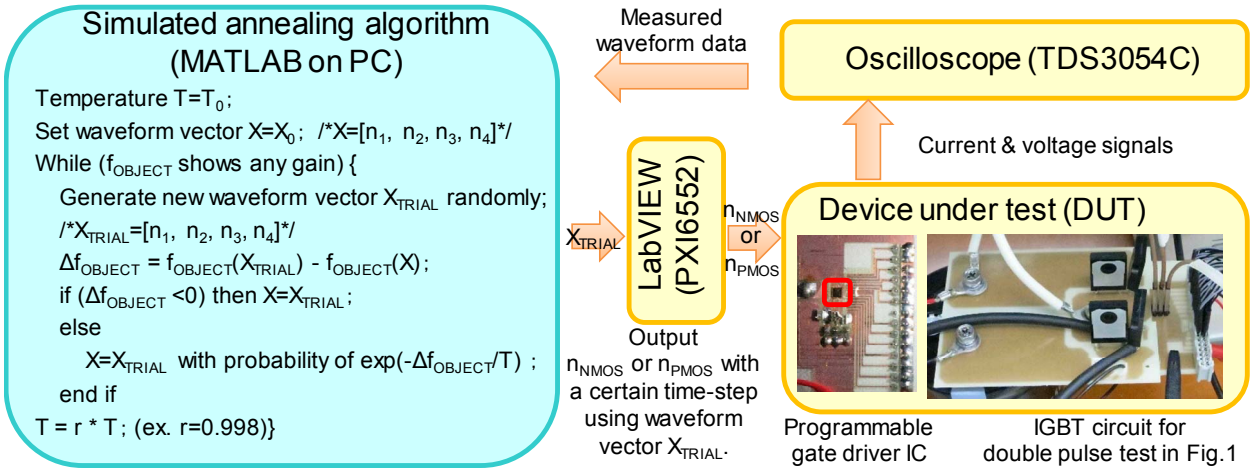

Fig. 2 System setup for automatic optimization (yellow part is hardware and blue part is software)

II. Optimization Method

This paper proposes the automation of the gate waveform optimization by using the simulated annealing (SA) algorithm [11] and a programmable gate driver IC [10]. The system setup used in this paper is shown in Fig.1. A 500-V double pulse test circuit is built using Si IGBT (IRG7PH46UPbF) and SiC diode (C4D10120D) with the load current of 52-A, which is driven +15V/0V gate voltage levels by a programmable driver IC with 64-level current resolution and 40-ns minimum time step [10]. The actual time step, T_{STEP}, used for the IGBT turn-on case whose time constant is mainly determined by the SiC diode is 80-ns and that for the IGBT turn-off case is 400-ns, which is determined by the Si IGBT itself. For both cases, the number of the time-segments is set to 4 in this paper as shown in Fig.1. After these segments, all PMOS or NMOS are on-state in order to avoid malfunction by reducing the gate impedance.

The programmable gate driver IC accepts a sequence of n_{PMOS} (the number of on-state PMOSs) and a sequence of n_{NMOS} (the number of on-state NMOSs) as the control inputs and changes the output drivability accordingly. Any strength of drivability from 0 to 63 (x 12-mA for both of PMOS and NMOS) can be chosen for each of the 4 time-segments, that is, n_1, n_2, n_3, and n_4 in Fig.1 can be any of integers from 0 to 63. Here, a set of the 4 integers [n_1, n_2, n_3, n_4] is called a waveform vector. Since the driver NMOS and PMOS are operated in a saturation region, an almost constant-current driving condition holds in driving the IGBT. Details of the gate driver IC are disclosed in [10].

In this waveform optimization process, 644 (~1.7e7) different waveforms need to be tried for an exhaustive search, which is impractical. The machine-based optimization using the simulated annealing (SA) is proposed to make the optimization practical. The objective is to reduce the energy loss, E_{LOSS} ($=\int I_C V_{CE} dt$), and at the same time to mitigate the overshoot of I_C, $I_{OVERSHOOT}$, for the turn-on case (the overshoot of V_{CE}, $V_{OVERSHOOT}$, for the turn-off case), whose definitions are shown graphically in Fig. 1. In order to achieve this goal, first, the energy loss and the overshoot values are normalized as below. The normalization helps to balance the energy loss optimization and the overshoot optimization.

$$E'_{LOSS} = \frac{E_{LOSS} - E_{LOSS,MIN}}{E_{LOSS,MAX} - E_{LOSS,MIN}},$$

$$I'_{OVERSHOOT} = \frac{I_{OVERSHOOT} - I_{OVERSHOOT,MIN}}{I_{OVERSHOOT,MAX} - I_{OVERSHOOT,MIN}},$$

$$V'_{OVERSHOOT} = \frac{V_{OVERSHOOT} - V_{OVERSHOOT,MIN}}{V_{OVERSHOOT,MAX} - V_{OVERSHOOT,MIN}},$$

where ' signifies the normalized quantity and the subscript MIN (MAX) signifies the minimum (maximum) of the corresponding quantity. For example, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate driving waveform is the fastest, that is, all of n_1, n_2, n_3, n_4, and n_∞ are 63. On the other hand, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate drive waveform is the slowest, that is, all of n_1, n_2, n_3, n_4, and n_∞ are 1. Likewise, the other minimum (maximum) overshoot values are obtained either by the slowest or the fastest gate driving waveform. After the normalization, all of the normalized quantities vary between 0 and 1. The object function, f_{OBJECT}, to be minimized is set as the Euclidean norm as below.

$$f_{OBJECT} = \sqrt{E'^{2}_{LOSS} + I'^{2}_{OVERSHOOT}}$$

for the IGBT turn-on case.

$$f_{OBJECT} = \sqrt{E'^{2}_{LOSS} + V'^{2}_{OVERSHOOT}}$$

for the IGBT turn-off case.

The total system setup is shown in Fig. 2. A pseudo-code of the SA algorithm is shown in the figure. The algorithm is implemented on a PC using MATLAB and generates a new trial waveform vector, X_{TRIAL}=[n_1, n_2, n_3, n_4]. Using this X_{TRIAL} vector as an input, LabVIEW generates control signals to the programmable gate driver. Then the device under test feeds back the measured voltage and current waveform data to

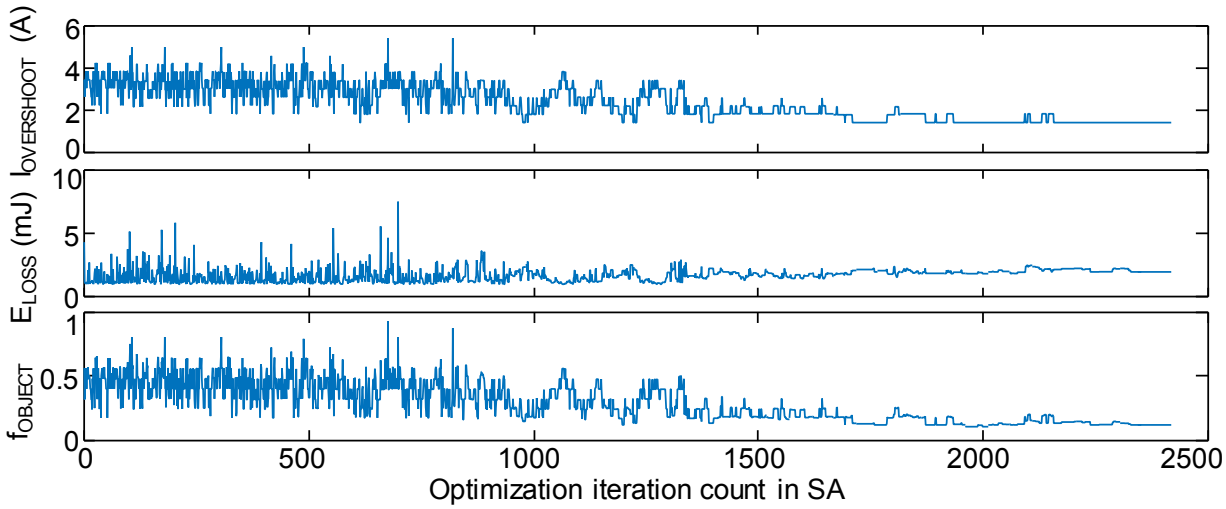

Fig. 3 History plots of $I_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during optimization process for turn-on

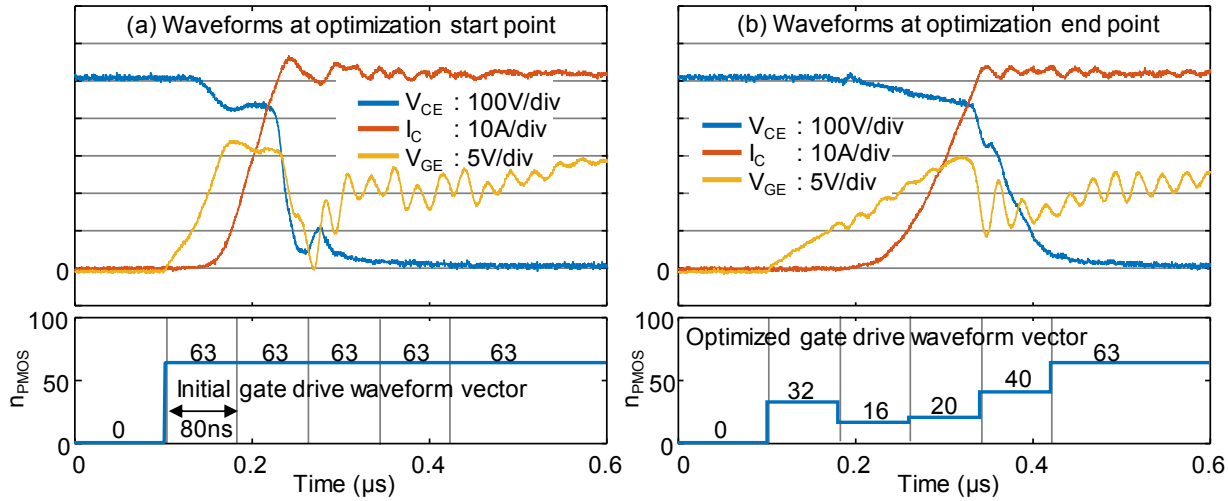

Fig. 4 Measured waveforms at (a) start point and (b) end point of SA optimization for IGBT turn-on case

the PC through an oscilloscope. Using the measured waveform data, PC calculates the object function, f_{OBJECT} based on the above-mentioned expressions. Depending on f_{OBJECT}, the PC generates the next trial waveform, X_{TRIAL}, according to the SA algorithm. The optimization itereation loop continues until no decrease in f_{OBJECT} is observed for a certain period. Other greedy algorithms were tried but stuck at sub-optimal points while the SA always finds much better optimal points.

III. Results for Turn-on of IGBT

The automatic optimization setup is applied to the turn-on case of the IGBT. In this case, a waveform vector [n_1, n_2, n_3, n_4] signifies the number of on-state driver PMOSs, n_{PMOS}, at a given time-segment. The initial waveform vector is set as [63, 63, 63, 63], that is, the fastest single-step turn-on case. Figure 3 shows the history plots of $I_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during the optimization process. The optimization process stops after 2420 iterations in this case. One iteration takes 2.2 seconds including the measurement time and the data transfer time to and from the PC. Thus, the total optimization takes 5324-s which is about one and a half hour. Multiple of the optimization processes were tried and all the trials finished within two hours.

The object function, f_{OBJECT}, is successfully minimized from 0.56 to 0.12 in this case. Just for information, a simple greedy optimization method where each of n_1, n_2, n_3, and n_4 is changed by either -1, 0 or 1 and the waveform vector which lowers f_{OBJECT} is searched, the optimization process is stuck at the initial point and never gives any better point. Thus, the optimization methods that can have the ability to get out from the local minima such as the SA is needed. No destructive breakdown of power devices was observed in the optimization process. The proposed method is demonstrated to be effective for an IGBT gate waveform optimization.

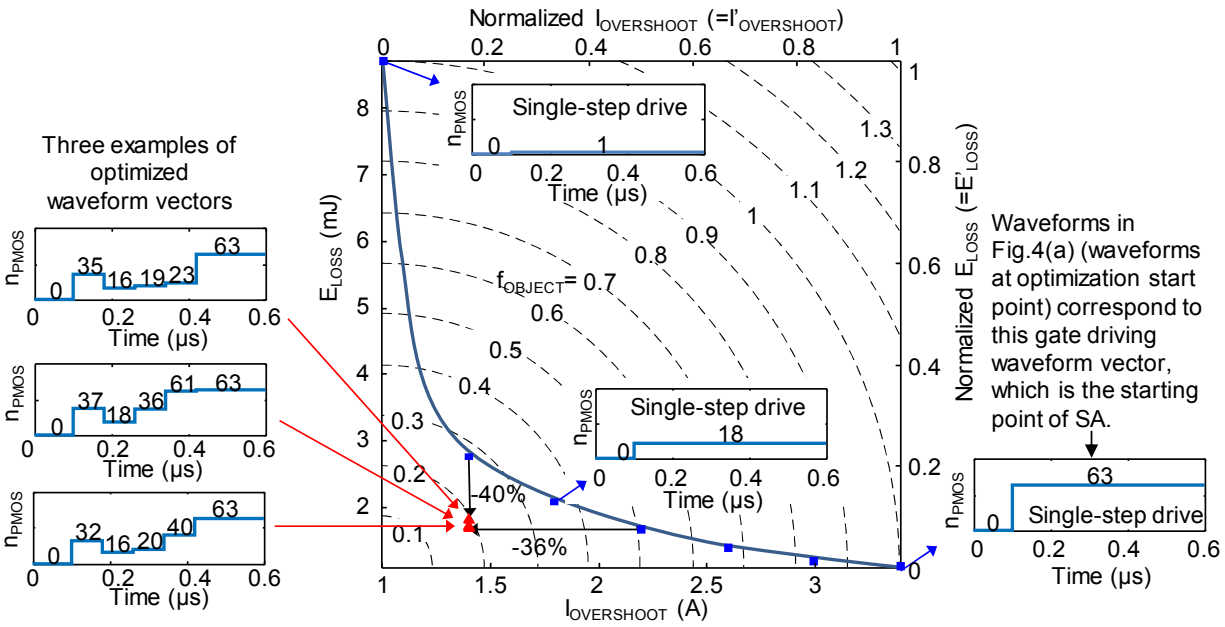

Fig. 5 E_{LOSS} - $I_{OVERSHOOT}$ trade-off. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

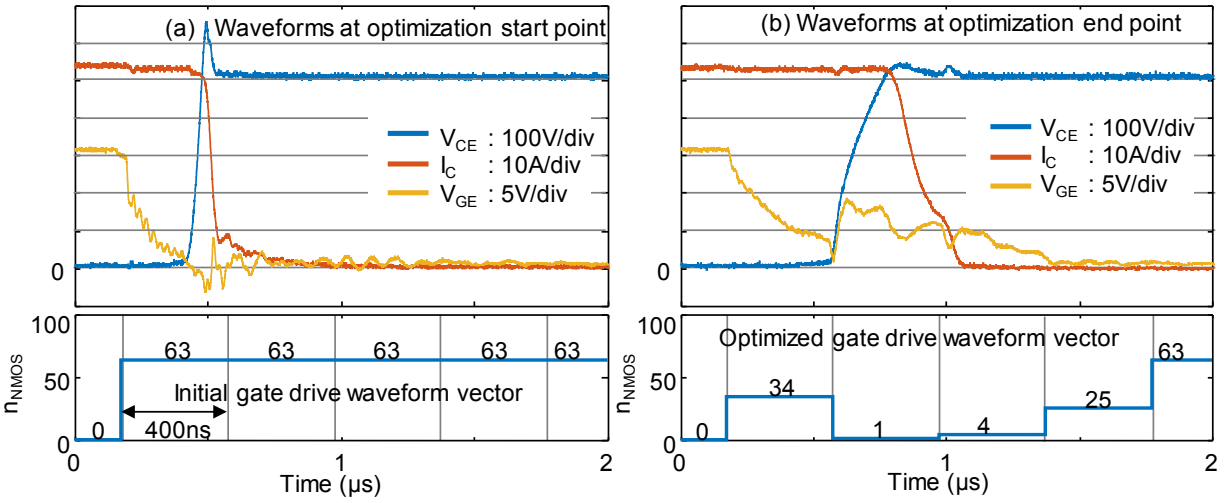

Fig. 6 Measured waveforms at (a) start point and (b) end point of SA optimization for IGBT turn-off case

Fig. 4 shows the measured waveforms at the initial point and the end point of the optimization iterations shown in Fig. 3. At the start, the waveform vector is a simple single-step function and shows the higher I_C overshoot. The improved gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This qualitative description of the optimized waveform is consistent with the previous publications [1,2,3] but the advantage of the proposed method is to provide the quantitative values of parameters.

More than ten optimization trials using SA are carried out and all the trials successfully found the optimized waveform vector, that is, the optimized gate driving waveform. Three examples of optimized waveform vectors are shown in Fig. 5. E_{LOSS} and $I_{OVERSHOOT}$ are in a trade-off situation. When E_{LOSS} is low with a fast gate drive, the current overshoot is large but when the current overshoot is decreased by the slower gate drive, the energy loss increases. Thus, in Fig. 5, the trade-off is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC, the achievable trade-off space is enlarged and 40% energy loss reduction and 36% current overshoot reduction are attained compared with the single-step gate drive.

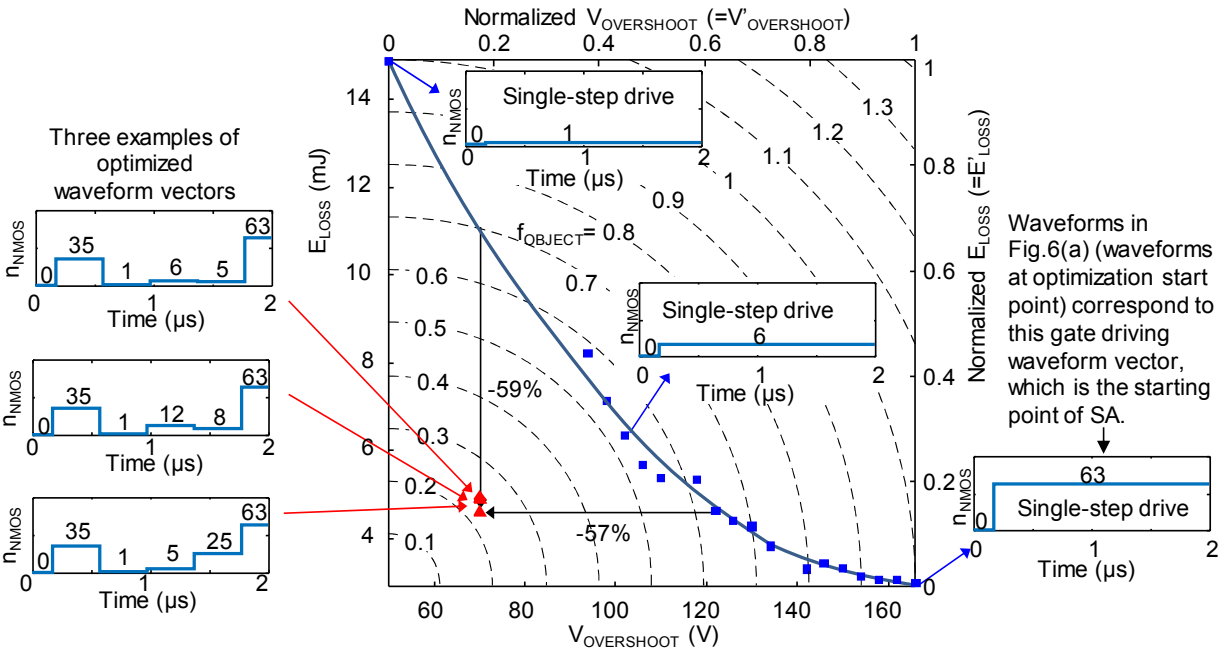

Fig. 7 E_{LOSS} - $V_{OVERSHOOT}$ trade-off. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

IV. Results for Turn-off of IGBT

As for the IGBT turn-off case, the optimization procedure is basically the same as the turn-on case. In this case, though, a waveform vector [n_1, n_2, n_3, n_4] signifies the number of on-state driver NMOSs, n_{NMOS}, at a given time-segment. Fig. 6 shows the measured waveforms at the initial point and the end point of the optimization process. The optimized gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This reduces the sharp voltage overshoot. The qualitative strategy for the optimized waveform is consistent with the previous publications [1,3] but the advantage of the proposed method is to be able to find the quantitative values of parameters in a practical time.

Three examples of optimized waveform vectors are shown in Fig. 7. It is seen that the three points are not exactly the same in the waveform vectors because of the stochastic nature of the SA optimization process. Still, all the optimized waveform shows considerable reduction in the object function and all have the characteristics that the drivability is lowered in the middle of the driving process. In Fig. 7, the trade-off between the energy loss, E_{LOSS}, and the voltage overshoot, $V_{OVERSHOOT}$, is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC and four time-segmented drive, the achievable trade-off space is enlarged and 59% energy loss decrease and 57% voltage overshoot reduction are achieved compared with the single-step gate drive.

V. Summary

A novel search method based on simulated annealing algorithm is described to find the better gate driving waveforms for power devices. The method is shown to be effective in optimizing the trade-off between the energy loss and the waveform overshoot by using a double pulse test configuration as an example. In this paper, the number of the time-segments is set to four but it may be increased to 16 or more for further better driving waveforms. Then, the search space increases exponentially and the proposed automatic optimization approach becomes more indispensable. Although an optimization example is depicted in this paper, the presented SA-based optimization for the gate driving waveforms can be applicable to the wider range of problems toward the better circuit performance.

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