General-Purpose Clocked Gate Driver (CGD) IC with Programmable 63-Level Drivability to Reduce Ic Overshoot and Switching Loss of Various Power Transistors

Koutaro Miyazaki*, Seiya Abe†, Masanori Tsukuda†, Ichiro Omura†, Keiji Wada‡, Makoto Takamiya* and Takayasu Sakurai*

*University of Tokyo, Tokyo, Japan
†Kyushu Institute of Technology, Fukuoka, Japan
‡Tokyo Metropolitan University, Tokyo, Japan
Email: koutaro@iis.u-tokyo.ac.jp

***Abstract*—A general-purpose clocked gate driver (CGD) IC to generate an arbitrary gate waveform is proposed to provide a universal platform for fine-grained gate waveform optimization handling various power transistors. The fabricated IC with 0.18µm BCD process has 63 PMOS and 63 NMOS driver transistors on a chip whose activation patterns are controlled by 6-bit digital signals and 25-MHz clock (= 40-ns time step control). In the 500-V switching measurements, the proposed CGD reduces the I_C overshoot by 25% and 41% and the energy loss by 38% and 55% for Si-IGBT and SiC-MOSFET, respectively.**

Keywords—Gate driver; IGBT; SiC; Clock; Programmable

I. INTRODUCTION

A gate driver is a key technology for the switching of power devices to minimize the switching loss and the current overshoot. Conventional gate drivers, however, have two problems: (1) customized design to each power transistor (e.g. Si-IGBT, SiC-MOSFET) increases the development cost and turnaround time (TAT), and (2) limited programmability (e.g. 2 gate resistances [1-5], multi voltage levels [6-9], and 9 output resistances of the segmented gate drivers [10]) prevents a precise gate waveform optimization for the low noise and the low loss of the power transistors. To solve the problems, a general-purpose clocked gate driver (CGD) IC is proposed to provide a universal platform for fine-grained gate waveform optimization handling various power transistors including Si-IGBT and SiC-MOSFET, thereby reducing the development cost and TAT for the gate drivers. The proposed CGD IC enables a fine-grained programmability of 63-level drivability and 40-ns step timing control, which reduces I_C overshoot and turn-on energy loss for Si-IGBT and SiC-MOSFET in the 500-V switching measurement. The programmability of CGD is the finest compared with the previous gate drivers [1-10].

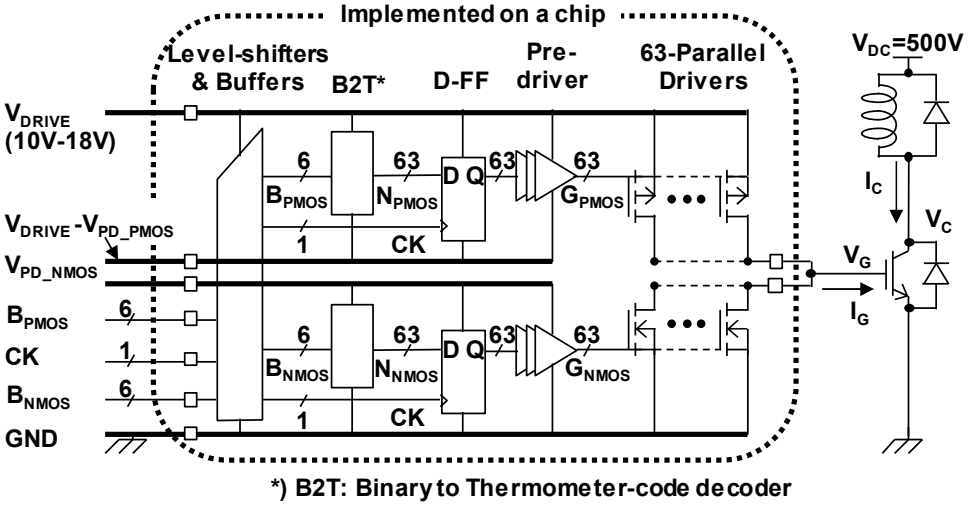

Fig. 1 Schematic diagram of general-purpose clocked gate driver (CGD) IC.

II. System Implementation

The schematic diagram of the implemented general-purpose CGD IC is shown in Fig. 1. CGD IC is developed for the switching of power devices at V_{DC} = 500V. In order to realize programmable 63-level drivability, 63 parallel drivers are connected to the gate of the power device and a 6-bit binary control signal, B_{PMOS} (B_{NMOS}), is applied to specify the number of activated PMOS (NMOS) driver transistors, N_{PMOS} (N_{NMOS}). A pair of 6-bit signals (B_{PMOS} and B_{NMOS}) are latched by the clock (CK) and activate the final 63 PMOS (NMOS) transistors. CK frequency is 25MHz and 40-ns time step control of the drivability is achieved. The power supply voltage (V_{DRIVE}) of CGD IC is 10V–18V, and V_{DRIVE} of 15V is used in the following measurements. The voltage swing of input digital signals (B_{PMOS}, B_{NMOS}, and CK) is 5V, and the swing is increased to V_{DRIVE} by level-shifters. By adjusting the pre-driver voltage swing, V_{PD_PMOS} and V_{PD_NMOS}, from 1.2V to 5V, the output drivability of a single driver MOS transistor can be tuned from 3mA to 80mA. The peak drivability is 63 times of the single driver, which corresponds to the maximum peak current of the gate current (I_G) from 0.19A (= 3mA x 63) to 5A (= 80mA x 63). V_{PD_PMOS} and V_{PD_NMOS} of 1.8V is used in the following measurements.

The binary-coded input is indispensable since 63 x 2 input pins are too many to handle. The binary signals, however, may cause glitch problems in the gate voltage (V_G). The glitch will break down the power transistors. For example, when the binary input changes from 011111 (31) to 100000 (32), there is a possibility that the state goes from 011111 (31) to 111111 (63) to 100000 (32) causing a few nano-seconds glitch at the pre-driver, if there are variability of devices and interconnection designs which make the most significant bit change faster than the other bits. This is the cause of the glitch problems. To prevent this problem, a small-sized binary to thermometer-code decoder in Fig. 2 is employed.

Fig. 3 shows operation waveforms for 63 PMOS transistors to pull up V_G in CGD IC. The operation for 63 NMOS transistors to pull down V_G is similar. An arbitrary I_G waveform is generated by applying a control bit pattern (B_{PMOS} (B_{NMOS})) in each clock cycle with 40-ns step and digitally specifying time and current pairs of t_i and I_{Gi} (i=1,2,3…n).

III. Modeling of Gate Driver

In this chapter, the modeling of the 63 parallel drivers in Fig. 1 is discussed. In the previous the segmented gate drivers [10], the transistors in the segmented gate drivers (Fig. 4(a)) were modeled as a resistor (Fig. 4(b)). In this paper, it is proposed that the transistors in the segmented gate drivers should be modeled as current-source (Fig. 4(c)) instead of the resistor (Fig. 4(b)). Fig. 5 shows the SPICE simulated pull-up and pull-down waveforms of V_G with two models in Fig. 4. The capacitance in Fig. 4 is 22nF emulating the gate capacitance of the power devices. V_{PD_PMOS} and V_{PD_NMOS} are 5V and 1.8V in Figs. 5 (a) and (b), respectively. Compared with the resistor model, the current-source model is in good agreement with the driver with transistors. Therefore, the gate driver behaves like the constant-current driver (Fig. 4(c)) rather than the resistor (Fig. 4(b)) because of the high output resistance of MOS transistors in a saturation region.

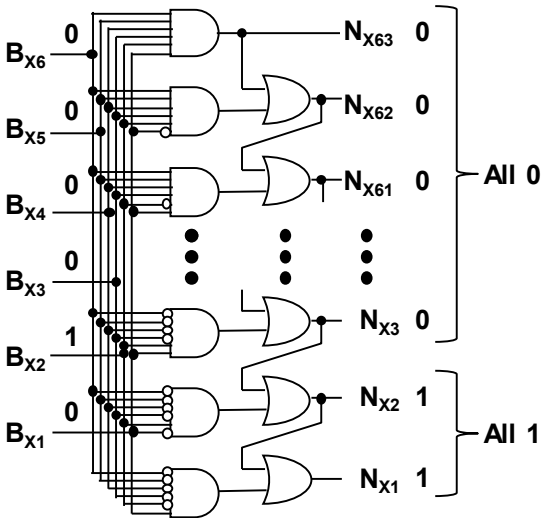

Fig. 2 Binary to thermometer-code decoder.

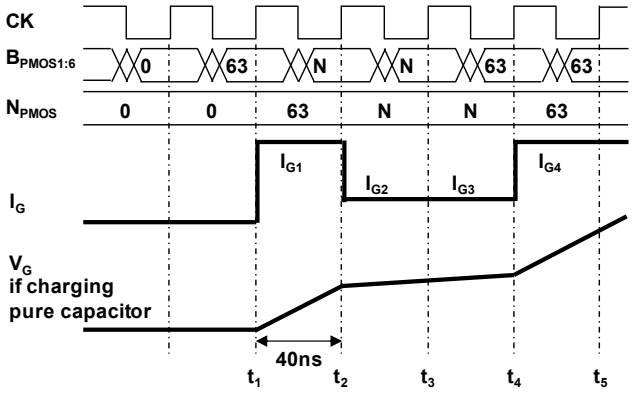

Fig. 3 Operation waveforms for 63 PMOS transistors to pull up V_G in CGD IC.

IV. Measurement Results

The proposed general-purpose CGD IC is fabricated with 40V, 0.18μm BCD process. Fig. 6 shows a die photo of CGD IC. The core size is 2300μm by 730μm. Fig. 7 shows photos of PCB. The 2.5-mm square CGD IC is placed on the top side of PCB. Si-IGBT and SiC diodes are placed on the reverse side of PCB.

Turn-on characteristics are measured with a double-pulse setup shown in Fig. 1 with SiC diodes (C4D10120D, 1200V, 18A) at V_{DC} = 500V. To demonstrate the versatility of the proposed general-purpose CGD IC, both Si-IGBT (IRG7PH46UPbF, 1200V, 75A) and SiC-MOSFET (SCH2080KE, 1200V, 40A) are driven by CGD IC. Although in Fig. 1, an IGBT symbol is used for a power device, the IGBT is replaced by SiC-MOSFET when SiC-MOSFET is under test. Notations such as I_C and V_C are used even for the SiC-MOSFET device just for simplicity.

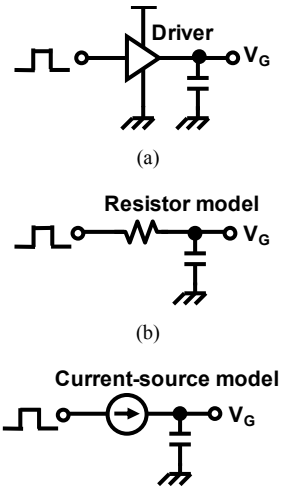

Fig. 4 Modeling of gate drivers. (a) Original gate driver. (b) Conventional resistor model. (c) Proposed current-source model.

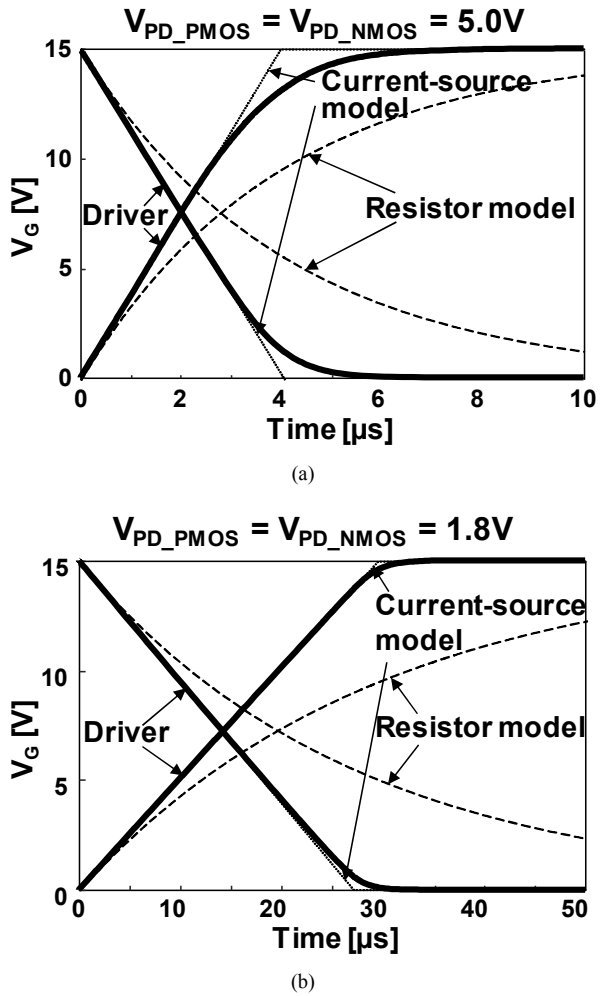

Fig. 5 SPICE simulated pull-up and pull-down waveforms of V_G with two models in Fig. 4. V_{PD_PMOS} and V_{PD_NMOS} are 5V and 1.8V in (a) and (b), respectively.

To show the advantage of the proposed CGD IC with programmable 63-level drivability, three types of gate waveforms shown in Fig. 8 are compared. Fig. 8 (a) shows a conventional "no active gate drive" [11]. To show the trade-off between the turn-on energy loss and I_C overshoot, I_G to pull-up V_G is varied by N_{PMOS} in the measurement. Fig. 8 (b) shows a conventional "9-level active gate drive" emulating the 9-level segmented gate drivers [10]. This waveform is based on [5, 7, 9-10, 12]. At the turn-on, N_{PMOS} changes from 0 to m and keeps m for t_1. Then, N_{PMOS} changes from m to 9 level of i (i = 2 to 58 with 7 increments in between) and keeps i for t_2. Finally, N_{PMOS} changes from i to m. Fig. 8 (c) shows the proposed "63-level active gate drive". Fig. 8 (c) is the same as Fig. 8 (b) except for i. In Fig. 8 (c), i is from 0 to 63 with 1 increment in

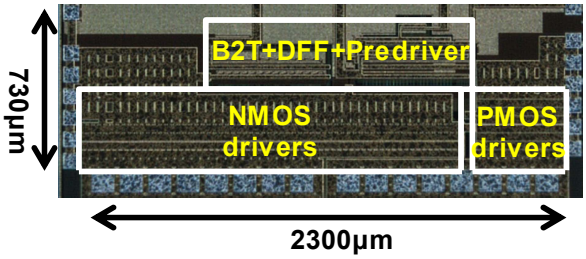

Fig. 6 Die photo of CGD IC.

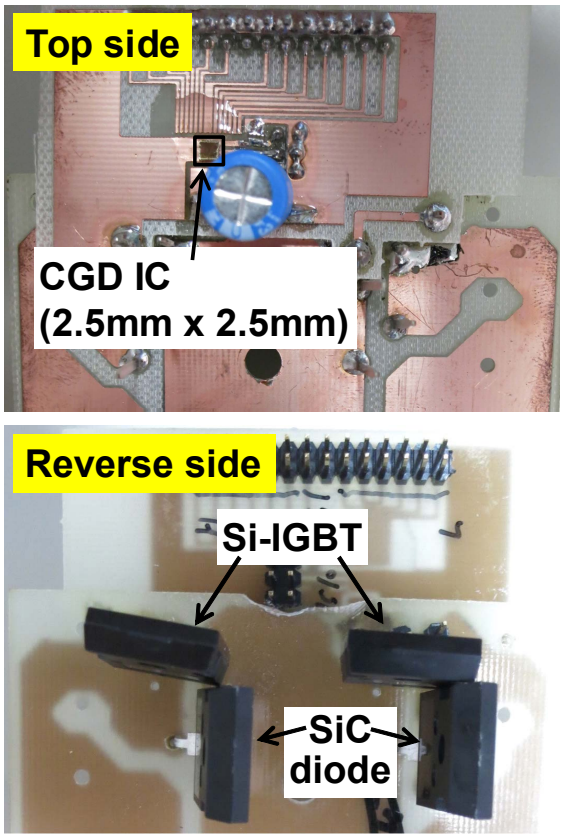

Fig. 7 Photos of PCB.

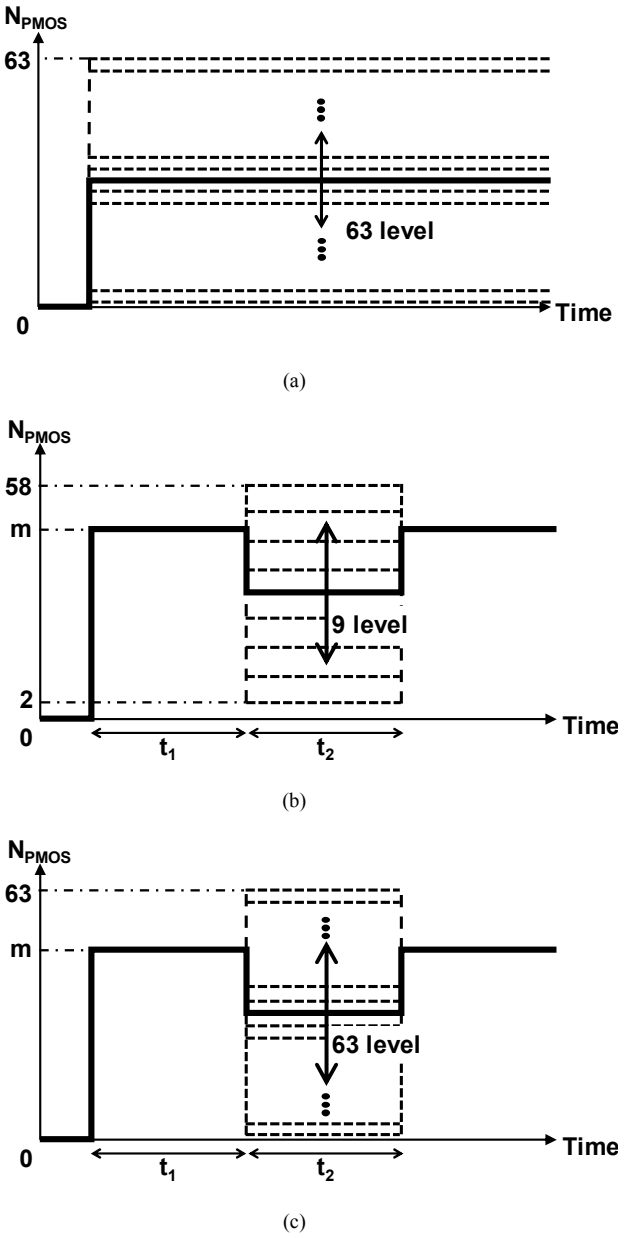

Fig. 8 Three types of gate waveforms. (a) No active gate drive. (b) 9-level active gate drive. (c) Proposed 63-level active gate drive.

between. Table I shows m, t_1, and t_2 in the measurements for Si-IGBT and SiC-MOSFET, respectively.

Figs. 9 and 10 show measured energy loss versus I_C overshoot in turn-on characteristics at 500-V switching with the three gate waveforms shown in Fig. 8 for Si-IGBT and SiC-MOSFET, respectively. In the no active gate drive, the trade-off between the turn-on energy loss and I_C overshoot is observed. By using 63-level active gate drive, however, the loss-overshoot trade-off can be optimized more compared with cases of 9-level active gate drive [10] and no active gate drive. The proposed 63-level active gate drive reduces the measured energy loss at the same I_C overshoot by 38% (Fig. 9) and 55%

Table I Parameters used in measurements for Si-IGBT and SiC-MOSFET

	Si-IGBT	SiC-MOSFET
m	31	63
t_1	160ns	40ns
t_2	160ns	80ns

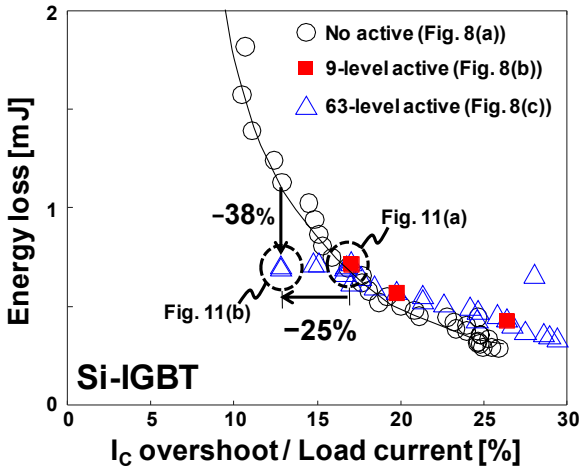

Fig. 9 Measured energy loss vs. I_C overshoot in turn-on characteristics at 500-V switching for Si-IGBT.

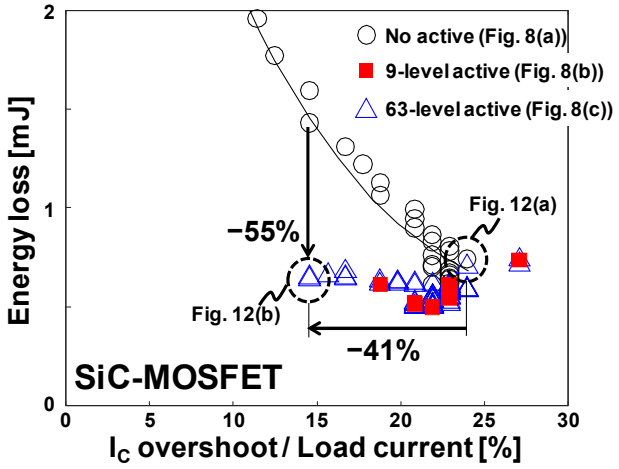

Fig. 10 Measured energy loss vs. I_C overshoot in turn-on characteristics at 500-V switching for SiC-MOSFET.

(Fig. 10) for Si-IGBT and SiC-MOSFET, respectively. Similarly, the proposed 63-level active gate drive reduces the measured I_C overshoot at the same energy loss by 25% (Fig. 9) and 41% (Fig. 10) for Si-IGBT and SiC-MOSFET, respectively. The corresponding measured waveforms of N_{PMOS}, V_G, V_C, and I_C for Si-IGBT and SiC-MOSFET are shown in Figs. 11 and 12, respectively. The 25% and 41% reduction of I_C overshoot are clearly shown in Figs. 11 and 12, respectively.

Table II shows a comparison of the proposed CGD IC with previous gate drivers. This work achieved the 40-ns step timing

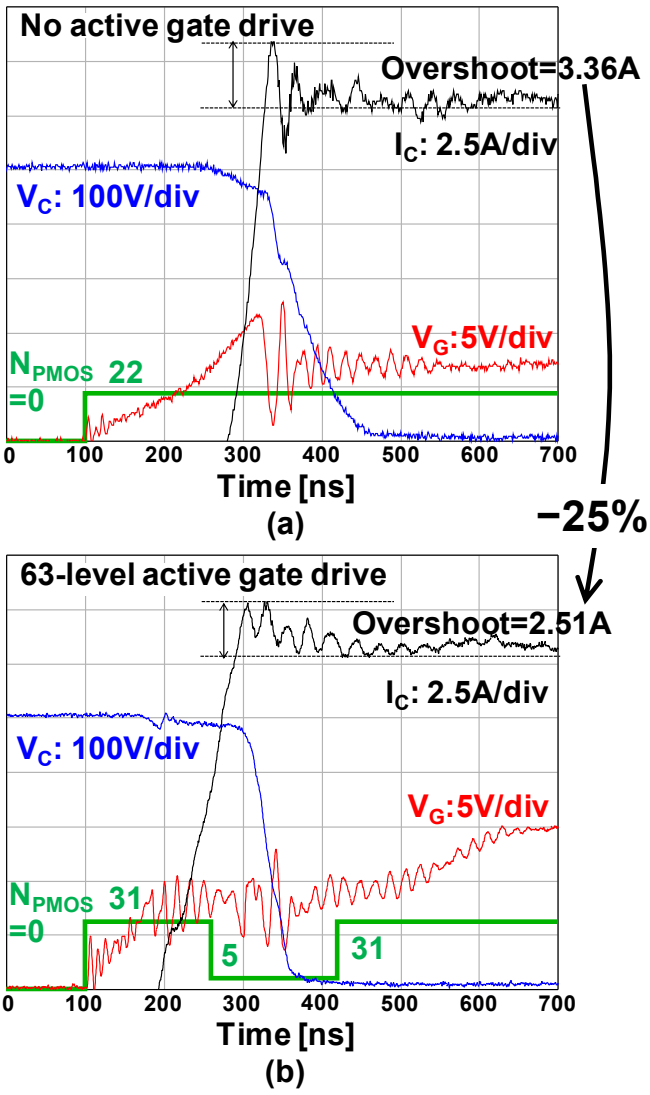

Fig. 11 Measured waveforms for Si-IGBT corresponding to Fig. 9. (a) No active gate drive. (b) Proposed 63-level active gate drive.

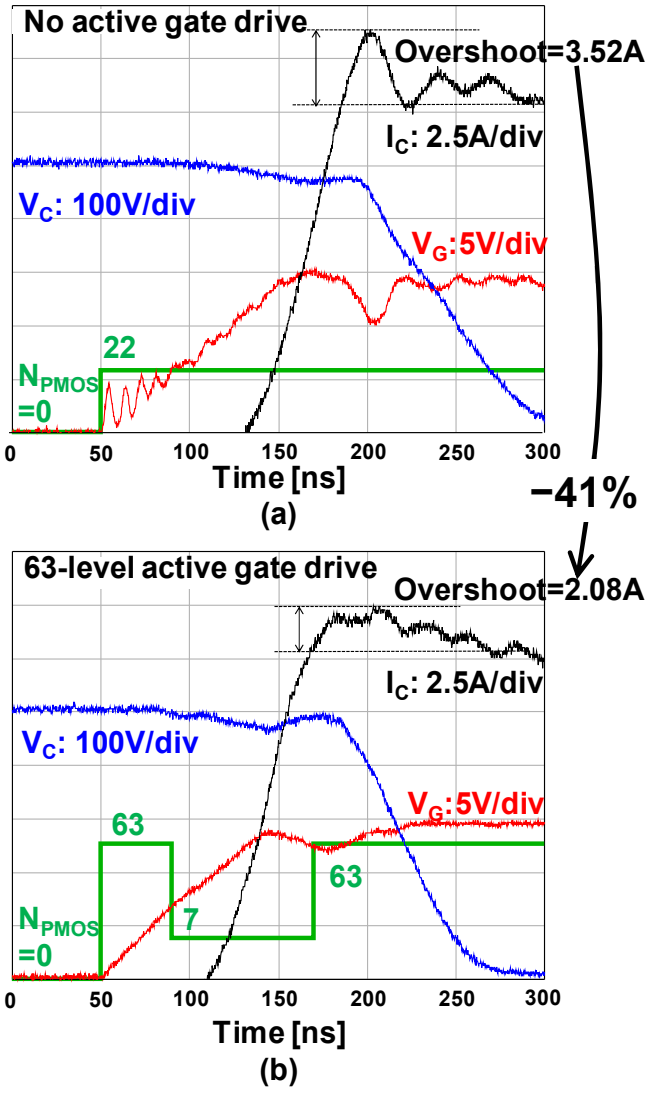

Fig. 12 Measured waveforms for SiC-MOSFET corresponding to Fig. 10. (a) No active gate drive. (b) Proposed 63-level active gate drive.

control and 63-level drivability, thereby enabling the gate waveform optimization for both Si-IGBT and SiC-MOSFET. The time programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels.

V. Conclusions

The general-purpose CGD IC to generate an arbitrary gate waveform is the universal platform for fine-grained gate waveform optimization handling various power transistors. The 40-ns step timing programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels in the previously published gate drivers. In the 500-V switching measurements, the proposed CGD

Table II Comparison with previous gate drivers

	[1]	[2]	[6]	[10]	This work
Implementation	PCB	PCB	PCB	IC	IC
Target power device	Si-IGBT	Si-IGBT	SiC-MOSFET	Si-IGBT	Si-IGBT & SiC-MOSFET
Time programmability	NA	NA	NA	NA	40-ns step
Number of drivability levels	2	2	4	9	63
How to change drivability	R_G	R_G	Drive voltage	Driver size	N_{PMOS}, N_{NMOS} V_{PD_PMOS}, V_{PD_NMOS}
Gate current	NA	NA	NA	NA	3mA~5A

reduces the I_C overshoot by 25% and 41% and the energy loss by 38% and 55% for Si-IGBT and SiC-MOSFET, respectively.

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