56-Level Programmable Voltage Detector in Steps of 50mV for Battery Management

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***Abstract*— A programmable voltage detector (PVD) for the battery management is developed for the first time. In battery management applications, PVD's with fine voltage resolution (<±1% of battery voltage) are required to precisely control the charging and discharging of the battery and to provide a universal voltage detector. The proposed fine voltage-step subtraction (FVS) method in PVD enables the wide detection voltage (V_{DETECT}) range from 1.88V to 4.67V, fine V_{DETECT} resolution of 50mV, and the 56-level linear programmability. Compared with previous publications, the 50-mV resolution is the smallest and the 56-level programmability is the largest. The programmability of V_{DETECT} enables a V_{DETECT} hopping capability achieving time-varying V_{DETECT} to reduce the number of voltage detectors in the battery management system. PVD fabricated in 5V, 250-nm CMOS process shows the measured power consumption of 13nW at 3.5V and the temperature coefficient of 0.17mV/°C in -20°C to 80°C.**

I. INTRODUCTION

In the applications of batteries (e.g. lithium-ion batteries), a voltage detector is one of the key building blocks in a battery management system. Fig. 1 shows the definition of the voltage detector in this paper. When the input voltage (V_{IN}) is higher than a pre-determined detection voltage (V_{DETECT}), the output voltage (V_{OUT}) is low. In contrast, when V_{IN} is lower than V_{DETECT}, V_{OUT} is high. In the recent battery management system for the lithium-ion batteries, both precise control of V_{DETECT} (e.g. ±1% (= ±42mV) of the battery voltage (4.2V)) and various V_{DETECT}'s (e.g. at least 2 V_{DETECT}'s to start charging or discharging, and typically 6 V_{DETECT}'s [1]) are required. In the conventional voltage detectors [2,7-8], however, have 3 problems: (1) V_{DETECT} is not programmable (= factory-trimmed) and users cannot change V_{DETECT}, (2) V_{DETECT} resolution (e.g. 100mV [2]) is larger than the target resolution of ±42mV, and (3) multiple voltage detectors are required for multiple V_{DETECT}'s, which increases cost and area. Though a programmable voltage detector (PVD) with V_{DETECT} ranging from 0.52V to 0.85V for a RF energy harvesting is reported [3], the PVD cannot be used for the lithium-ion batteries, because the V_{DETECT} range does not fit the voltage range (e.g. 3.0V to 4.2V) of the lithium-ion batteries.

Therefore, in this paper, a new PVD with a programmable 56-level V_{DETECT} ranging from 1.88V to 4.67V in steps of 50mV is proposed for the battery management system. The 50-mV step (= ±25mV) programmability satisfies the target resolution of ±42mV for the lithium-ion batteries. Compared with previous publications, the 50-mV step is the smallest and the 56-level programmability is the largest. Thanks to the programmability, the proposed PVD can be a general-purpose component and users can freely change V_{DETECT}. The programmability of V_{DETECT} also enables a V_{DETECT} hopping capability achieving time-varying V_{DETECT}, thereby reducing the number of voltage detectors.

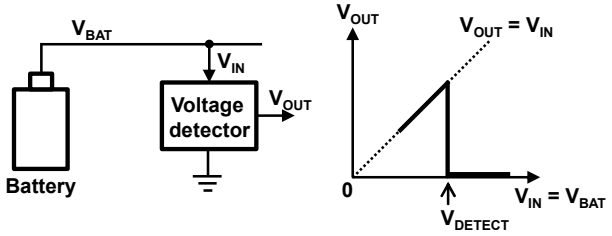

Fig. 1. Definition of voltage detector for battery management.

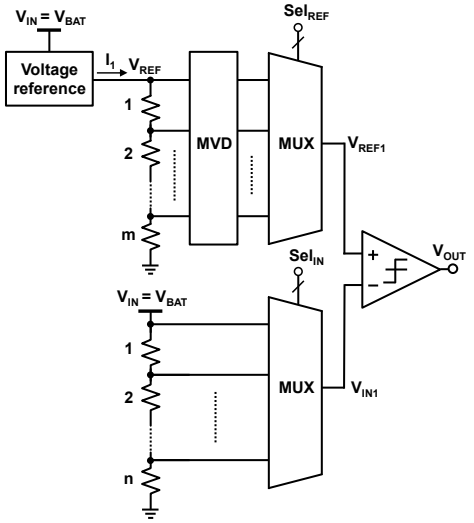

Fig. 2. Circuit schematic of conventional programmable voltage detector (PVD) [3]. MVD is multiple voltage duplicator.

In this paper, to achieve PVD with wide V_{DETECT} range, fine V_{DETECT} steps, and linear V_{DETECT} programmability, a fine voltage-step subtraction (FVS) method is proposed. In PVD, a low power operation is also required in battery-operated mobile devices and IoT nodes, because PVD always operates to monitor the battery. In the conventional voltage detectors, however, the power consumption is dominated by the bandgap reference circuits (32nW [4] to 100nW [5]). Though a low power voltage reference (VR) circuit is reported [6], PVD with the VR circuit shows a non-linear V_{DETECT} programmability, because the line sensitivity of the VR is large (= 2.3mV/V). To solve the problem, a V_{DD} regulated voltage reference (VRVR) circuit with low power (2nW) and low line sensitivity of 50μV/V is proposed.

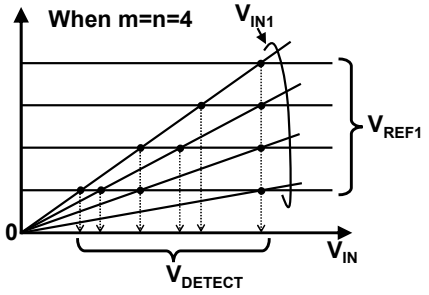

Fig. 3. Operation principle of conventional PVD.

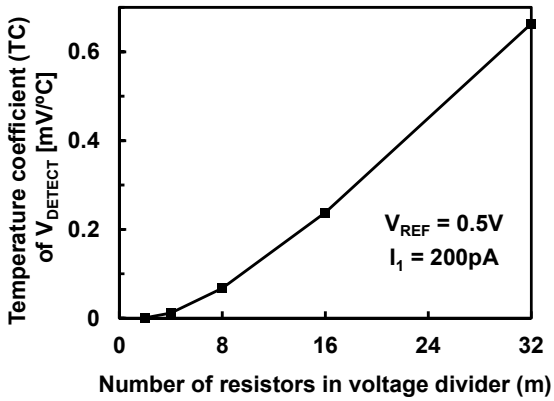

Fig. 4. Simulated m dependence of TC of V_{DETECT} in conventional PVD.

II. Conventional Programmable Voltage Detectors

It is shown that a conventional PVD [3] has 2 problems: (1) linear V_{DETECT} programmability is not available, and (2) both fine V_{DETECT} steps and low temperature coefficient (TC) of V_{DETECT} are not achieved. Fig. 2 shows a circuit schematic of the conventional PVD [3], where a multiple voltage duplicator (MVD) is a multiple-input multiple-output voltage buffer. Fig. 3 shows an operation principle of the conventional PVD. The offset of V_{REF1} is varied by m and the gradient of V_{IN1} is varied by n. Points at the intersection of V_{REF1}'s with V_{IN1}'s are V_{DETECT}'s. As shown in Fig. 3, V_{DETECT} changes non-linearly and non-monotonously with control-bits. A straightforward method to obtain both linear V_{DETECT} programmability and fine V_{DETECT} steps is to change V_{REF1} at fixed V_{IN1} with increasing m. Fig. 4, however, shows a simulated m dependence of TC of V_{DETECT} in the conventional PVD at fixed V_{IN1}, $V_{REF} = 0.5$V, and $I_1 = 200$pA. With increasing m, TC also increases and exceeds the design target of 0.2mV/°C (= 20mV across 100°C). When m is increased, the voltage drop per resistor is reduced and the drain-source voltage (V_{DS}) of MOSFET's in MVD is reduced. The reduced V_{DS} degrades the capability of the multiple voltage duplication in MVD and increases TC. Therefore, another method is required to achieve both fine V_{DETECT} steps and low TC of V_{DETECT}.

III. Proposed Programmable Voltage Detectors

A. Fine Voltage-Step Subtraction (FVS) Method

Fig. 5 shows a circuit schematic of a proposed PVD with FVS method. The circuit implementation of resistors for voltage divider, MVD, MUX's, and a comparator is similar to [3]. Instead of increasing m in the voltage divider in Fig. 2, a

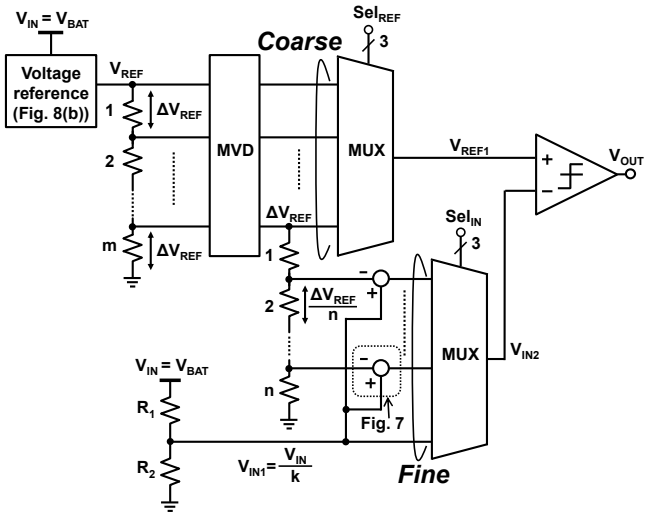

Fig. 5. Circuit schematic of proposed PVD with fine voltage-step subtraction (FVS) method.

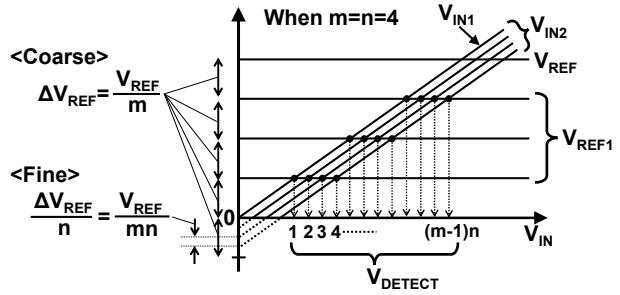

Fig. 6. Operation principle of proposed PVD with FVS.

hierarchy of a coarse voltage divider for V_{REF1} and a fine voltage divider for V_{IN2} is used in Fig. 5. Fig. 6 shows an operation principle of FVS. ΔV_{REF} is a coarse voltage step and $\Delta V_{REF}/n$ is a fine voltage step. In FVS, the fine V_{DETECT} steps are achieved by comparing the coarsely varied V_{REF1} and finely varied V_{IN2}, where V_{IN2} is obtained by subtracting the fine voltage steps of $\Delta V_{REF}/n$ from V_{IN1}. The linear V_{DETECT} programmability is achieved, because the fine voltage step is generated from the coarse voltage step. An equation for V_{DETECT} is derived below.

$$\Delta V_{REF} = \frac{V_{REF}}{m} \tag{1}$$

$$V_{REF1} = \frac{i}{m} V_{REF} \quad (i = 1, 2, \ldots, m-1) \tag{2}$$

$$V_{IN1} = \frac{V_{IN}}{k} \qquad (k > 1) \tag{3}$$

$$V_{IN2} = V_{IN1} - \frac{j}{n} \Delta V_{REF} \qquad (j = 0, 1, \ldots, n-1) \tag{4}$$

Substituting (1) into (4),

$$V_{IN2} = V_{IN1} - \frac{j}{mn} V_{REF} \tag{5}$$

V_{DETECT} is V_{IN} when

$$V_{REF1} = V_{IN2} \tag{6}$$

Substituting (2) and (5) into (6),

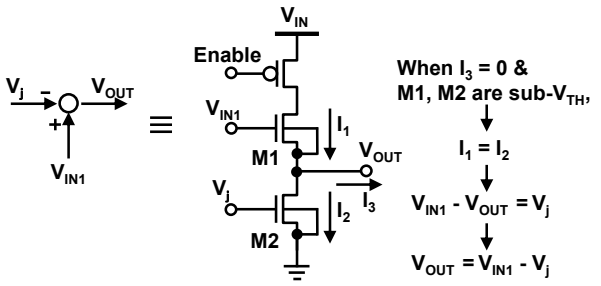

Fig. 7. Proposed voltage subtractor.

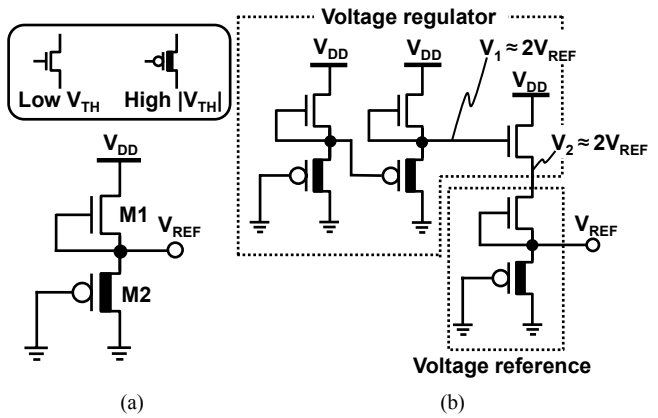

Fig. 8. (a) Conventional voltage reference (VR) based on [6]. (b) Proposed V_{DD} regulated voltage reference (VRVR).

$$\frac{i}{m}V_{\mathrm{REF}} = V_{\mathrm{IN1}} - \frac{j}{mn}V_{\mathrm{REF}} \tag{7}$$

$$V_{\mathrm{IN1}} = \left(\frac{i}{m} + \frac{j}{mn}\right)V_{\mathrm{REF}} \tag{8}$$

Substituting (3) into (8),

$$V_{\mathrm{DETECT}} = k\left(\frac{i}{m} + \frac{j}{mn}\right)V_{\mathrm{REF}} \tag{9}$$

As shown in (9), by adding coarse voltage steps of V_{REF}/m and fine voltage steps of V_{REF}/mn, both linear V_{DETECT} programmability and fine V_{DETECT} steps are achieved. Thus, in the proposed PVD with FVS, wide V_{DETECT} range, fine V_{DETECT} steps, linear V_{DETECT} programmability, and TC of V_{DETECT} less than 0.2mV/°C are achieved, because m and n are 8 in our implementation.

In FVS, low power voltage subtractors in Fig. 5 are one of the key building blocks. Fig. 7 shows a circuit schematic of the proposed voltage subtractor and its operation principle. M1 and M2 are in subthreshold operation, and $I_3 = 0$, because the input impedance of MUX is high. As shown in Fig. 7, $V_{OUT} = V_{IN1} - V_j$, and the voltage subtraction is achieved. The proposed voltage subtractor is low power (1.4nA at 3.5V) because of the subthreshold operation. To reduce the power consumption of the multiple voltage subtractors in PVD, a power gating switch is added as shown in Fig. 7 and non-selected voltage subtractors are turned off.

B. V_{DD} Regulated Voltage Reference (VRVR)

VRVR with low power (2nW) and low line sensitivity of 50µV/V is proposed. Figs. 8 (a) and (b) show circuit schematics of a conventional 2-transistor VR circuit based on [6] and the proposed VRVR, respectively. In Fig. 8 (a), V_{REF} is determined by the threshold voltage difference between M1 and M2. In Fig. 8 (b), power supply voltage (V_{DD}) regulator is added to Fig. 8 (a) to improve the line sensitivity (= ΔV_{REF} / ΔV_{DD}). The power overhead due to the regulator over Fig. 8 (a) is 10%. When all transistors are in subthreshold operation, $V_1 = V_2 \approx 2V_{REF}$, which shows V_2 is regulated. Specifically, when ΔV_1 / ΔV_{DD} is $1/a$, ΔV_{REF} / ΔV_2 is also $1/a$, and ΔV_{REF} / ΔV_{DD} is $1/a^2$. Fig. 9 shows a simulated V_{DETECT} dependence on digital code of PVD in the conventional VR and the proposed VRVR. In the conventional VR, a non-linear V_{DETECT} programmability is observed, while linear V_{DETECT} programmability is achieved in VRVR. To clarify the reason for the non-linearity, Fig. 10 shows a simulated V_{DD} dependence of V_{REF} in the conventional VR and the proposed VRVR. In the conventional VR, the line sensitivity is large (=2.3mV/V), which results in the non-linearity of V_{DETECT} in PVD. In contrast, the line sensitivity of VRVR is 50µV/V, which is 1/46 of that of the conventional VR, thereby achieving the linear V_{DETECT} programmability.

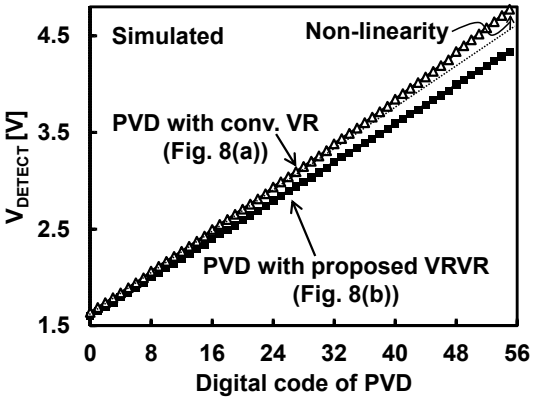

Fig. 9. Simulated V_{DETECT} dependence on digital code of PVD.

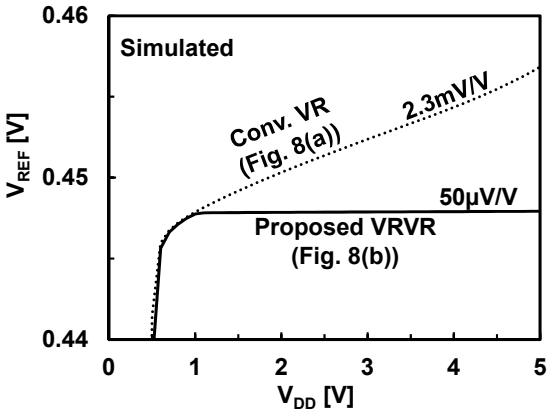

Fig. 10. Simulated V_{DD} dependence of V_{REF}.

IV. Measured Results

Fig. 11 shows a die photo and a layout of the proposed PVD fabricated in 5V, 250-nm CMOS process. The core area is 230µm by 180µm. The measured power consumption is 13nW at 3.5V. Fig. 12 shows a measured V_{DETECT} dependence on digital code of PVD. PVD with linear 56-level V_{DETECT} ranging from 1.88V to 4.67V in steps of 50mV is achieved. Fig. 13 shows a measured temperature dependence of V_{DETECT}. TC is

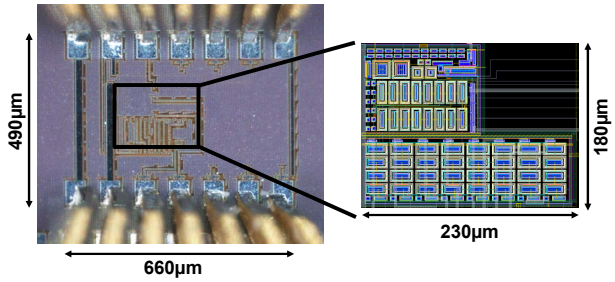

Fig. 11. Die photo and layout of proposed PVD.

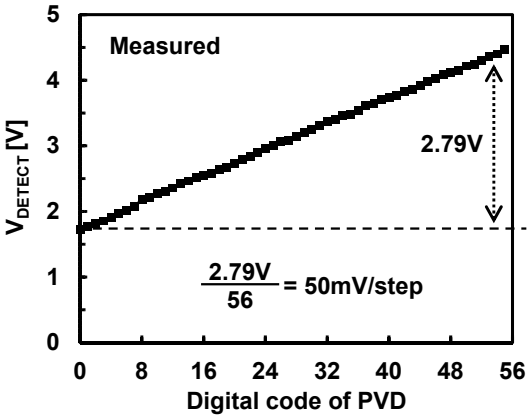

Fig. 12. Measured V_{DETECT} dependence on digital code of PVD.

0.17mV/°C in -20°C to 80°C, achieving the design target of 0.2mV/°C. The programmability of V_{DETECT} enables a V_{DETECT} hopping capability achieving time-varying V_{DETECT}, thereby reducing the number of voltage detectors. Fig. 14 shows measured waveforms of V_{DETECT} hopping, where V_{DETECT} is varied between $V_{DETECT(MAX)}$ and $V_{DETECT(MIN)}$, and V_{IN} is fixed to 3.3V. The proposed V_{DETECT} hopping is successfully demonstrated. The hopping delay is 3.2ms and 0.16ms for rise and fall edge of V_{OUT}, respectively, which is sufficiently fast for the battery management. In Table I, this work is compared with the previously published voltage detectors. This work is first PVD covering the V_{DETECT} range for the lithium-ion batteries. The 56-level programmability is the largest and the 50-mV step is the smallest.

V. Conclusions

Thanks to the proposed FVS and VRVR, PVD with linear 56-level V_{DETECT} ranging from 1.88V to 4.67V, covering the range for the lithium-ion batteries, in steps of 50mV (=±25mV) (<±1% of battery voltage) is achieved for the first time. Thanks to the programmability, the proposed PVD can be a general-purpose component and users can freely change V_{DETECT}. The 56-level programmability is the largest and the 50-mV step is the smallest. PVD fabricated in 5V, 250-nm CMOS process shows the measured power consumption of 13nW at 3.5V and TC of 0.17mV/°C in -20°C to 80°C.

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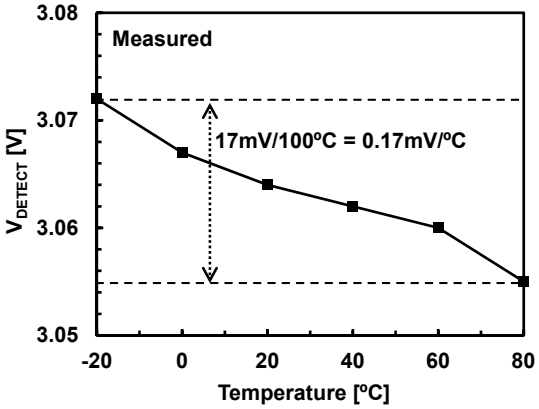

Fig. 13. Measured temperature dependence of V_{DETECT}.

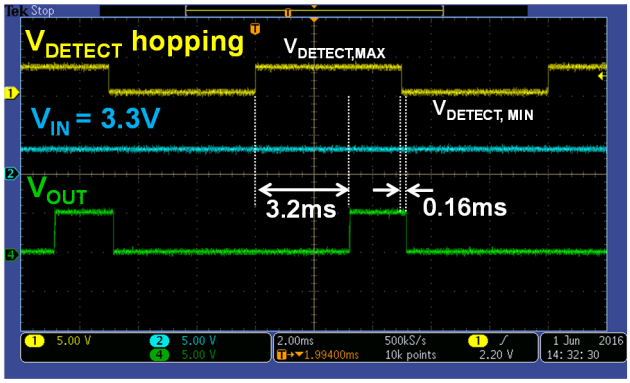

Fig. 14. Measured waveforms of V_{DETECT} hopping.

TABLE I Comparison with Previous Voltage Detectors

		[7] TPS3839	[2] AP4400A	[8] VLSI'12	[3] ESSCIRC'15	This work
CMOS process		N/A	N/A	180nm	250nm	250nm
Detection voltage	Programmability	No	No	No	Yes	Yes
	Max	4.38V	4.2V	3.58V (Fixed)	0.85V	4.67V
	Min	0.9V	2.0V		0.52V	1.88V
	Range	3.48V	2.2V		0.33V	2.79V
	Number of Steps	9	23	1	21	56
	Uniform step	No	Yes (100mV step)		No	Yes (50mV step)
Power (25°C)		180nW @1.2V	68nW @3.4V	286pW @3.6V	248pW @1.0V	13nW @3.5V
Temperature coefficient of V_{DETECT}		0.055mV/°C	0.75mV/°C	1.5mV/°C	0.11mV/°C	0.17mV/°C
Temperature range		-40°C to 85°C	-15°C to 85°C	0°C to 80°C	-20°C to 80°C	-20°C to 80°C