A Low-Power CMOS Crystal Oscillator Using a Stacked-Amplifier Architecture

Shunta Iguchi, *Member, IEEE*, Takayasu Sakurai, *Fellow, IEEE*, and Makoto Takamiya, *Senior Member, IEEE*

***Abstract*— This paper presents a low-power 39.25-MHz crystal oscillator with a new stacked-amplifier architecture achieving the smallest figure of merit (FoM) ever reported for a crystal oscillator for wireless communications. Theoretical analyses of the power consumption and the phase noise (PN) in the proposed stacked-amplifier architecture are newly provided to clarify the reason why the proposed stacked-amplifier architecture achieves the smallest FoM. Additionally, a new self-forward-body-biasing technique and flicker noise suppression technique are shown to reduce the minimum operational supply voltage ($V_{DD(MIN)}$) and the PN, respectively. The proposed 3.3-V, 39.25-MHz stacked-amplifier crystal oscillator fabricated in a 65-nm CMOS process exhibits the smallest FoM for a crystal oscillator of −248 dBc/Hz with a power consumption of 19 μW and PN of −139 dBc/Hz at 1-kHz offset frequency. The relative frequency errors among 11 samples at temperatures of −30 °C to 80 °C and for ±10% supply voltage variation are ±10.5 ppm and ±0.12 ppm, respectively. The long-term frequency error is −0.98 ppm in the first year (=365 days).**

***Index Terms*— CMOS, crystal oscillator, low noise, low power, quartz crystal, stacked-amplifier architecture.**

I. Introduction

CRYSTAL oscillators have undergone revolutionary decades every 30–40 years since their invention by Nicolson [1] and Cady [2] in the 1920s. Many technical challenges to reduce the aging effect [3] around World War II in the 1940s–50s and to achieve low-power operation for wristwatches in the 1970s–80s [4], [5] were overcome owing to the huge demand for crystal oscillators. In the 2020s, the Internet of Things (IoT) [6] is a promising application to provide the huge demand for crystal oscillators because it requires a huge capacity for wireless communications. The low-power and low-noise operation of crystal oscillators is the most fundamental requirement for energy-efficient wireless communications (e.g., Bluetooth with low energy (BLE) [7]) in IoT applications. The tradeoff between the power consumption (P_{dc})[1] and the single-sideband phase noise (PN) in oscillator circuits can be evaluated using the following figure of merit (FoM) [8] with the unit of dBc/Hz:

$$\mathrm{FoM} = \mathrm{PN} - 20\log_{10}(f_{OSC}/f_{OFFSET}) + 10\log_{10}(P_{dc}) \quad (1)$$

where f_{OSC} is the oscillation frequency, f_{OFFSET} is the offset frequency from f_{OSC}, and the unit of PN is dBc/Hz. For the low-power and low-noise operation of oscillator circuits, circuit designers should aim to achieve a smaller FoM than that in conventional studies.

This paper reports a low-power and low-noise crystal oscillator with the smallest FoM ever reported for a crystal oscillator. In Section II, the concept of a stacked-amplifier architecture [9] and theoretical analyses of P_{dc} and PN in the stacked-amplifier architecture are newly presented to clarify its advantages for reducing FoM, thereby demonstrating the low-power and low-noise operation of the crystal oscillator. In Section III, the detailed circuit designs with the stacked-amplifier architecture are shown. Additionally, a new self-forward-body-biasing technique and flicker noise suppression technique are demonstrated that, respectively, reduce P_{dc} and PN for the proposed crystal oscillator. To verify the low-power, low-noise, and reliable operation of the proposed crystal oscillator, measurement results are given in Section IV. Finally, conclusions are given in Section V.

II. Analysis of Stacked-Amplifier Architecture

To clarify the advantages of the stacked-amplifier architecture for achieving low-power and low-noise operation, theoretical analyses of P_{dc} and PN are newly presented in this section. The analyses clarify the reason why the stacked-amplifier architecture can achieve the smallest FoM.

A. Power Reduction With Stacked-Amplifier Architecture

The power consumption in many crystal oscillator architectures [5], [10]–[16] is mainly determined by a negative resistance generator consisting of an amplifier circuit (e.g., an inverter amplifier and differential amplifier). Several techniques using an energy-efficient amplifier operating in the weak-inversion region (overdrive voltage: $V_{OV} < 0$) [5], [16], an intermittent amplifier [17], [18], and a pulsed driver [19], [20] have been reported for achieving low-power operation. However, these conventional techniques targeted a low-frequency (e.g., 32.768 kHz) real-time-clock (RTC) generator because PN in an RTC does not make significant problems as a system clock. The temperature dependence and aging effect of the oscillation frequency are the major problems in such applications. On the other hand, high-frequency (>10 MHz) crystal oscillators for wireless communications require a low PN because the PN in a crystal oscillator and phase-locked loop (PLL)[2] degrades the

Manuscript received February 17, 2017; revised April 30, 2017 and June 24, 2017; accepted August 14, 2017. Date of publication September 13, 2017; date of current version October 23, 2017. This work was partly supported by STARC. This paper was approved by Associate Editor Seonghwan Cho. *(Corresponding author: Shunta Iguchi.)*

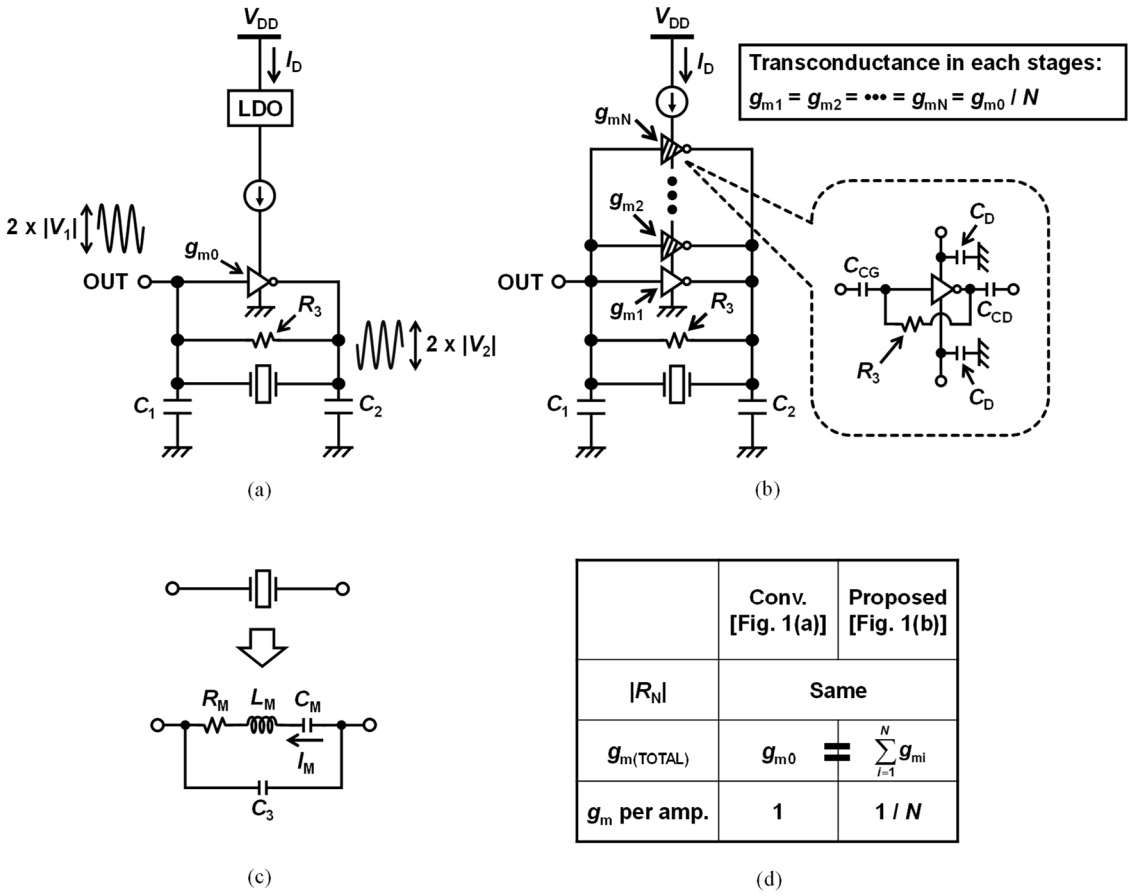
The authors are with The University of Tokyo, Tokyo 153-8505, Japan (e-mail: shunta.iguchi.jp@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2017.2743174

[1] Note that P_{dc} in (1) must be calculated in the unit of milliwatt for consistency with the unit of dBc/Hz in (1).

[2] The PN in the crystal oscillator is amplified by the frequency multiplication ratio in the PLL. In a case of upconversion from 24 MHz to 2.4 GHz, the PN in the PLL is 40 dB (=$20\times\log_{10}(100)$) larger than that in the crystal oscillator.



	Conv. [Fig. 1(a)]	Proposed [Fig. 1(b)]
$\|R_N\|$	Same	
$g_{m(TOTAL)}$	g_{m0} =	$\sum_{i=1}^{N} g_{mi}$
g_m per amp.	1	1 / N

Fig. 1. Schematics of (a) conventional one-stage CMOS Pierce crystal oscillator, (b) proposed stacked-amplifier crystal oscillator, (c) equivalent circuit of the quartz crystal, and (d) table comparing properties of a conventional oscillator and the proposed oscillator.

sensitivity of wireless receivers owing to adjacent-channel interference.

To achieve low-power and low-noise operation, the stacked-amplifier architecture was proposed in [9]. Fig. 1(a)–(d) shows the schematics of a conventional one-stage CMOS Pierce crystal oscillator, a proposed stacked-amplifier crystal oscillator with N-stages stacked amplifiers, an equivalent circuit of the quartz crystal, and a table comparing the properties of a conventional oscillator and the proposed oscillator, respectively. C_1 is the gate-to-ground capacitor, C_2 is the drain-to-ground capacitor, C_3 is the parallel parasitic capacitor in the quartz crystal, and R_3 is the feedback resistor. C_M, L_M, and R_M are the motional capacitor, inductor, and resistor in the quartz crystal, respectively. The current waveform (I_M) in the node containing C_M, L_M, and R_M is expressed as $|I_M| \times \cos(\omega t)$, where $|I_M|$ is the amplitude of the current swing, ω is the angular frequency, and t is the time. The inverter amplifiers in Fig. 1(a) and (b) configure the negative resistance (R_N) to provide energy to the resonator of the quartz crystal. In many cases, the amplifiers are biased by a current source with a bias current (I_D) to reduce the sensitivity to process, voltage, and temperature (PVT) variations. The inverter amplifiers except for that in the lowest stage ($N = 1$) in Fig. 1(b) consist of a CMOS inverter, a decoupling capacitor (C_D), and two coupling capacitors at the gate (C_{CG}) and drain (C_{CD}). $|V_1|$ and $|V_2|$ are the amplitudes of the voltage swing at the gate and drain of the inverter amplifier, respectively. Assuming that $C_1 = C_2$ and $g_{m(TOTAL)} \ll \omega_{OSC}$ for simplicity, the equivalent R_N [5], [21] in Fig. 1(a) and (b) is approximated as

$$R_N = -\frac{g_{m(TOTAL)} C_1 C_2}{g_{m(TOTAL)}^2 C_3^2 + \omega_{OSC}^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2} \approx -\frac{g_{m(TOTAL)}}{\omega_{OSC}^2 (C_1 + 2C_3)^2} \quad (2)$$

where $g_{m(TOTAL)}$ is the equivalent transconductance of the inverter amplifiers and ω_{OSC} is the angular frequency of f_{OSC}. In the initial state, the absolute value of R_N ($|R_N|$) is set to approximately five times larger than R_M to ensure reliable and quick startup [22]. In the steady state, $|R_N|$ settles down to R_M owing to the nonlinearity of the amplifiers. This indicates that the characteristic of the quartz crystal ($=R_M$) is the fundamental limitation in minimizing the value of $g_{m(TOTAL)}$ and the corresponding power consumption of the crystal oscillators. In Fig. 1(a), $g_{m(TOTAL)}$ is simply given by the transconductance (g_{m0}) in an inverter amplifier. On the other hand, $g_{m(TOTAL)}$ in Fig. 1(b) is given by

$$g_{m(TOTAL)} = \sum_{i=1}^{N} g_{mi} = g_{m1} + g_{m2} + \cdots + g_{mN} \quad (3)$$

where g_{mN} is the transconductance of the inverter amplifiers in the Nth stage. When the impedances of C_D, C_{CG}, and C_{CD} are approximated to zero at f_{OSC}, the stacked amplifiers in Fig. 1(b) are equivalent to a transconductance amplifier with a transconductance of $g_{m(TOTAL)}$, because all the stacked amplifiers are virtually connected in parallel at f_{OSC}. The minimum transconductance of each inverter amplifier in the proposed stacked-amplifier crystal oscillator is N times smaller than that of the conventional one-stage CMOS Pierce crystal oscillator. The smaller transconductance in the proposed architecture makes it possible to reduce P_{dc} compared with that of conventional crystal oscillators. This discussion is summarized in Fig. 1(d), which clarifies the difference between the conventional architecture and the proposed stacked-amplifier architecture.

Subsequently, the power consumption of the stacked-amplifier crystal oscillator is analytically derived using ideal long-channel models [23] to verify the power reduction by the proposed architecture. The theoretical analyses are performed using fixed-size amplifiers because the aim of this paper is to design a low-power crystal oscillator for low-energy wireless communications (e.g., BLE). Such low-power operation is a more essential requirement than small-area implementation for this application. For simplicity, it is assumed that the transconductances (g_{mN} and g_{mP}) and threshold voltages (V_{THN} and V_{THP}) of the NMOS and PMOS transistors are the same without random variations. The lengths of the NMOS (L_N) and PMOS (L_P) transistors are the same, and their widths (W_N and W_P) are varied as $n \times W_N = W_P$ to satisfy the condition $g_{mN} = g_{mP}$, where n is the relative size ratio of W_P compared with W_N.

When the sizes of the inverter amplifiers in each stage are fixed for the stacked-amplifier architecture with N-stages stacked amplifiers, V_{OV} is scaled down by a factor of N. Then, the relationship between g_{mN}, g_{mP}, $g_{m(TOTAL)}$, I_D, and N is given as

$$g_{mN} = g_{mP} = \frac{g_{m(TOTAL)}}{2N} = \sqrt{2\mu_N C_{OX}(W_N/L_N)I_D} \quad (4)$$

where μ_N is the carrier mobility in the NMOS transistor and C_{OX} is the unit capacitance of the gate oxide. Substituting (4) into (2), I_D in the case of N-stages stacked amplifiers is derived as

$$I_D = \frac{\omega_{OSC}^4 |R_N|^2 (C_1 + 2C_3)^4}{8N^2 \mu_N C_{OX}(W_N/L_N)} \propto \frac{1}{N^2}. \quad (5)$$

Equation (5) clarifies that I_D and P_{dc} are proportional to $1/N^2$. The power consumption of the proposed stacked-amplifier architecture is 16 times smaller than that of the conventional one-stage CMOS Pierce crystal oscillator when four-stage stacked amplifiers are available. To verify the consistency of the derived equation, the simulated N dependence of I_D is shown in Fig. 2. The simulated results show that the power is reduced by a factor of N^2 within a relative error of 42%. The simulated I_D is reduced by 91% from 65.4 μA ($N = 1$) to 5.8 μA ($N = 4$). It is verified that the proposed stacked-amplifier architecture can reduce P_{dc} by increasing N. Note that the maximum value of N is limited by the minimum operational supply voltage ($V_{DD(MIN)}$) and the design specification for PVT variations.

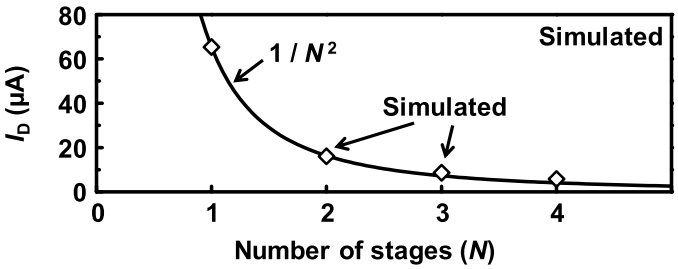


Fig. 2. Simulated N dependence of I_D at $|R_N|$ of 50 Ω. The solid line shows a function of $1/N^2$ fit using the value of I_D at $N = 1$ to verify the consistency of the proportional relationship with the factor of $1/N^2$.

$V_{DD(MIN)}$ in the stacked-amplifier architecture is higher than that in the conventional one-stage Pierce crystal oscillator; however, the higher $V_{DD(MIN)}$ is not a critical problem in many cases because crystal oscillators are often powered by I/O voltage (e.g., 3.3 V). There are several reasons why crystal oscillators utilize I/O voltage. Firstly, crystal oscillators need to start up first and provide the clock for all sub-blocks in a system-on-chip (SoC). Second, crystal oscillators are often designed as an I/O cell for small-area implementation with electrostatic discharge protection circuits and I/O pads. Third, the power supply of a crystal oscillator should be isolated from the core supply voltage because the harmonics of the oscillation frequency in the crystal oscillator propagate to noise-sensitive circuits (e.g., wireless receivers) through the power supply.

In contrast, the maximum voltage swing in a crystal oscillator should be smaller than a certain voltage (e.g., 0.8 V) to minimize the long-term frequency variation (e.g., 1 ppm/year). The large difference between the supply voltage and oscillation amplitude (e.g., 3.3 V − 0.8 V = 2.5 V) is the fundamental limitation in reducing the power consumption. This large voltage difference has been decreased by employing a resistive divider consisting of a low-dropout (LDO) regulator and a current source in conventional approaches [13], [16]. The power loss in the resistive divider is not negligible in low-power applications. On the other hand, dc–dc converters (e.g., Buck converters) are not available for low-noise crystal oscillator designs because the output noise in a dc–dc converter is significantly larger than that in an LDO. Additionally, the overheads of the area and cost of a capacitor, inductor, and I/O pads are not feasible for low-cost IoT applications. The advantage of the proposed stacked-amplifier architecture is that it utilizes the wasted voltage drop to increase $g_{m(TOTAL)}$. The proposed architecture reduces the total power consumption, including the voltage drop in the LDO and current source, compared with conventional approaches using one-stage Pierce crystal oscillators.

B. Phase Noise in Stacked-Amplifier Architecture

The FoM in oscillator circuits is calculated from P_{dc} and PN using (1). A detailed analysis of the noise in the proposed stacked-amplifier architecture is also important to clarify its

advantages compared with conventional architectures. In crystal oscillator design, PN for f_{OFFSET} of 1–10 kHz should be reduced to as low as possible because it is difficult to suppress PN in this frequency range by using a loop filter in a PLL. This section provides a theoretical analysis of the PN due to flicker noise because the contribution of flicker noise is considerably larger than that of thermal noise in this frequency range. The N dependence of PN is analytically discussed using linear time-varying (LTV) theory [24], [25].

The spectrum of PN at a low f_{OFFSET} ($=1/f^3$ region) is mainly determined by the flicker noise in transistors and the upconversion effect due to the impulse response in LTV systems. In accordance with LTV theory and a theoretical analysis [26], PN for a Pierce crystal oscillator in the $1/f^3$ region ($PN_{1/\mathrm{f3}}$) is given as

$$PN_{1/\mathrm{f3}} = \frac{\Gamma_{\mathrm{dc}}^2 I_{\mathrm{D\_n(rms)}}^2}{2(C_2|V_2|)^2\omega_{\mathrm{OFFSET}}^2}\left(\frac{C_{\mathrm{M}}}{C_2}\right)^2 \tag{6}$$

where Γ_{dc} is the direct current (dc) value of the effective impulse sensitivity function for a sinusoidal voltage of $|V_2| \times \sin(\omega t)$ and $I_{\mathrm{D\_n(rms)}}$ is the root-mean-square (RMS) value of the noise current in I_{D} for a 1-Hz bandwidth. The angular frequency of f_{OFFSET} is denoted as ω_{OFFSET}. Equation (6) can be applied[3] to all types of Pierce crystal oscillator including the one-stage CMOS Pierce crystal oscillator and the stacked-amplifier crystal oscillator shown in Fig. 1. $I_{\mathrm{D\_n(rms)}}$ is one of a few controllable parameters for circuit designers. PN in the $1/f^3$ region should be reduced by ensuring a small $I_{\mathrm{D\_n(rms)}}$.

To analyze the N dependence of PN in the $1/f^3$ region; at first, $I_{\mathrm{D\_n(rms)}}$ for different numbers of stacked amplifiers is derived because $I_{\mathrm{D\_n(rms)}}$ can easily be calculated using a small-signal approximation. According to [26], the square of the equivalent flicker noise voltage ($V_{\mathrm{1/f\_n(rms)}}^2$) at the gate of a transistor is given as

$$V_{\mathrm{1/f\_n(rms)}}^2 = \frac{K}{\omega L W} \tag{7}$$

where K is the flicker noise voltage constant, L and W are the length and width of the transistors, respectively. In the following discussion, the values of K in NMOS and PMOS transistors are denoted as K_{N} and K_{P}, respectively. $I_{\mathrm{D\_n(rms)}}^2$ with the N-stages stacked amplifiers is derived as

$$I_{\mathrm{D\_n(rms)}}^2 = \frac{(nK_{\mathrm{N}} + K_{\mathrm{P}})g_{\mathrm{m(TOTAL)}}^2}{16n\omega N^3 L_{\mathrm{N}} W_{\mathrm{N}}} \propto \frac{1}{N^3}. \tag{8}$$

The detailed derivation of (8) is given in the Appendix. Equation (8) clarifies that $I_{\mathrm{D\_n(rms)}}^2$ is reduced by a factor of N^3 when N-stages stacked amplifiers are used for the proposed stacked-amplifier architecture. A comparison between a theoretical calculation using (8) and simulation results is shown in Fig. 3. The calculated results match to the simulation results within a relative error of 21%. The small error verifies that (8) is consistent with the simulation results. For the calculations using (8), K_{N} and K_{P} are extracted by SPICE simulation because they depend on the overdrive voltage of the transistors [27]. The N dependences of K_{N} and K_{P} are not incorporated in (8) for simplicity. It is concluded that the proposed stacked-amplifier architecture can reduce both P_{dc} and $I_{\mathrm{D\_n(rms)}}^2$ in the $1/f^3$ region by increasing N.

[3]Note that the theoretical calculation of Γ_{dc} is complicated even in the ideal case assuming sinusoidal voltage waveforms. For simplicity, this study assumes that Γ_{dc} is independent of N.

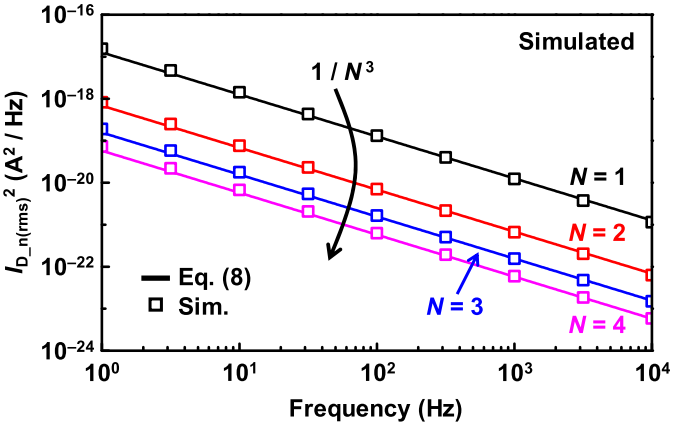


Fig. 3. Simulated frequency dependences of $I_{\mathrm{D\_n(rms)}}^2$ with $|R_{\mathrm{N}}|$ of 50 Ω at $N = 1, 2, 3$, and 4. Solid lines show the results calculated using (8). The simulated and calculated results verify that the flicker noise in I_{D} is inversely proportional to N^3.

To calculate PN, $I_{\mathrm{D\_n(rms)}}$ should be normalized by $|V_2|$ ($\approx|V_1|$). The accurate estimation of $|V_2|$ is difficult because the oscillation amplitude is determined by the nonlinearity in the inverter amplifiers. Experimentally, $|V_2|$ is approximately proportional to $N^{-\beta}$ (e.g., $\beta = 0.73$ when $N = 2$ and $\beta = 0.56$ when $N = 4$). To simplify the discussion, it is assumed that $|V_2|$ is inversely proportional to N because the stacked amplifiers are considered as an N-stages voltage divider. The maximum oscillation swing is limited by the equivalent supply voltage ($\approx V_{\mathrm{DD}}/N$) in each stage because the stacked amplifiers operate as CMOS inverters in the steady state. Note that this assumption is a pessimistic approximation compared with the experimental results. Then, N dependence of the PN is obtained from (6) as

$$PN_{1/\mathrm{f3}} \propto \frac{I_{\mathrm{D\_n(rms)}}^2}{|V_2|^2} \propto \frac{1}{N}. \tag{9}$$

Equation (9) shows that PN in the $1/f^3$ region is reduced by the proposed stacked-amplifier architecture. Finally, the N dependence of FoM is also easily derived using (5) and (9). It is concluded that the proposed stacked-amplifier architecture can reduce FoM by $10 \times \log_{10}(N^3)$ dB, thereby achieving the smallest ever reported value of FoM for crystal oscillators.

III. Circuit Implementation

Fig. 4(a) and (b) shows the schematics of a crystal oscillator with the proposed stacked-amplifier architecture for $N = 4$ and an amplifier cell with a proposed self-forward-body-biasing technique, respectively. To minimize the power consumption, 1.2-V core transistors and 3.3-V I/O transistors are used in the deep n-well process. The proposed self-forward-body-biasing technique reduces the threshold voltage (V_{TH}) of transistors in the stacked amplifiers for

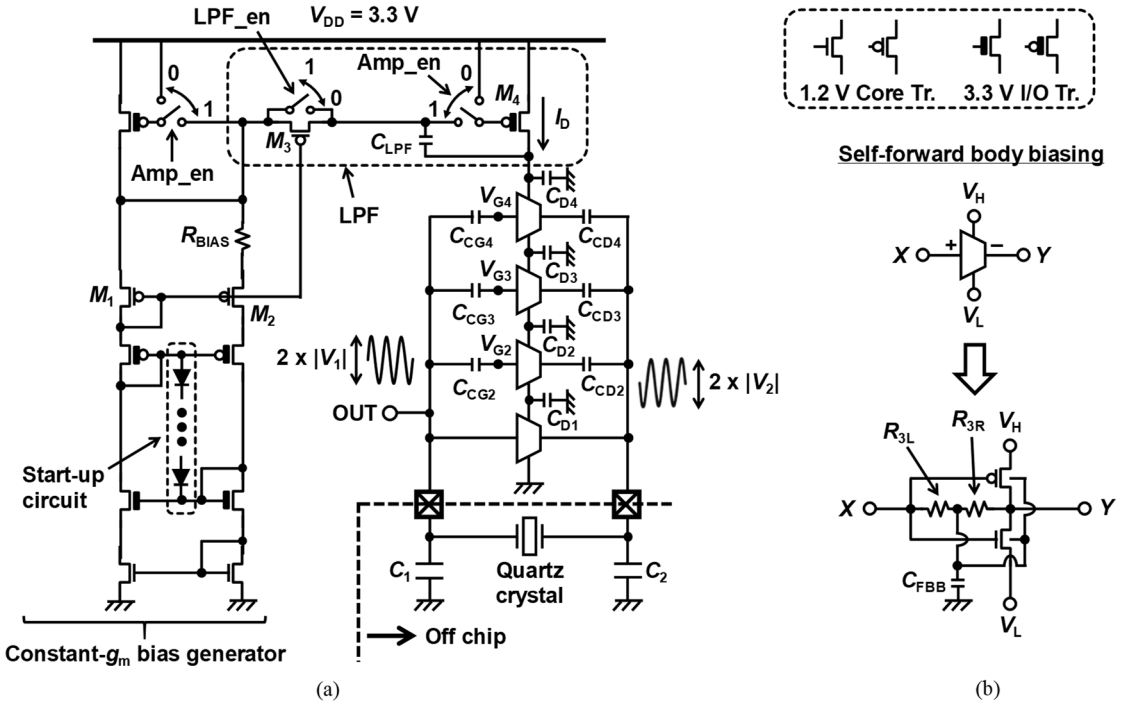


Fig. 4. Schematics of (a) crystal oscillator with the proposed stacked-amplifier architecture and (b) amplifier cell with the proposed self-forward-body-biasing technique.

TABLE I
DESIGN PARAMETERS

C_1, C_2	12 pF, 15 pF
C_{CD2}, C_{CD3}, C_{CD4}	1.4 pF, 1.4 pF, 1.4 pF
C_{CG2}, C_{CG3}, C_{CG4}	1.4 pF, 1.4 pF, 1.4 pF
C_{D1}, C_{D2}, C_{D3}, C_{D4}	43 pF, 43 pF, 43 pF, 12 pF
C_{FBB}, C_{LPF}	5.8 pF, 58 pF
R_{3L}, R_{3R}, R_{BIAS}	150 kΩ, 150 kΩ, 80 kΩ

low-voltage operation. C_{FBB}, R_{3L}, and R_{3R} are used to configure the low-pass filter (LPF) to provide the forward body bias voltage on the substrate in the NMOS and PMOS transistors. To compensate the variation in $|R_N|$ due to the PVT variations, a constant-g_m biasing technique is used for the proposed stacked-amplifier architecture. An area-efficient LPF is also added to suppress the flicker noise in the constant-g_m bias generator. The values of all the capacitors and resistors in Fig. 4 are summarized in Table I.

The stacked amplifiers are equivalent to a parallel connection at oscillation frequency. To reduce the power loss owing to the phase mismatch, the phase differences among the stacked amplifiers should be small. This means that the cutoff frequency (f_{HPF}) of a high-pass filter (HPF) consisting of C_{CG} and the input resistance of the stacked amplifiers should be lower than f_{OSC}. The simulated voltage waveforms of the four stages of the stacked amplifiers are shown in Fig. 5 to verify the small phase difference of 1.2° among the stages. The simulation results do not include any parasitic and device mismatches; however, non-ideal effects do not have a critical effect on the phase mismatch when f_{HPF} is lower than f_{OSC}. The simulated phase difference of 1.2° in Fig. 5 shows that f_{HPF} is approximately 50 times lower than f_{OSC}. When 10% random mismatches are assumed among the stages, the mismatches generate a phase error of 0.1° (=$\tan^{-1}$ $(0.1 \times 1/50)$). The calculated small phase error of 0.1° verifies that the proposed architecture is insensitive to parasitic and device mismatches. The voltage drop in each stage is also estimated

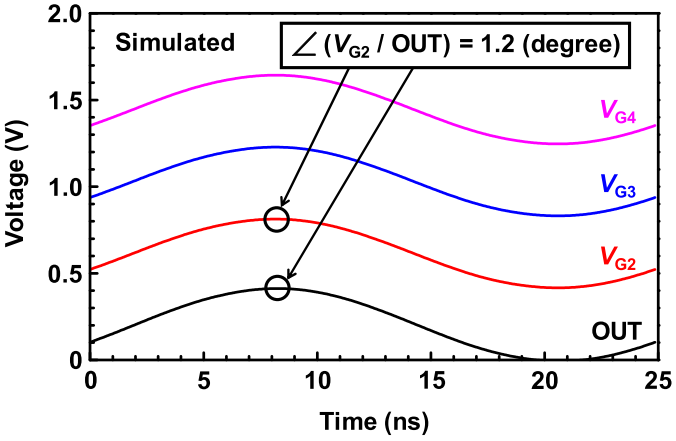


Fig. 5. Simulated voltage waveforms at OUT, V_{G2}, V_{G3}, and V_{G4} in the proposed stacked-amplifier crystal oscillator. The waveform at OUT is delayed by 83 ps (=1.2°) compared with that at V_{G2}. The phase differences between V_{G2}, V_{G3}, and V_{G4} are approximately zero owing to the symmetrical configurations in the second to fourth stages.

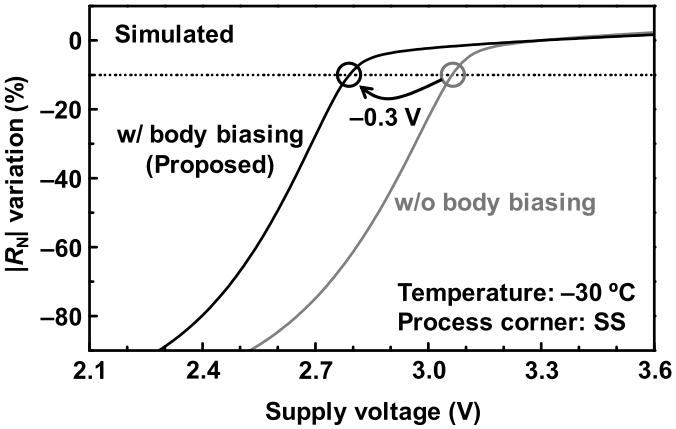


Fig. 6. Simulated relative variation of $|R_N|$ with and without the proposed self-forward-body-biasing technique in the worst case (=low temperature and slow corner). $V_{DD(MIN)}$ with the proposed technique is 0.3 V lower than that without the proposed technique.

from the amplitude of the waveforms in Fig. 5. The voltage drops across the stacked amplifiers at $N = 1, 2, 3$, and 4 are 419, 397, 397, and 396 mV, respectively. It is thus verified that the stacked amplifiers in each stage equally provide the transconductance.

Fig. 6 shows the simulated relative variation of $|R_N|$ with and without the proposed self-forward-body-biasing technique. As discussed above, the proposed stacked-amplifier architecture reduces P_{dc} and PN; however, $V_{DD(MIN)}$ is increased in proportional to N. $V_{DD(MIN)}$ is the fundamental limitation in maximizing the value of N in the proposed stacked-amplifier architecture. To reduce $V_{DD(MIN)}$, specifically in the worst case of a low temperature and slow corner, a new self-forward-body-biasing technique is demonstrated in this paper. This technique reduces V_{TH} in the NMOS and PMOS transistors by the body effect. Using the self-forward-body-biasing technique, $V_{DD(MIN)}$ in the worst case is reduced by 0.3 V compared with that in a stacked-amplifier crystal oscillator without the proposed technique. Without the proposed technique in Fig. 6, the substrates of the NMOS and PMOS transistors are connected to the sources in order to prevent the body effect. The reduced $V_{DD(MIN)}$ makes it possible to use the four-stages stacked amplifiers at the supply voltage (V_{DD}) of 3.3 V. Note that the leakage current is not increased by the self-forward-body-biasing technique because the leakage current is limited by a 3.3-V I/O transistor (M_4). V_{TH} in an I/O transistor is approximately two times higher than that in a core transistor. This indicates that the off-resistance in the stacked amplifiers is mainly determined by the I/O transistor.

The proposed self-forward-body-biasing technique reduces the variation of $|R_N|$ in the worst case; however, it does not reduce the temperature and supply voltage dependences of $|R_N|$. To compensate the PVT variations of $|R_N|$ in the stacked amplifiers, a constant-g_m bias generator is implemented. Fig. 7 shows the simulated relative variation of $|R_N|$ with and without the constant-g_m bias generator. Using the constant-g_m biasing technique, the supply voltage and temperature dependences of $|R_N|$ are respectively reduced by 89% ($\pm 24\% \rightarrow \pm 3\%$) and 45% ($\pm 21\% \rightarrow \pm 12\%$) compared with those without the constant-g_m bias generator.

The constant-g_m biasing technique increases PN owing to the flicker noise in the constant-g_m bias generator, although the technique can reduce the PVT variation of $|R_N|$. To reduce the flicker noise from the constant-g_m bias generator, an LPF using an active resistor (M_3) and an amplified capacitor (C_{LPF}) based on the Miller effect is developed for the low-noise operation of the crystal oscillator. The cutoff frequency of the LPF (f_{LPF}) is given by

$$f_{LPF} = \frac{1}{2\pi (1 + A_{LPF}) R_{ON3} C_{LPF}} \tag{10}$$

where A_{LPF} is the voltage gain of the common source amplifier of M_4 and R_{ON3} is the on-resistance of M_3 in the linear region. To suppress the flicker noise around 1 kHz, f_{LPF} should be smaller than 100 Hz. In this paper, R_{ON3} of 27 MΩ is implemented with a small area of 1800 μm^2 because R_{BIAS} is amplified by the size ratio of M_1 and M_3 as

$$R_{ON3} \propto R_{BIAS} \times (L_{M3} W_{M1})/(L_{M1} W_{M3}). \tag{11}$$

The areas of C_{LPF} and R_{ON3} with the amplified capacitor and active resistor are approximately 10 times and 30 times[4] smaller than those with only passive components, respectively. Fig. 8 shows the simulated frequency dependences of $I^2_{D\_n(rms)}$ with and without the area-efficient LPF. The simulation result verifies that the area-efficient LPF suppresses the flicker noise of the constant-g_m bias generator by 45 dB at 1 kHz.

IV. Measurement Results and Discussion

To demonstrate the low-power and low-noise operation of the proposed stacked-amplifier architecture, a crystal oscillator is fabricated in a 65-nm CMOS process. Fig. 9 shows the die micrograph of the fabricated stacked-amplifier crystal oscillator with a core area of 420 μm × 210 μm. The large area of C_{D1}, C_{D2}, C_{D3}, and C_{D4} is a disadvantage of the

[4]Assumed that the poly resistor has a sheet resistance of 500 Ω and a width of 1 μm.

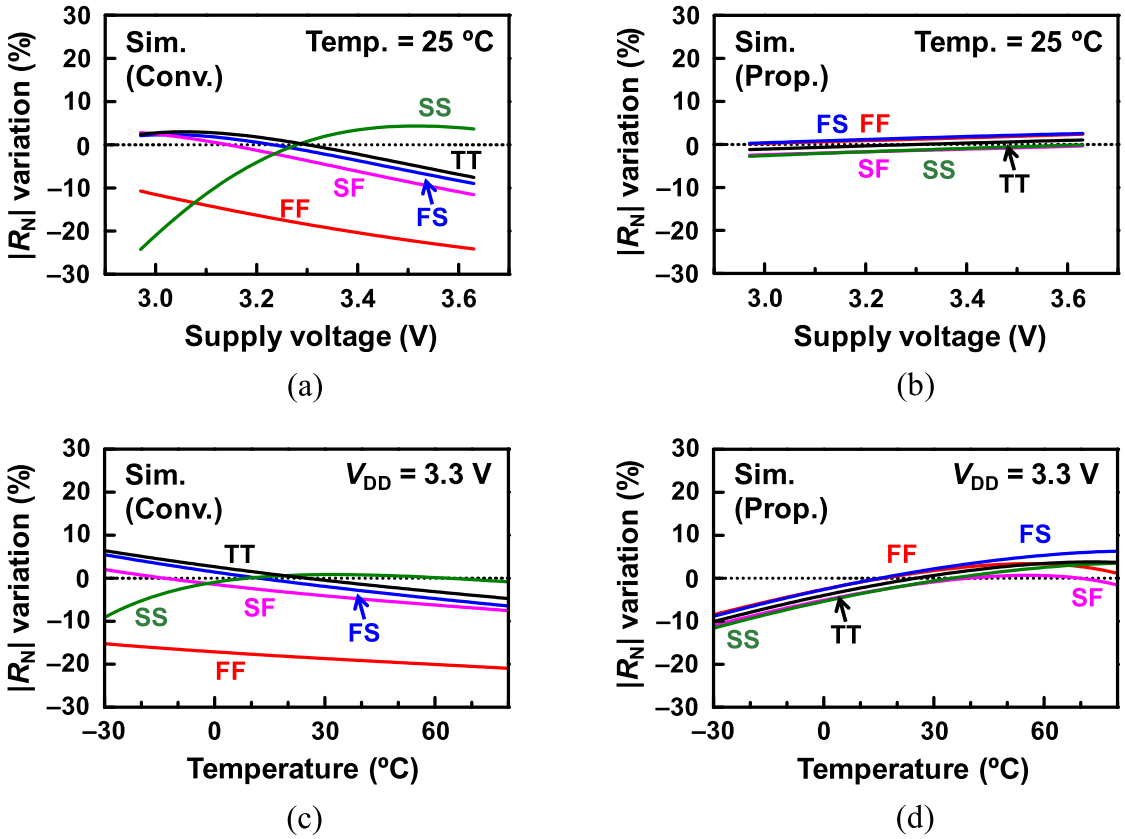


Fig. 7. Simulated relative variation of $|R_N|$ with and without the constant-g_m bias generator. (a) and (c) Supply voltage and temperature dependences of $|R_N|$ without the bias generator, respectively. (b) and (d) Supply voltage and temperature dependences of $|R_N|$ with the bias generator, respectively.

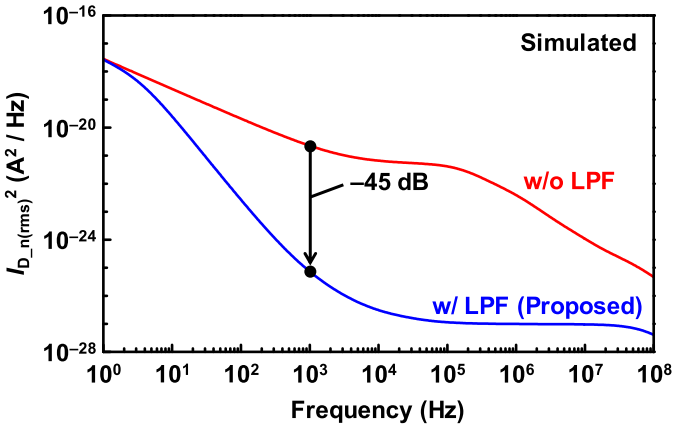


Fig. 8. Simulated frequency dependences of $I^2_{D\_n(rms)}$ at $|R_N|$ of 50 Ω with and without the proposed LPF. To clarify the noise suppression in the LPF, only the noise generated by the constant-g_m bias generator is included in the simulation. The noise current at 1 kHz with the proposed LPF is 45 dB smaller than that without the LPF.

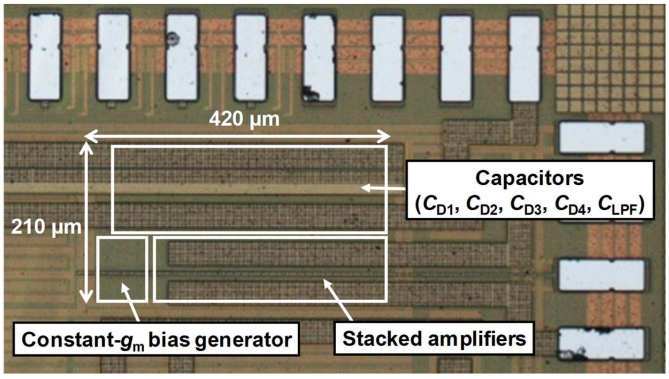


Fig. 9. Die micrograph of test chip fabricated in 65-nm CMOS process.

proposed stacked-amplifier architecture; however, the minimum die area of the SoC will be limited by the I/O pins in many cases. Additionally, the total area of 88 200 μm^2 is not larger than that in conventional works [13], [28]. The area overhead should be acceptable in most applications. In this paper, the characteristic of the quartz crystal is the same as that in [22] with a load capacitance of 8 pF. To achieve an oscillation frequency of 39.25 MHz, C_1 of 12 pF, and C_2 of 15 pF are mounted on an FR4 PCB. The reason why C_1 is smaller than C_2 is to increase the oscillation amplitude at OUT [29].

Fig. 10 shows the measured PN with and without an LPF in the proposed stacked-amplifier crystal oscillator. By enabling the LPF, PN at 1 kHz offset frequency is reduced from −122 dBc/Hz to −139 dBc/Hz. The 17-dB noise reduction by the area-efficient LPF, consisting of an amplified capacitor and active resistor, clarifies that it successfully suppresses the flicker noise from the constant-g_m generator. On the other hand, PN at offset frequencies higher than 10 kHz is not reduced because the thermal noise in an output buffer is dominant in this frequency range. A buffer circuit is required

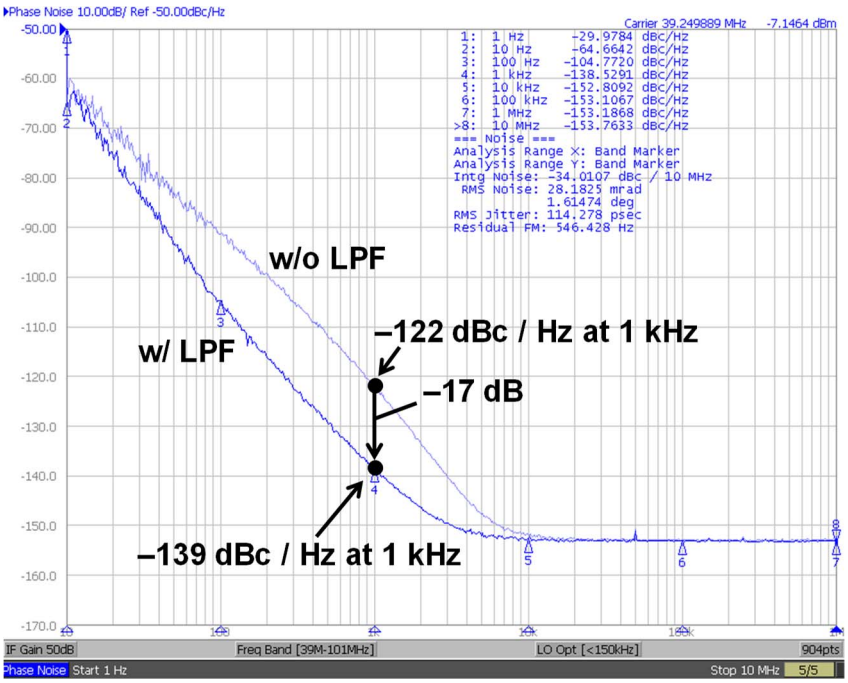


Fig. 10. Measured PN for the proposed stacked-amplifier crystal oscillator with and without the LPF. The PN at 1-kHz offset frequency is reduced by 17 dB when using the proposed active LPF.

to provide a squire wave with a rail-to-rail swing for other circuit blocks in integrated products. The power consumption of a buffer circuit significantly depends on the requirement of the PN in the systems because the PN in a high offset frequency (>100 kHz) is determined by the thermal noise in a buffer circuit. The specification of the PN in low-power and low-cost IoT applications would be 10–20 dB higher than that in high-speed wireless transceivers. For IoT applications, the power consumption in the buffer circuit will be comparable (e.g., 1–10 μA) to that in a core circuit. For the fair comparison of the proposed techniques in a core circuit, the power consumption in a buffer circuit is not included for the total power consumption because the power consumption highly depends on the requirement in applications (e.g., swing level and load impedance). Additionally, the dedicated buffer circuit consisting of a source follower and open-drain output in the test chip needs to drive an external load of 50 Ω in a measurement equipment (Keysight E5052B) for the low-noise PN measurement. Such a huge drivability for a 50-Ω load is not required for commercial integrated products.

The variation of f_{OSC} is the most important specification for the reference clock generator. To verify that the proposed techniques do not increase the variation of f_{OSC}, the temperature and supply voltage dependences of f_{OSC} for 11 samples are measured as shown in Figs. 11 and 12, respectively. Fig. 11(a) and (b) shows the measured temperature dependences of the absolute frequency variation and the relative frequency variation, respectively. The absolute and relative frequency variations at V_{DD} of 3.3 V in the temperature range of −30 °C to 80 °C are ±15.8 and ±10.5 ppm, respectively. The relative frequency variation with the same quartz crystal is ±5.5 ppm [22] in the temperature range of −10 °C to 60 °C. Note that each of the 11 samples are measured with a different

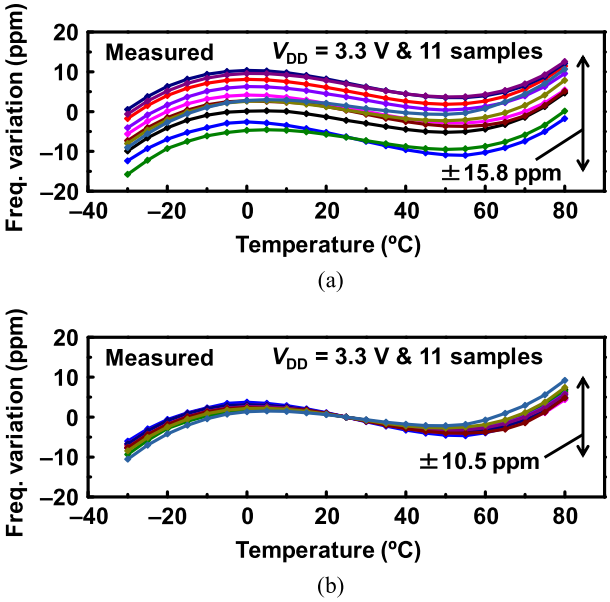


Fig. 11. Measured temperature dependences of (a) absolute frequency variation and (b) relative frequency variation for 11 samples.

PCB board. This indicates that the absolute frequency variations in Figs. 11 and 12 include the variations of the circuit, off-chip components, PCB, and quartz crystal. The frequency variation of the 39.25-MHz quartz crystal (DSX221G) is ±20 ppm at a temperature of 25 °C ± 3 °C. The absolute frequency variations in Figs. 11 and 12 are considered to be mainly determined by the variation of the quartz crystals. In the same temperature range, the measured frequency variation in the proposed crystal oscillator is comparable to that in the conventional one-stage CMOS Pierce

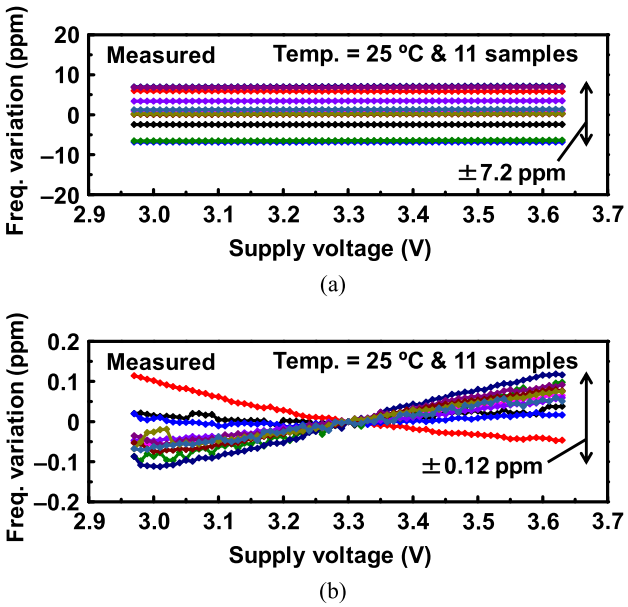


Fig. 12. Measured supply voltage dependences of (a) absolute frequency variation and (b) relative frequency variation for 11 samples.

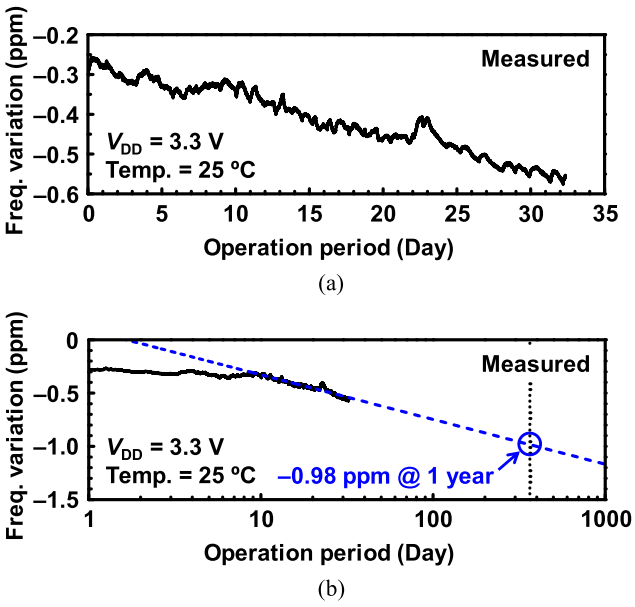


Fig. 13. Measured time dependences of the frequency variation: (a) linear–linear plot and (b) log–linear plot. The predicted frequency variation in the first year (=365 days) is −0.98 ppm.

crystal oscillator. This verifies that the proposed techniques do not increase the frequency variation.

In the same way, the measured supply voltage dependences of the absolute frequency variation and the relative frequency variation are shown in Figs. 12(a) and (b), respectively. The absolute and relative frequency variations at a temperature of 25 °C at V_{DD} of 3.3 V ±10% are ±7.2 and ±0.12 ppm, respectively. The supply voltage dependence of the frequency variation in the proposed crystal oscillator is also well matched to the relative frequency variation of ±0.6 ppm [22] in the conventional oscillator with V_{DD} of 1.5 V ± 20%. These measured results in Figs. 11 and 12 clearly show that the proposed crystal oscillator can be used as a reference clock generator for low-energy wireless communications.

Fig. 13(a) and (b) shows the measured time dependence of the frequency variation as a linear–linear plot and a log–linear plot, respectively. To evaluate the aging effect in the proposed crystal oscillator, f_{OSC} is measured for 32 days at a temperature of 25 °C and V_{DD} of 3.3 V. The measured long-term frequency variation for 32 days is −0.57 ppm and the predicted frequency variation in the first year (=365 days) is −0.98 ppm. The long-term frequency variation is derived by extrapolation of the logarithmic function [30] using the data from 10 to 32 days. The data until 10 days are excluded from the extrapolation because f_{OSC} is unstable in the first several days. The measured long-term frequency variation of −0.98 ppm/year is comparable to that of conventional crystal oscillators (e.g., 2.5 ppm/year [31]).

The Allan deviation is also used to evaluate the time-domain frequency stability of oscillators. To evaluate the frequency stability of the proposed crystal oscillator, the Allan deviation (σ_y) is calculated from the measured PN in the offset frequency of 1 Hz to 10 MHz using [32]

$$\sigma_y = \frac{2}{\pi \tau f_{OSC}} \sqrt{\int_0^{f_H} 10^{PN/10} \times \sin^4(\pi \tau f) df} \qquad (12)$$

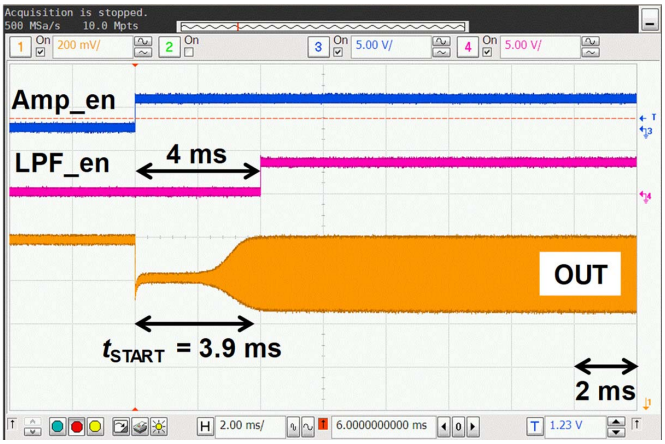


Fig. 14. Measured start-up waveforms.

where f_H is the upper cutoff frequency of the measuring system and τ is the observation time. The calculated Allan deviations at $\tau = 0.1$ and 1 s are 1.1×10^{-9} and 1.7×10^{-10}, respectively.

The measured start-up waveforms of the proposed crystal oscillator are shown in Fig. 14. To prevent a long start-up time (t_{START}) owing to the LPF used for flicker noise suppression, the LPF is disabled during the startup. When LPF_en is enabled after 4 ms from Amp_en, the measured start-up time is 3.9 ms. The start-up time and energy are also important specifications in IoT applications. Several quick-startup and energy-reduction techniques have been demonstrated recently [22], [33], [34]. These techniques can be applicable to the proposed architecture because the stacked-amplifier architecture is equivalent to the Pierce crystal oscillator. Using these techniques, the start-up time can easily be reduced to less than 1 ms. The proposed architecture is able to support the quick-startup and energy-reduction techniques in low-energy IoT applications.

TABLE II
COMPARISON WITH PREVIOUS WORKS

	TI [28]	Broadcom [13]	UTokyo [17]		Qualcomm [14]	UTokyo [22]	TI [33]	This work [9]
Oscillation frequency (MHz)	26	26	39.25		48	39.25	24	39.25
CMOS process (nm)	90	65	40		28	180	65	65
Supply voltage (V)	1.4	1.8	0.7		1	1.5	1.68	3.3
Current (μA)	2143	1200	99	13	1500	121	413	5.8
Power (μW)	3000	2160	69	9.2	1500	181	693	19
Number of samples	N/A	N/A	N/A		N/A	N/A	N/A	11
Temperature range (°C)	–30 to 85	N/A	N/A		N/A	–10 to 60	–40 to 90	–30 to 80
Freq. variations over temp. (ppm)	±7	N/A	N/A		N/A	±5.5	N/A	±10.5
Freq. variations with voltage (ppm / V)	0.5	N/A	25.1	120	N/A	1.3	N/A	0.18
Phase noise @1 kHz offset (dBc / Hz)	–140	–136	–120	–70	–114	–147	N/A	–139
FoM (dBc / Hz)	–224	–221	–223	–182	–206	–246	N/A	–248
Die area (μm^2)	180,000	150,000	60,500		13,300	120,000	80,000	88,200
Start-up time (ms)	2.5	3.2	0.259	N/A	N/A	0.158	0.435	3.9

A summary of the performances of the proposed crystal oscillator [9] and a comparison with those in previous works [13], [14], [17], [22], [28], [33] are shown in Table II in chronological order. The proposed stacked-amplifier crystal oscillator demonstrates the smallest ever reported FoM of −248 dBc/Hz for a crystal oscillator. The values of FoM in [9] and [22] are 30 dB larger than that in Table II, because the power consumption was normalized by the unit of watt in the previous publications. However, the power consumption is normalized by the unit of milliwatt in many studies on high-frequency oscillators [8]. To prevent confusion due to the different definitions among studies, all values of FoM in Table II are calculated with the unit of milliwatt. The current consumption of 5.8 μA is achieved by the proposed power reduction technique of the stacked-amplifier architecture. The relative frequency errors among the 11 samples at temperatures of −30 °C to 80 °C and for ±10% supply voltage variation are ±10.5 ppm and ±0.12 ppm (=±0.18 ppm/V), respectively.

V. CONCLUSION

A low-power 39.25-MHz crystal oscillator with a stacked-amplifier architecture was presented. The proposed stacked-amplifier architecture reduces the power consumption by 91% in the case of four stages of stacked amplifiers. New theoretical analyses of the power consumption and PN in a proposed stacked-amplifier crystal oscillator clarify the reason why the proposed oscillator achieves the smallest ever reported FoM of −248 dBc/Hz with a power consumption of 19 μW and PN of −139 dBc/Hz at 1-kHz offset frequency. A new self-forward-body-biasing technique and flicker noise suppression technique were also presented, which reduce the minimum operational supply voltage ($V_{DD(MIN)}$) and the PN, respectively. Using the proposed self-forward-body-biasing technique, $V_{DD(MIN)}$ in the worst case (−30 °C and a slow corner) is reduced by 0.3 V, thereby achieving reliable operation even with PVT variations. The measurement results for 11 samples verify the reliable and accurate frequency generation of the proposed crystal oscillator with relative frequency errors of ±10.5 and ±0.12 ppm at temperature of −30 °C to 80 °C and for ±10% supply voltage variation, respectively.

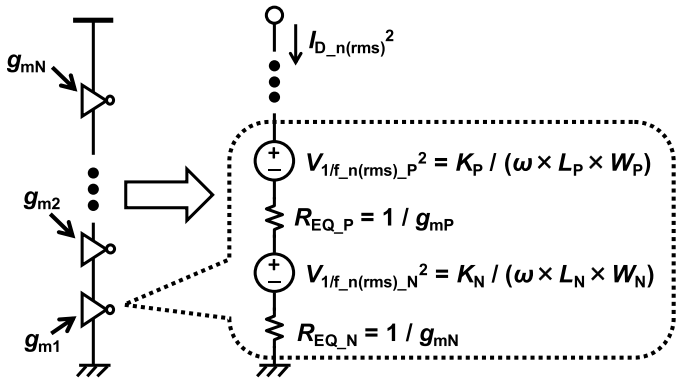


Fig. 15. Equivalent circuit of the N-stages stacked amplifiers.

APPENDIX
DERIVATION OF (8)

The detailed derivation of (8) is given in this Appendix. The equivalent circuit of the N-stages stacked amplifiers is shown in Fig. 15. The equivalent resistances of the NMOS and PMOS transistors are denoted as R_{EQ_N} and R_{EQ_P}, respectively. The squares of the equivalent flicker noise voltage ($V_{1/f\_n(rms)}^2$) of the NMOS and PMOS transistors are denoted as $V_{1/f\_n(rms)\_N}^2$ and $V_{1/f\_n(rms)\_P}^2$, respectively. Using the relationship $g_{mN} = g_{mP} = g_{m(TOTAL)}/(2 \times N)$ and Thevenin's theorem, the total equivalent resistance (R_{EQ_TOTAL}) and the total square of the equivalent flicker noise voltage ($V_{1/f\_n(rms)\_TOTAL}^2$) are given as

$$R_{EQ\_TOTAL} = N \times \left(\frac{1}{g_{mN}} + \frac{1}{g_{mP}} \right) = \frac{4N^2}{g_{m(TOTAL)}} \quad \text{(A1)}$$

and

$$V^2_{\mathrm{1/f\_n(rms)\_TOTAL}} = N \times (V^2_{\mathrm{1/f\_n(rms)\_N}} + V^2_{\mathrm{1/f\_n(rms)\_P}}) = N \times \left(\frac{K_\mathrm{N}}{\omega L_\mathrm{N} W_\mathrm{N}} + \frac{K_\mathrm{P}}{\omega L_\mathrm{P} W_\mathrm{P}}\right). \quad \text{(A2)}$$

Using (A1) and (A2), $I^2_{\mathrm{D\_n(rms)}}$ for the N-stages stacked amplifiers is derived as

$$I^2_{\mathrm{D\_n(rms)}} = \frac{V^2_{\mathrm{1/f\_n(rms)\_TOTAL}}}{R^2_{\mathrm{EQ\_TOTAL}}} = \frac{(nK_\mathrm{N} + K_\mathrm{P}) g^2_{\mathrm{m(TOTAL)}}}{16 n \omega N^3 L_\mathrm{N} W_\mathrm{N}} \quad \text{(A3)}$$

assuming with the relationships $L_\mathrm{N} = L_\mathrm{P}$ and $n \times W_\mathrm{N} = W_\mathrm{P}$.

Acknowledgment

The authors would like to thank Y. Yoshihara, Y. Niki, and R. Fujimoto of Toshiba Corporation for technical discussions, and R. Shidachi and S. Lee of The University of Tokyo for support in the measurements.

References

[1] A. M. Nicolson, "Generating and transmitting electric currents," U.S. Patent 2,212,845 A, Aug. 27, 1940.
[2] W. G. Cady, "Method of maintaining electric currents of constant frequency," U.S. Patent 1,472,583 A, Oct. 30, 1923.
[3] R. J. Thompson, Jr., *Crystal Clear: The Struggle for Reliable Communications Technology in World War II*, 1st ed. Hoboken, NJ, USA: Wiley, 2011.
[4] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE J. Solid-State Circuits*, vol. SSC-12, no. 3, pp. 224–231, Jun. 1977.
[5] E. A. Vittoz, M. G. R. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: Theory and application," *IEEE J. Solid-State Circuits*, vol. SSC-23, no. 3, pp. 774–783, Jun. 1988.
[6] L. Atzori, A. Lera, and G. Morabito, "The Internet of Things: A survey," *Comput. Netw.*, vol. 54, no. 15, pp. 2787–2805, Oct. 2010.
[7] Bluetooth Special Interest Group (SIG). (2014). *Specification of the Bluetooth System, Core Package Version 4.2, Bluetooth Specifications, Bluetooth Special Interest Group (SIG)*. [Online]. Available: https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=286439
[8] W. Deng, K. Okada, and A. Matsuzawa, "Class-C VCO with amplitude feedback loop for robust start-up and enhanced oscillation swing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 429–440, Feb. 2013.
[9] S. Iguchi, T. Sakurai, and M. Takamiya, "A 39.25 MHz 278 dB-FOM 19 μW LDO-free stacked-amplifier crystal oscillator (SAXO) operating at I/O voltage," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 100–101.
[10] J. T. Santos and R. G. Meyer, "A one-pin crystal oscillator for VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 2, pp. 228–236, Apr. 1984.
[11] D. Aebischer, H. J. Oguey, and V. R. V. Kaenel, "A 2.1-MHz crystal oscillator time base with a current consumption under 500 nA," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 999–1005, Jul. 1997.
[12] D. Ruffieux, "A high-stability, ultra-low-power quartz differential oscillator circuit for demanding radio applications," in *Proc. 28th Eur. Solid-State Circuits Conf.*, Sep. 2002, pp. 85–88.
[13] Y. Chang, J. Leete, Z. Zhou, M. Vadipour, Y.-T. Chang, and H. Darabi, "A differential digitally controlled crystal oscillator with a 14-bit tuning resolution and sine wave outputs for cellular applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 421–434, Feb. 2012.
[14] M. M. Ghahramani, Y. Rajavi, A. Khalili, A. Kavousian, B. Kim, and M. P. Flynn, "A 192 MHz differential XO based frequency quadrupler with sub-picosecond jitter in 28 nm CMOS," in *IEEE Radio Freq. Integr. Circuits Conf. Dig. Tech. Papers*, May 2015, pp. 59–62.
[15] U. Karthaus, "A differential two-pin crystal oscillator–concept, analysis, and implementation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 10, pp. 1073–1077, Oct. 2006.
[16] D. Ruffieux *et al.*, "A 3.2×1.5×0.8 mm^3 240 nA 1.25-to-5.5 V 32 kHz-DTCXO RTC module with an overall accuracy of ±1 ppm and an all-digital 0.1 ppm compensation-resolution scheme at 1 Hz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 208–209.
[17] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and M. Takamiya, "93% power reduction by automatic self power gating (ASPG) and multistage inverter for negative resistance (MINR) in 0.7 V, 9.2 μW, 39 MHz crystal oscillator," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2013, pp. C142–C143.
[18] A. Shrivastava, D. A. Kamakshi, and B. H. Calhoun, "A 1.5 nW, 32.768 kHz XTAL oscillator operational from a 0.3 V supply," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 686–696, Mar. 2016.
[19] K.-J. Hsiao, "A 1.89 nW/0.15 V self-charged XO for real-time clock generation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 298–299.
[20] D. Yoon, T. Jang, D. Sylvester, and D. Blaauw, "A 5.58 nW crystal oscillator using pulsed driver for real-time clocks," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 509–522, Feb. 2016.
[21] A. Rusznyak, "Start-up time of CMOS oscillators," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 3, pp. 259–268, Mar. 1987.
[22] S. Iguchi, H. Fuketa, T. Sakurai, and M. Takamiya, "Variation-tolerant quick-start-up CMOS crystal oscillator with chirp injection and negative resistance booster," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 496–508, Feb. 2016.
[23] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.
[24] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[25] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, Mar. 2000.
[26] E. Vittoz, *Low-Power Crystal and MEMS Oscillators*, 1st ed. Berlin, Germany: Springer, 2010.
[27] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd ed. Oxford, U.K.: Oxford Univ. Press, 2011.
[28] J. Lin, "A low-phase-noise 0.004-ppm/step DCXO with guaranteed monotonicity in the 90-nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2726–2734, Dec. 2005.
[29] S. G. de A. Garcin, "Crystal oscillator troubleshooting guide," Freescale Semiconductor, Austin, TX, USA, Appl. Note AN3208, 2006. [Online]. Available: http://www.nxp.com/assets/documents/data/en/application-notes/AN3208.pdf
[30] R. L. Filler and J. R. Vig, "Long-term aging of oscillators," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 40, no. 4, pp. 387–394, Jul. 1993.
[31] R. A. Bianchi, J. M. Karam, and B. Courtois, "Analog ALC crystal oscillators for high-temperature applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 2–14, Jan. 2000.
[32] R. M. Cerda, *Understanding Quartz Crystals and Oscillators*, 1st ed. Norwood, MA, USA: Artech House, 2014.
[33] D. Griffith, J. Murdock, and P. T. Røine, "A 24 MHz crystal oscillator with robust fast start-up using dithered injection," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 104–105.
[34] M. Ding *et al.*, "A 95 μW 24 MHz digitally controlled crystal oscillator for IoT applications with 36 nJ start-up energy and >13× start-up time reduction using a fully-autonomous dynamically-adjusted load," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 90–91.

Shunta Iguchi (S'12–M'16) received the B.S. degree in electronic engineering from The University of Electro-Communications, Tokyo, Japan, in 2011, and the M.S. and Ph.D. degrees in electrical engineering and information systems from The University of Tokyo, Tokyo, in 2013 and 2016, respectively.

He joined Analog Devices, Tokyo, Japan, in 2011, Toshiba, Kanagawa, Japan, in 2013, and TSMC, Hsinchu, Taiwan, in 2014, as an Intern. He was a Project Researcher with The University of Tokyo in 2016. In 2016, he joined Qualcomm, San Diego, CA, USA, where he is involved in the circuit design of ultra-low-noise oscillators for smartphone chipsets. His current research interests include the design of low-power and low-noise oscillators, RF transceiver circuits, and wireless power transmission circuits.

Dr. Iguchi was a recipient of the Outstanding Award in NE Analog Innovation Award 2016 and the Best Paper Award at the 2013 IEEE Wireless Power Transfer Conference.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, Kawasaki, Japan, where he was involved in the design of CMOS DRAM, SRAM, RISC processors, DSPs, and system-on-chip Solutions. He was involved extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher at the University of California, Berkeley, CA, USA, where he conducted research in the field of very large scale integration (VLSI) CAD. Since 1996, he has been a Professor with The University of Tokyo, where he was involved in low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's and large-area electronics. He has authored or co-authored more than 600 technical publications including 100 invited presentations and several books and holds more than 200 patents.

Dr. Sakurai is an IEICE Fellow. He served as an Executive Committee Member of ISLPED and a Program Committee Member of ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He was a recipient of the 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, the 2009 and 2010 IEEE Paul Rappaport Award, the 2010 IEICE Electronics Society Award, the 2009 IEICE Achievement Award, the 2005 IEEE ICICDT Award, the 2004 IEEE Takuo Sugano Award, and the 2005 P&I Patent of the Year Award and four product awards. He was the Executive Committee Chair of the VLSI Symposia and the Steering Committee Chair of the IEEE A-SSCC. He served as the Conference Chair of the Symposium on the VLSI Circuits and ICICDT, the Vice Chair of ASPDAC, and the TPC Chair of the A-SSCC and VLSI symposium. He delivered keynote speech at more than 50 conferences including ISSCC, ESSCIRC, and ISLPED. He was an elected AdCom Member of the IEEE Solid-State Circuits Society and the IEEE CAS and SSCS Distinguished Lecturer. He is also a Domain Research Supervisor for nano-electronics area with Japan Science and Technology Agency.

Makoto Takamiya (S'98–M'00–SM'14) received the B.S., M.S., and Ph.D. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined NEC Corporation, Sagamihara, Japan, where he was involved in the circuit design of high-speed digital LSIs. In 2005, he joined The University of Tokyo, where he is an Associate Professor with the VLSI Design and Education Center. From 2013 to 2014, he was a Visiting Scholar at the University of California, Berkeley, CA, USA. His current research interests include the integrated power management circuits for the ultralow power Internet of Things applications and the digital gate driver circuits for IGBT.

Dr. Takamiya is a member of the technical program committee of the IEEE International Solid-State Circuits Conference and the IEEE Symposium on VLSI Circuits. He received the 2009 and 2010 IEEE Paul Rappaport Awards and the Best Paper Award in 2013 IEEE Wireless Power Transfer Conference.