General-Purpose Clocked Gate Driver IC With Programmable 63-Level Drivability to Optimize Overshoot and Energy Loss in Switching by a Simulated Annealing Algorithm

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***Abstract*—A general-purpose clocked gate driver integrated circuit (IC) to generate an arbitrary gate waveform is proposed to provide a universal platform for fine-grained gate waveform optimization handling various power transistors. The fabricated IC with a 0.18 μm Bipolar-CMOS-DMOS process has 63 P-type MOS (PMOS) and 63 N-type MOS (NMOS) driver transistors on a chip whose activation patterns are controlled by 6-bit digital signals and 40 ns time step control. In the 500 V switching measurements with a manual gate waveform optimization, the proposed gate driver reduces the $I_{\rm C}$ overshoot by 25% and 41%, and the energy loss by 38% and 55% for Si-insulated-gate bipolar transistor and SiC-MOSFET, respectively, which demonstrate the feasibility of driving various power devices with the same driver. An automatic optimization by simulated annealing algorithm is introduced to fully utilize the benefit of the gate driver, and the further reduction of $I_{\rm C}$ overshoot by 26% and the energy loss by 18% are achieved over the manual optimization.**

***Index Terms*—Gate driver, insulated-gate bipolar transistor (IGBT), SiC, simulated annealing (SA).**

I. Introduction

A GATE driver is a key technology for the switching of devices to minimize the switching loss and the current overshoot. The conventional gate drivers, however, have two problems: 1) customized design to each power transistor (e.g., Si-insulated-gate bipolar transistor (IGBT), SiC-MOSFET) increases the development cost and turnaround time (TAT); and 2) limited programmability [2]–[10] prevents a precise gate waveform optimization for the low noise and the low loss of the power transistors. To solve these issues, a general-purpose clocked gate driver (CGD) integrated circuit (IC) is proposed to provide a universal platform for fine-grained gate waveform optimization handling various power transistors including Si-IGBT and SiC-MOSFET, thereby reducing the development cost and TAT for the gate drivers. The programmability of the proposed gate driver is the finest compared with the previous gate drivers [1]–[10] and it is shown that the finer programmability realizes the better performance. However, in order to fully enjoy the benefit of the fine granularity of the proposed gate driver, a manual optimization may not be sufficient as the degree of freedom is much increased. Thus, in this paper, an automatic optimization based on simulated annealing (SA) is introduced and shows the possibility of the further increase in performance.

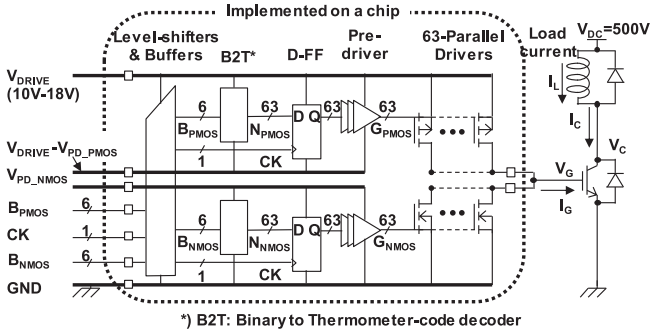

Fig. 1. Schematic diagram of general-purpose CGD IC.

II. System Implementation

The schematic diagram of the implemented general-purpose CGD IC is shown in Fig. 1 [15]. CGD IC is developed for the switching of power devices at $V_{\rm DC} = 500$ V. In order to realize programmable 63-level drivability, 63 parallel drivers are connected to the gate of the power device and a 6-bit binary control signal, $B_{\rm PMOS}$ ($B_{\rm NMOS}$), is applied to specify the number of activated P-type-MOS (PMOS) [N-type MOS (NMOS)] driver transistors, $N_{\rm PMOS}$ ($N_{\rm NMOS}$). A pair of 6-bit signals ($B_{\rm PMOS}$ and $B_{\rm NMOS}$) are latched by

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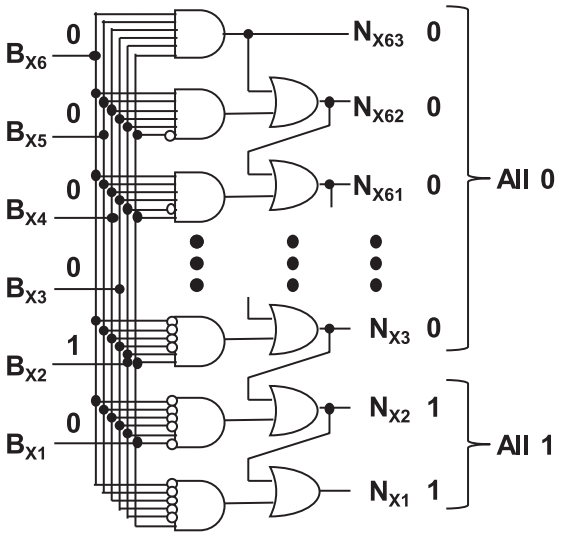

Fig. 2. Binary to thermometer-code decoder.

the clock (CK) and activate the final 63 PMOS (NMOS) transistors. CK frequency is 25 MHz and 40 ns time step control of the drivability is achieved. The power supply voltage (V_{DRIVE}) of CGD IC is 10–18 V, and V_{DRIVE} of 15 V is used in the following measurements. The voltage swing of input digital signals (B_{PMOS}, B_{NMOS}, and CK) is 5 V, and the swing is increased to V_{DRIVE} by level-shifters. By adjusting the predriver voltage swing, $V_{\mathrm{PD\_PMOS}}$ and $V_{\mathrm{PD\_NMOS}}$, from 1.2 to 5 V, the output drivability of a single-driver metal-oxide-semiconductor (MOS) transistor can be tuned from 3 to 80 mA. The peak drivability is 63 times of the single driver, which corresponds to the maximum peak current of the gate current (I_G) from 0.19 A ($=$ 3 mA $\times$ 63) to 5 A ($=$ 80 mA $\times$ 63). $V_{\mathrm{PD\_PMOS}}$ and $V_{\mathrm{PD\_NMOS}}$ of 1.8 V are used in the following measurements.

The binary-coded input is indispensable since 63 $\times$ 2 input pins are too many to handle. The binary signals, however, may cause glitch problems in the gate voltage (V_G). The glitch will break down the power transistors. For example, when the binary input changes from 011111 (31) to 100000 (32), there is a possibility that the state goes from 011111 (31) to 111111 (63) to 100000 (32) causing a few nanoseconds glitch at the predriver, if there are variability of devices and interconnection designs which make the most significant bit change faster than the other bits. This is the cause of the glitch problems. To prevent this problem, a small-sized binary to thermometer-code decoder in Fig. 2 is employed.

Fig. 3 shows operation waveforms for 63 PMOS transistors to pull up V_{G} in CGD IC. The operation for 63 NMOS transistors to pull down V_G is similar. An arbitrary I_G waveform is generated by applying a control bit pattern (B_{PMOS} (B_{NMOS})) in each clock cycle with 40-ns step and digitally specifying time and current pairs of t_i and I_{Gi} ($i = 1, 2, 3, \ldots, n$).

Here, the modeling of the 63-parallel drivers in Fig. 1 is discussed. In the previous segmented gate drivers [10], the transistors in the segmented gate drivers [see Fig. 4(a)] were modeled as a resistor [see Fig. 4(b)]. The transistors in the segmented gate drivers, however, are to be modeled as a current source [see

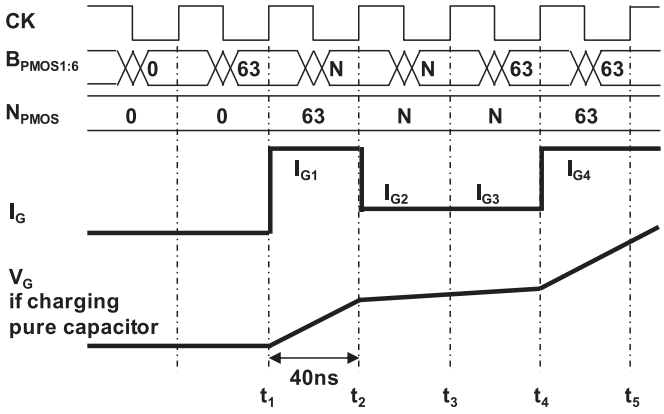

Fig. 3. Operation waveforms for 63 PMOS transistors to pull up V_G in CGD IC.

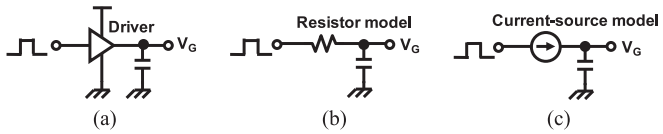

Fig. 4. Modeling of gate drivers. (a) Original gate driver. (b) Conventional resistor model. (c) Proposed current-source model.

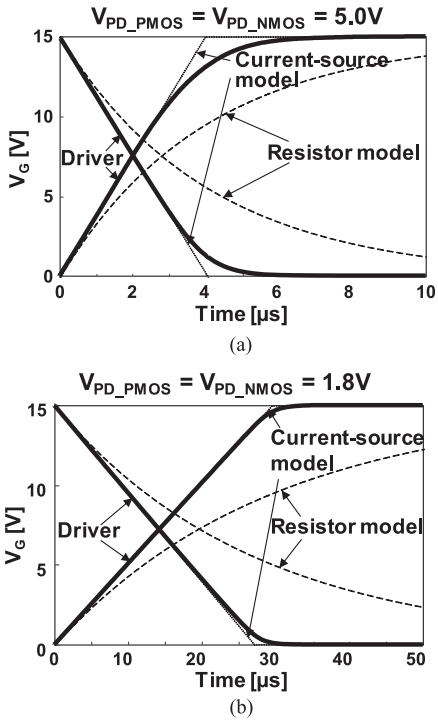

Fig. 5. SPICE simulated pull-up and pull-down waveforms of VG with two models in Fig. 4. VPD_PMOS and VPD_NMOS are 5 and 1.8 V in (a) and (b), respectively.

Fig. 4(c)] instead of a resistor [see Fig. 4(b)]. Fig. 5 shows the simulation program with integrated circuit emphasis (SPICE) simulated pull-up and pull-down waveforms of V_G with two models in Fig. 4. The capacitance in Fig. 4 is 22 nF emulating the gate capacitance of the power devices. $V_{\mathrm{PD\_PMOS}}$ and $V_{\mathrm{PD\_NMOS}}$ are 5 and 1.8 V in Fig. 5(a) and (b), respectively. It

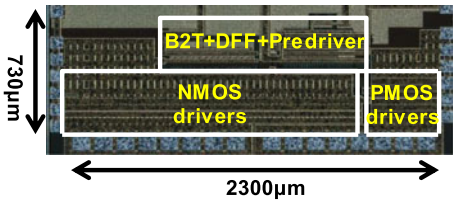

Fig. 6. Die photograph of gate driver IC.

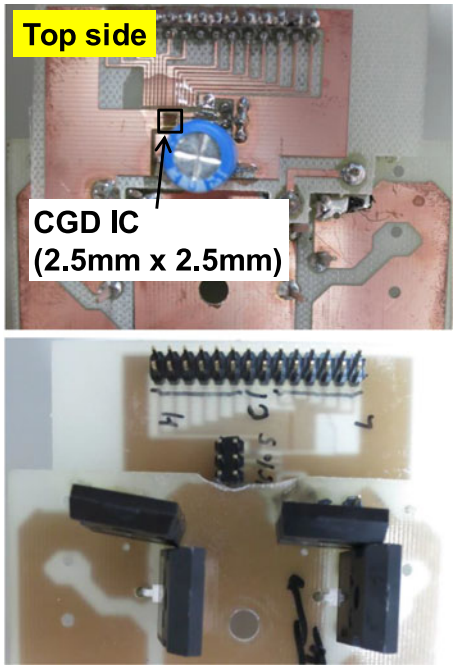

Fig. 7. Photographs of PCB.

is seen that the gate driver behaves more like a constant-current driver [see Fig. 4(c)] rather than a resistor [see Fig. 4(b)] because of the high output resistance of MOS transistors in a saturation region. Still, the behavior of a MOS driver is fundamentally similar to a resistor, which has been used for a long time in driving the power devices. A minor difference is that when considering the switching between two different driver strength states, the driver current is the more predictable for MOS drivers whose driving current is independent from the voltage of the switching, while the driving current is dependent on the switching voltage and thus timing for a driver based on resistors

The proposed general-purpose CGD IC is fabricated with 40 V, 0.18 μm Bipolar-CMOS-DMOS process. Fig. 6 shows a die photograph of CGD IC. The core size is 2300 μm by 730 μm. The total chip size is 2.5 mm^2, which is determined by the foundry, although the core size is much smaller than the total chip size. Fig. 7 shows photographs of printed circuit board (PCB). The 2.5 mm^2 CGD IC is placed on the top side of PCB. Si-IGBT and SiC diodes are placed on the reverse side of PCB.

III. Measurement Results

Turn-on and turn-off characteristics are measured with a double-pulse setup shown in Fig. 1 with SiC diodes

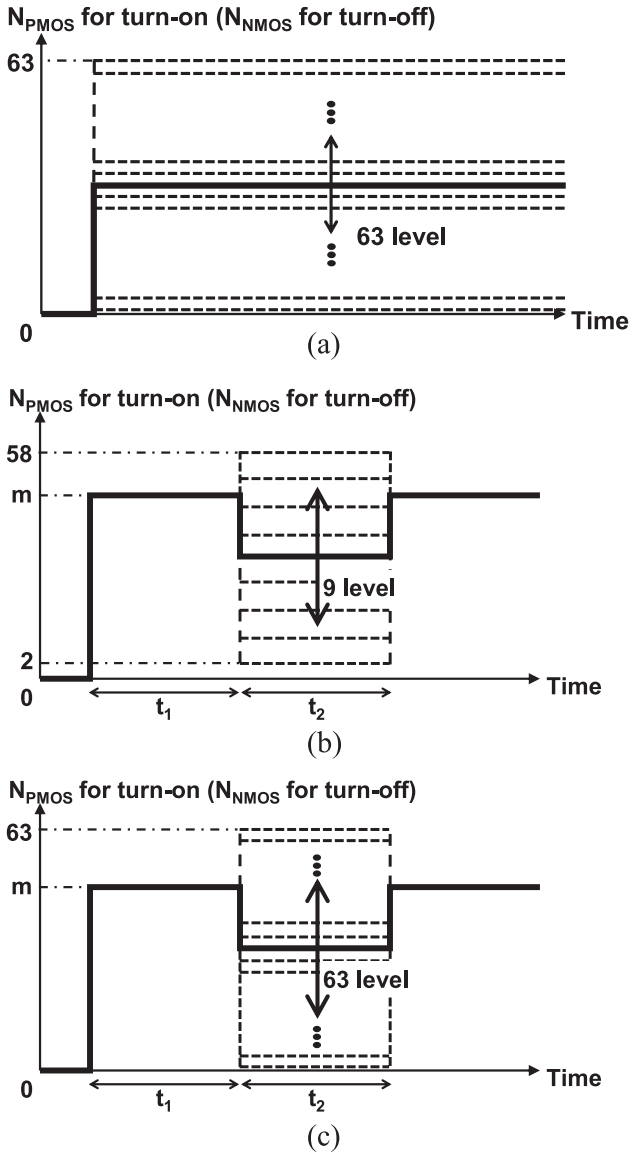

Fig. 8. Three types of gate waveforms. (a) No active gate drive. (b) Nine-level active gate drive. (c) Proposed 63-level active gate drive.

(C4D10120D, 1200 V, 18 A) at $V_{\rm DC}$ = 500 V. To demonstrate the versatility of the proposed general-purpose CGD IC, both Si-IGBT (IRG7PH46UPbF, 1200 V, 75 A) and SiC-MOSFET (SCH2080KE, 1200 V, 40 A) are driven by CGD IC. Although in Fig. 1, an IGBT symbol is used for a power device, the IGBT is replaced by SiC-MOSFET when SiC-MOSFET is under test. Notations such as I_C and V_C are used even for the SiC-MOSFET device just for simplicity. Turn-off characteristics are described only for Si-IGBT in Section III-B as the results basically do not change much for the SiC-MOSFET.

A. Turn-on Case

To show the advantage of the proposed CGD IC with programmable 63-level drivability, three types of gate waveforms shown in Fig. 8 are compared. Fig. 8(a) shows a conventional "no active gate drive" [11]. To show the tradeoff between the

TABLE I
PARAMETERS USED IN MEASUREMENTS FOR SI-IGBT AND SIC-MOSFET

	Si-IGBT turn on	SiC-MOSFET turn on	Si-IGBT turn off
m	31	63	32
t_1	160 ns	40 ns	400 ns
t_2	160 ns	80 ns	400 ns

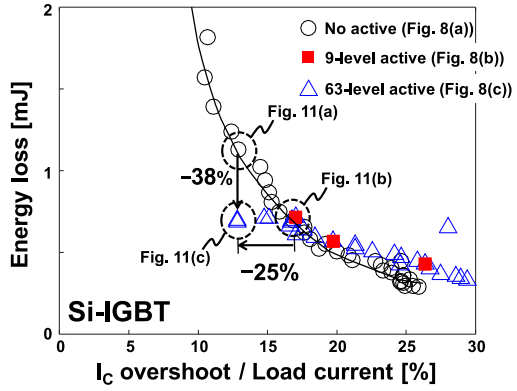

Fig. 9. Measured energy loss versus IC overshoot in turn-on characteristics at 500 V switching for Si-IGBT. The load current I_L is set to be 15.4 A.

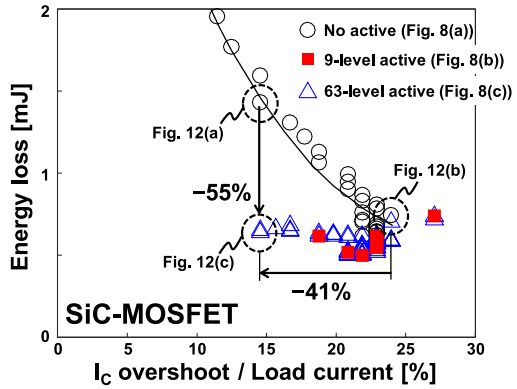

Fig. 10. Measured energy loss versus I_C overshoot in turn-on characteristics at 500 V switching for SiC-MOSFET. The load current I_L is set to be 15.4 A.

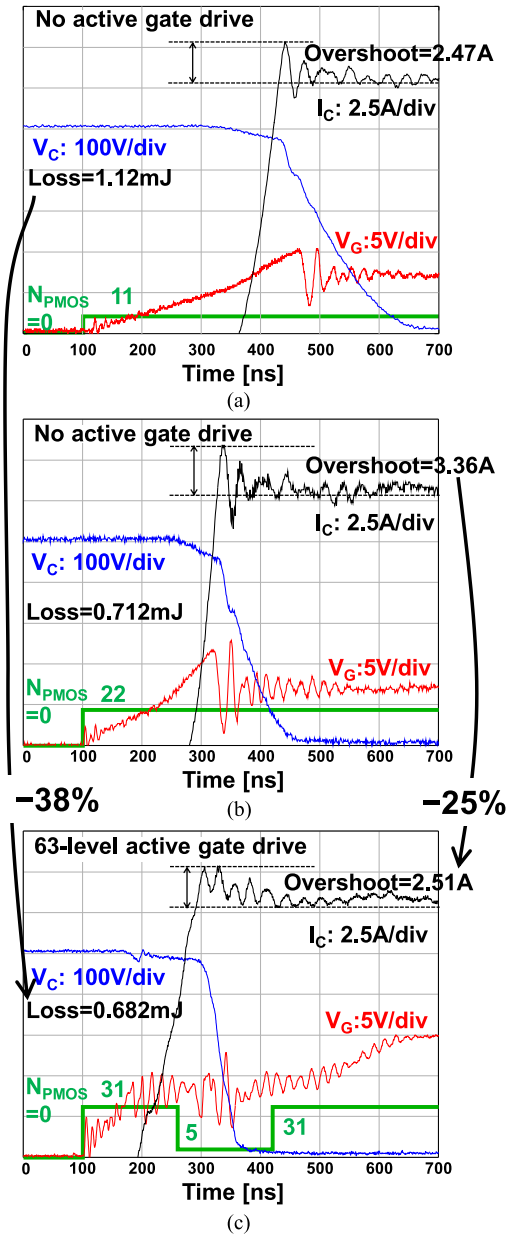

Fig. 11. Measured waveforms for Si-IGBT corresponding to Fig. 9. (a) No active gate drive at the same I_C overshoot to (c). (b) No active gate drive at the same energy loss to (c). (c) Proposed 63-level active gate drive.

turn-on energy loss and I_C overshoot, I_G to pull-up V_G is varied by N_{PMOS} in the measurement. Fig. 8(b) shows a conventional "9-level active gate drive" emulating the 9-level segmented gate drivers [10]. This waveform is based on [5], [7], [9], and [12]. At the turn on, N_{PMOS} changes from 0 to m and keeps m for t_1. Then, N_{PMOS} changes from m to 9 level of i ($i = 2$–58 with seven increments in between) and keeps i for t_2. Finally, N_{PMOS} changes from i to m. Fig. 8(c) shows the proposed "63-level active gate drive." Fig. 8(c) is the same as Fig. 8(b) except for i. In Fig. 8(c), i is from 0 to 63 with one increment in between. Table I shows m, t_1, and t_2 in the measurements for Si-IGBT and SiC-MOSFET, respectively.

Figs. 9 and 10 show measured energy loss versus I_{C} overshoot in turn-on characteristics at 500-V switching with the three gate waveforms shown in Fig. 8 for Si-IGBT and SiC-MOSFET, respectively. In the no active gate drive, the tradeoff between the turn-on energy loss and I_C overshoot is observed. By using 63-level active gate drive, however, the loss-overshoot tradeoff can be optimized more compared with cases of nine-level active gate drive [10] and no active gate drive. In Figs. 9 and 10, the blue open triangle points near the optimum point are observed by changing just one turn-on transistor count (N_{PMOS}) for the time segment t_2. It is seen from these figures that the change in the loss and overshoot by just one step in 63 levels is visible and thus providing 63 levels of driving strength if justified.

The proposed 63-level active gate drive reduces the measured energy loss at the same I_{C} overshoot by 38% (see Fig. 9) and 55% (see Fig. 10) for Si-IGBT and SiC-MOSFET, respectively. Similarly, the proposed 63-level active gate drive reduces the

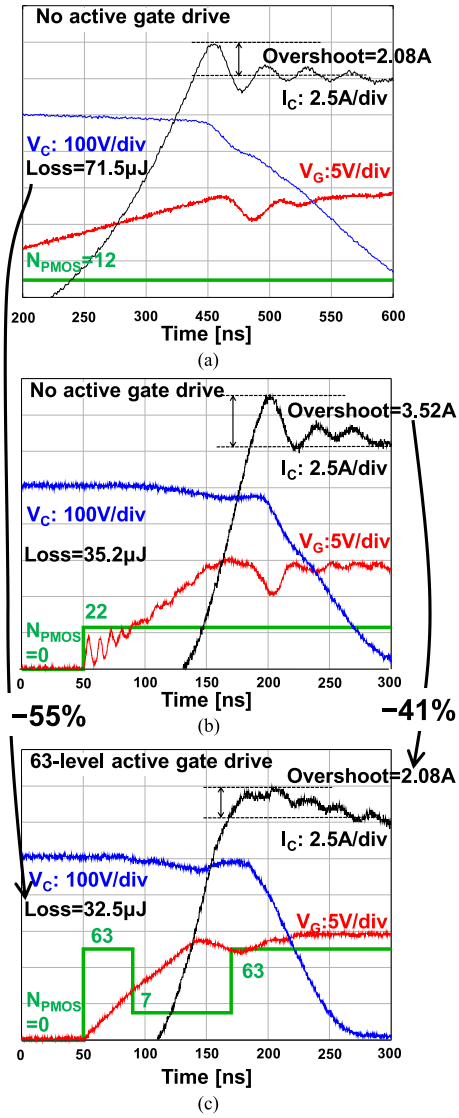

Fig. 12. Measured waveforms for SiC-MOSFET corresponding to Fig. 10. (a) No active gate drive at the same IC overshoot to (c). (b) No active gate drive at the same energy loss to (c). (c) Proposed 63-level active gate drive.

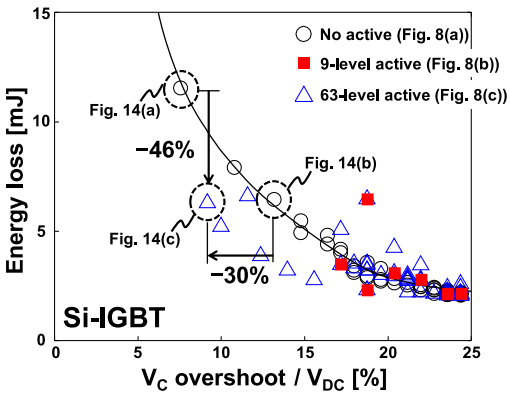

Fig. 13. Measured energy loss versus VC overshoot in turn-on characteristics at 500-V switching for Si-IGBT. The load current I_L is set to be 52 A.

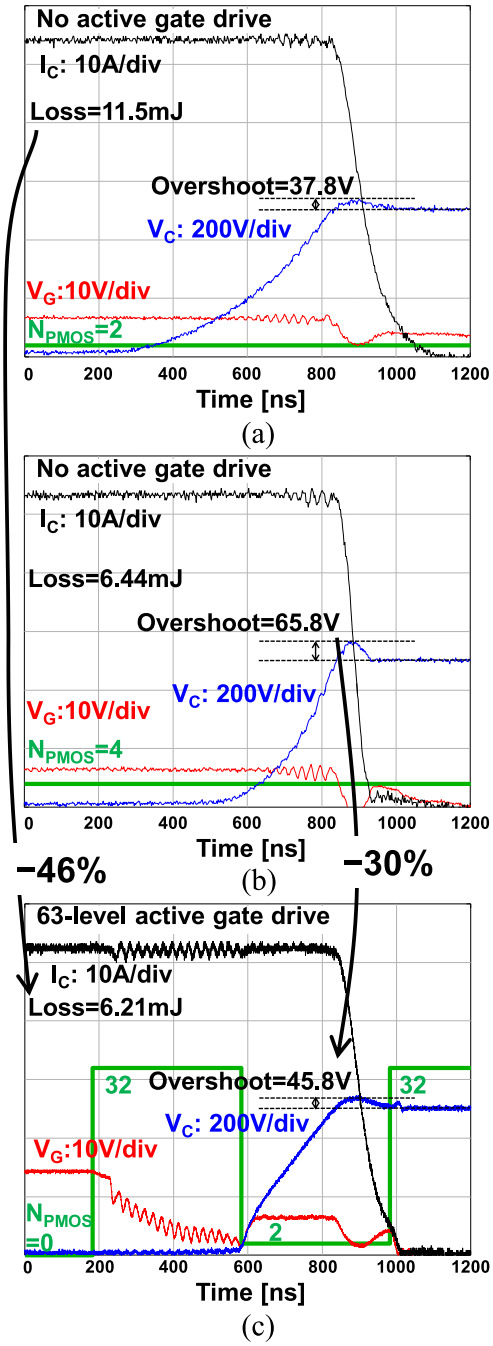

Fig. 14. Measured waveforms for Si-IGBT corresponding to Fig. 13. (a) No active gate drive at the same VC overshoot to (c). (b) No active gate drive at the same energy loss to (c). (c) Proposed 63-level active gate drive.

measured I_C overshoot at the same energy loss by 25% (see Fig. 9) and 41% (see Fig. 10) for Si-IGBT and SiC-MOSFET, respectively. The corresponding measured waveforms of N_{PMOS}, V_G, V_C, and I_C for Si-IGBT and SiC-MOSFET are shown in Figs. 11 and 12, respectively. The 25% and 41% reduction of I_C overshoot is clearly shown in Figs. 11 and 12, respectively.

In this paper, the search for the best driving waveform is carried out manually through trial and error by confining the search space and by reducing the waveform choices. In general, however, more time segments can be used and the number of

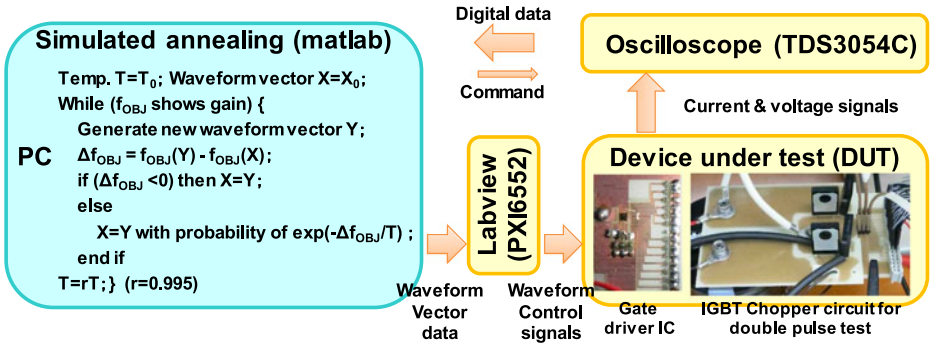

Fig. 15. Setup for automatic optimization (yellow part is hardware and blue part is software).

turn-on transistors in each time segment can be selected out of 64 choices. Thus, the search complexity becomes huge and may not be done manually. For this kind of general case, a machine-based search method can be effective. An example of the machine-based search using the SA algorithm is reported elsewhere [13]. Even though this paper confined the search space compared with the more general search space, much improvement is found as is described above and it can be said that the scheme is effective.

B. Turn-off Case

For the measurements of the turn-off case, the gate drivability optimization is achieved by changing the turn-on NMOS count, N_{NMOS}, instead of N_{PMOS} for the turn-on case. One more difference between the turn-on case and turn-off case measurements is that the voltage overshoot, V_C, is taken as the overshoot instead of the current overshoot, I_C, in the turn-on case. Similar to the turn-on case in Section III-A, three types of gate waveforms shown in Fig. 8(a)–(c) are compared.

Fig. 13 shows measured energy loss versus V_{C} overshoot in turn-on characteristics at 500 V switching with the three gate waveforms shown in Fig. 8 for Si-IGBT. The proposed 63-level active gate drive reduces the measured energy loss at the same V_C overshoot by 46%. Similarly, the proposed gate drive reduces the measured V_C overshoot at the same energy loss by 30%. The corresponding measured waveforms of N_{PMOS}, V_G, V_C, and I_C for Si-IGBT are shown in Fig. 14. The 30% reduction of V_C overshoot is clearly seen from the figure.

The optimized gate driving waveform is driving relatively strongly at first and then, reducing the driving strength just before the gate voltage reaches the threshold voltage of the IGBT, and increasing the strength again. This reduces the sharp voltage overshoot. The qualitative strategy for the optimized waveform is consistent with the previous publications [9], [14] and the advantage of the proposed driver is to achieve the quantitative optimization by digital control.

IV. Optimization by SA

As is described in the previous section, it is possible to improve the performance of the circuit by the manual optimization of the gate waveforms by confining ourselves to try the waveforms as shown in Fig. 8. By exploring the wider search space, eight time segments in this case, it may be possible to further improve the performance. Thus, an automatic optimization is applied by combining real measurements and a software optimization loop as shown in Fig. 15.

Any strength of drivability from 0 to 64 ($\times$ 12 mA) can be chosen for each of eight time segments of 40 ns. Thus, 64^8 ($> 10^{14}$) number of waveforms need to be tried for an exhaustive search, which is impractical. Thus, SA is applied in this paper. The target is to minimize the object function, f_{OBJ}, defined as follows:

$$f_{\mathrm{OBJ}} = \sqrt{{E'_{\mathrm{loss}}}^2 + {I'_{C\ \mathrm{overshoot}}}^2}$$

where the energy loss E_{loss} and I_C overshoot $I_{\mathrm{C\,overshoot}}$ are normalized as follows:

$$\begin{cases} E'_{\mathrm{loss}} = \dfrac{E_{\mathrm{loss}} - E_{\mathrm{loss,\,min}}}{E_{\mathrm{loss,\,max}} - E_{loss,\mathrm{min}}} \\ I'_{C\ \mathrm{overshoot}} = \dfrac{I_{C\ \mathrm{overshoot}} - I_{C\ \mathrm{overshoot,\,min}}}{I_{C\ \mathrm{overshoot,\,max}} - I_{C\ \mathrm{overshoot,\,min}}}. \end{cases}$$

The subscript min (max) signifies the minimum (maximum) of the corresponding quantity. For example, $E_{\mathrm{loss,min}}$ is set to 0 as an ideal minimum value. On the other hand, $E_{\mathrm{loss,max}}$ is the measured E_{loss} when the gate drive waveform is the slowest, that is, all of $n_1, n_2, \ldots, n_8$ are 1. Here, n_i signifies the number of turn-on NMOS of the gate driver in ith time-segment in Fig. 1. Likewise, the minimum (maximum) overshoot values are obtained either by the slowest or the fastest gate driving waveform. The values of $I_{\mathrm{C\,overshoot,min}}$ and $I_{\mathrm{C\,overshoot,max}}$ are set similar to $E_{\mathrm{loss,min}}$ and $E_{\mathrm{loss,max}}$. After the normalization, all of the normalized quantities vary between 0 and 1.

First, a PC randomly generates a new trial waveform, that is, a new waveform vector $(n_1 \ldots n_8)$ using MATLAB and sends control signals to the gate driver through LabVIEW, and then the digital oscilloscope receives the measured voltage and current from the board and sends the digital data back to the PC. Depending on the measured value of f_{OBJ}, the PC generates the next trial waveform according to the SA algorithm described in Fig. 15. The optimization iterations continue until no gain in observed. One physical measurement of about 2 s is needed in one SA iteration loop and less than 2000 measurements are needed to complete the optimization, and thus it takes about an hour for the whole process. No destructive breakdown of power devices was observed in the optimization process. A greedy optimization algorithm, that is, the hill descending algorithm is also tried but it stops at a suboptimal point, which is even worse than no

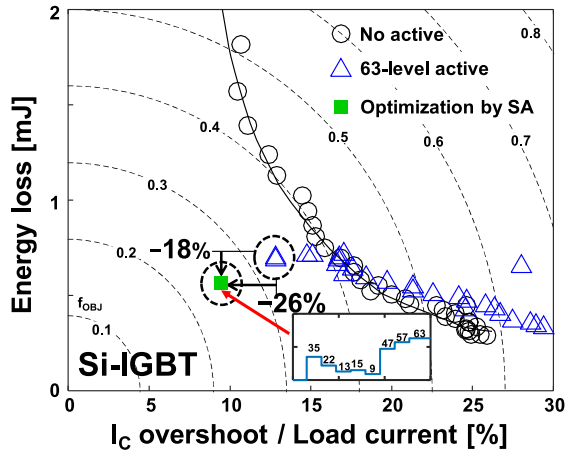

Fig. 16. Measured optimization result by the SA algorithm in turn-on characteristics at 500 V switching for Si-IGBT. The load current I_L is set to be 15.4 A.

TABLE II
COMPARISON WITH PREVIOUS GATE DRIVERS

	[1]	[2]	[6]	[10]	This work
Implementation	PCB	PCB	PCB	IC	IC
Target power device	Si-IGBT	Si-IGBT	SiC-MOSFET	Si-IGBT	Si-IGBT & SiC-MOSFET
Time programmability	NA	NA	NA	NA	40-ns step
Number of drivability levels	2	2	4	9	63
How to change drivability	R_G	R_G	Drive voltage	Driver size	N_{PMOS}, N_{NMOS} V_{PD_PMOS}, V_{PD_NMOS}
Gate current	NA	NA	NA	NA	3mA~5A
Optimization method	Manual	Manual	Manual	Manual	Manual & Simulated Annealing

active control case. Consequently, it is concluded that a global optimization algorithm such as SA should be used.

In Fig. 16, the optimization result by the SA algorithm is shown together with the human manual search results. I_C overshoot and the energy loss are better than the human manual search results (see Fig. 9) by 26% and 18%, respectively. Generally speaking, the optimized waveform is a function of several parameters such as $V_{\rm DC}$ and I_L, and a table lookup approach will be implemented in the future to cope with the parameter dependence. The optimization is executed in the development stage. Some may argue that a dynamic on-the-fly optimization is more suitable but applying a new trial waveform may be risky in a product in operation and moreover when the aforementioned parameters change from cycle to cycle, as is observed in multilevel converters, it is difficult to optimize on the fly due to the short time period permitted for optimization.

V. CONCLUSION

Table II shows a comparison of the proposed CGD IC with previous gate drivers. This work achieved the 40-ns step timing control and 63-level drivability, thereby enabling the gate waveform optimization for both Si-IGBT and SiC-MOSFET. The time programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels.

The general-purpose gate driver IC to generate an arbitrary gate waveform is the universal platform for fine-grained gate waveform optimization handling various power transistors. The 40-ns step timing programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels in the previously published gate drivers. In the 500 V turn-on measurements, the proposed CGD reduces the $I_{\rm C}$ overshoot by 25% and 41% and the energy loss by 38% and 55% for Si-IGBT and SiC-MOSFET, respectively. For a turn-off case, the measurement for Si-IGBT shows that V_C overshoot and the energy loss are reduced by 30% and 46%, respectively. Not only for the case of turn on, the improvement is also observed for the turn-off case of Si-IGBT.

An automatic optimization by the SA algorithm is introduced to fully utilize the benefit of the gate driver and the further reduction of I_C overshoot by 26% and the energy loss by 18% are achieved over the manual optimization for a Si-IGBT case. The automatic optimization method can open up a way to effectively optimize the driving waveform of power devices for the better circuit performance.

The proposed driver and the optimization method can be used as a platform for the driving waveform optimization of various power devices by providing fine tunability.

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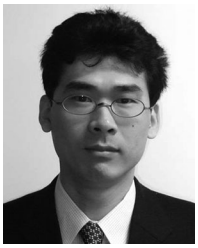

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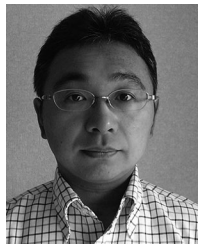

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