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Design and Analysis of Ultra-Low Power Glitch-Free Programmable Voltage Detector Based on Multiple Voltage Copier

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SUMMARY This paper presents an ultra-low power and temperature-independent voltage detector with a post-fabrication programming method, and presents a theoretical analysis and measurement results. The voltage detector is composed of a programmable voltage detector and a glitch-free voltage detector to realize both programmable and glitch-free operation. The programmable voltage detector enables the programmable detection voltages in the range from 0.52 V to 0.85 V in steps of less than 49 mV. The glitch-free voltage detector enables glitch-free operation when the supply voltage is near 0 V. A multiple voltage copier (MVC) in the programmable voltage detector is newly proposed to eliminate the tradeoff between the temperature dependence and power consumption. The design consideration and a theoretical analysis of the MVC are introduced to clarify the relationship between the current in the MVC and the accuracy of the duplication. From the analysis, the tradeoff between the duplication error and the current of MVC is introduced. The proposed voltage detector is fabricated in a 250 nm CMOS process. The measurement results show that the power consumption is 248 pW and the temperature coefficient is 0.11 mV/°C.

key words: *voltage detector, voltage reference, low power, low voltage, multiple voltage copier*

1. Introduction

Energy harvesting has attracted considerable attention since it can realize energy-autonomous applications, and many battery-free applications using energy harvesting have been proposed [1]–[5]. RF energy harvesting [6] is one of the energy harvesting approaches that produces energy from ambient RF signals. Although it can only obtain a small amount of energy, it is more stable than energy harvesting from solar and wind energy [7]. Figure 1 (a) shows a block diagram of a typical IoT node with RF energy harvesting. The antenna receives an RF signal (e.g., 920 MHz). Then, the charge pump converts the RF signal into a DC voltage (V_{DD}) and charges the output capacitor C_1. Before the energy harvesting operation starts, V_{DD} is 0 V. Once it starts, V_{DD} increases gradually with the charging current from the charge pump. Since the charging current is very small (e.g., 1 μA [8] or 1 nA [6]), during the charging period, the output switch M_1 must be turned off completely to prevent the charging current from flowing into the output load. The voltage detector (VD) monitors V_{DD} and turns the output switch M_1 on or off depending on the value of V_{DD}. Figure 1 (b) shows an operation sequence of the IoT node shown in Fig. 1 (a). At the start of the charging, V_{DD} gradually increases from 0 V since the output power of the antenna is very small. While the charge pump charges C_1, the VD keeps M_1 off. When V_{DD} reaches a predefined detection voltage (V_{DETECT}), the VD turns M_1 on and the load circuits start their operation. Since the VD is directly connected to the output node of the charge pump, it must have very low power consumption of less than 1 nA [6]. The VD must operate from 0 V without any glitch in V_{OUT}, otherwise it will mistakenly turn M_1 on and spoil the energy harvesting. Furthermore, V_{DETECT} must be robust against variation in the process, voltage, and temperature (PVT).

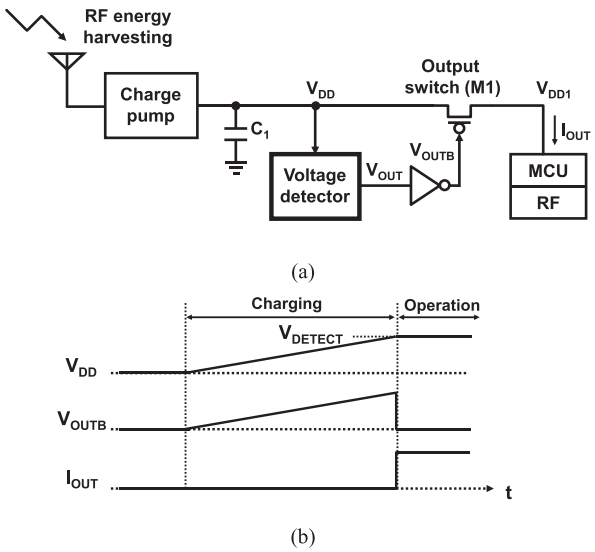

Fig. 1 Example of IoT node with RF energy harvesting. (a) Block diagram. (b) Waveform illustrating operation sequence.

In this paper, a novel circuit scheme for a VD [9] is introduced to achieve ultra-low power operation, robustness against PVT variations, and glitch-free operation at the same time. The theoretical analysis and design consideration of the proposed VD is added to [9].

This paper is organized as follows. In Sect. 2, the conventional VDs are introduced with emphasis on their problems. In Sect. 3, the concept of the proposed glitch-free and programmable VD is described. Section 4 introduces the design consideration of the proposed multiple voltage copier. Section 5 gives measurement results and a comparison with

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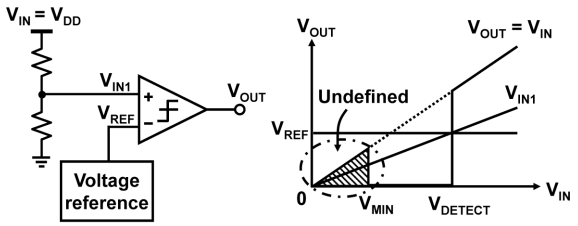
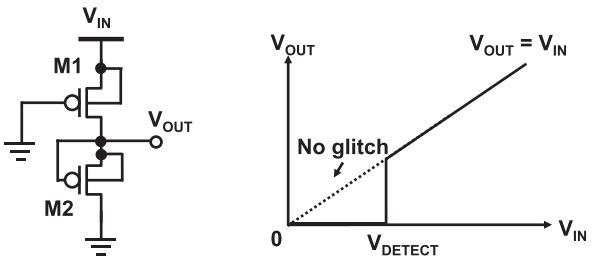


(a) (b)

Fig. 2 (a) Circuit schematic and (b) input-output characteristic of commercially available voltage detectors [10]–[12].



(a) (b)

Fig. 3 (a) Circuit schematic and (b) input-output characteristic of glitch-free voltage detector [14].

other VDs. Finally, conclusions are described in Sect. 6.

2. Issues with Conventional Voltage Detectors

2.1 Glitch-Free and Programmable Operation

Figures 2 (a) and (b) show a circuit schematic and an input-output characteristic of commercially available VDs [10]–[12], respectively. The VD is composed of a voltage divider for V_{IN}, a voltage reference generator, and a comparator. When the input voltage (V_{IN}) is lower or higher than V_{DETECT}, V_{OUT} is low or high, respectively. V_{DETECT} is expressed as follows:

$$V_{DETECT} = \frac{V_{REF}}{k} \quad (0 < k < 1), \tag{1}$$

where k is the division ratio of the voltage divider for V_{IN}. V_{REF} is the supply voltage from the voltage reference circuit. In most cases, V_{DETECT} is factory-trimmed by changing the value of k. The voltage reference circuit is an important part in that it dominates the power consumption of the VD and determines the temperature dependence of V_{DETECT}. Typical voltage reference circuit is bandgap reference (BGR), on the other hand, the power consumption of BGR is usually over 10 nW. It also limits the operation voltage of the VD since the typical minimum operation voltage of BGR is over 1 V. An ultra-low power 2-transistor voltage reference was proposed in [13]. Though it operates at 0.5 V supply voltage with sub-10 pW power consumption, V_{REF} is sensitive to the process variation because V_{REF} is determined by the threshold voltages of the transistors in the voltage reference circuit. With the voltage reference [13], the power consumption of the VD is reduced, on the other hand, V_{DETECT} varies by the process variation. Some post-fabrication programming methods are required to compensate for the variation in V_{DETECT}. In this work, a post-fabrication programming method is proposed.

Another problem of the commercially available VD is the glitch in V_{OUT}. Compared with VDs for hardware reset detection such as Brown-out Reset (BOR), VDs for energy harvesters with small output power must operate even though V_{IN} is near 0 V as mentioned in Sect. 1. The minimum operating voltage (V_{MIN}), however, is defined in commercially available VDs. As shown in Fig. 2 (b), when V_{IN} is between 0 V and V_{MIN}, V_{OUT} is undefined and sometimes

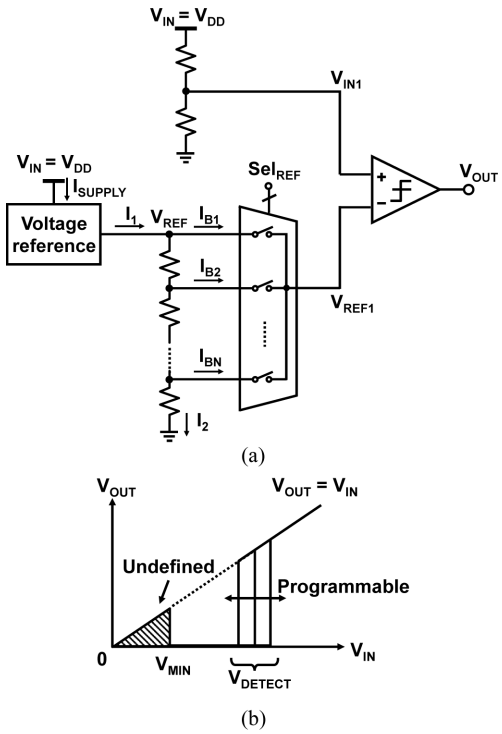


Fig. 4 (a) Circuit schematic and (b) input-output characteristic of conventional programmable voltage detector.

a glitch is generated, which spoils the power charging in the energy harvesting.

Figure 3 shows the 1.6 nW glitch-free VD proposed in [14]. As shown in Fig. 3 (b), the VD has no glitch in V_{OUT}, whereas V_{DETECT} is fixed. In addition, V_{DETECT} has a large temperature coefficient (TC) which is calculated to be 2.0 mV/°C using typical transistor parameters. In [15], a VD for miniature sensor nodes was proposed. Although the VD realized sub-1 nW operation, the programmability of V_{DETECT} was not discussed and V_{DETECT} had a large TC of 1.5 mV/°C.

2.2 Low Power and Temperature-Variation-Tolerant Operation of Programmable Voltage Detector

A simple idea for realizing a post-fabrication programmable VD is to use a voltage reference with a resistance ladder

as shown in Fig. 4. A multiplexer (MUX) which is implemented with transistor switches, selects the output voltage of the programmable voltage reference to achieve a suitable V_{DETECT}. The problem of the scheme, however, is that there is a tradeoff between the temperature dependence of the output voltage of the programmable voltage reference (V_{REF1}) and the power consumption required to generate V_{REF1}. Ideally, the MUX has no leakage current, that is, I_{B1}, I_{B2}, and $I_{BN} = 0$ and $I_1 = I_2$. Then, the TC of V_{REF1} is equal to that of V_{REF}. In reality, the switches in the MUX have leakage currents [16]. Without a sufficient I_1, the temperature dependence of V_{REF1} is inferior to that in the ideal case. The voltage reference must drive a large I_1, which causes an increase in the power consumption of the voltage reference. The TC of V_{REF1} and the power consumption of the voltage reference have a tradeoff relationship. The tradeoff is later quantitatively shown in Fig. 14.

3. Proposed Glitch-Free Programmable Voltage Detector

3.1 Glitch-Free and Programmable Operation

Figures 5 (a) and (b) show a block diagram and the concept of the proposed glitch-free programmable VD, respectively. As shown in Fig. 5, by combining the programmable VD with the glitch, and the glitch-free VD with a fixed V_{DETECT}, both glitch-free and programmable operation are achieved when $V_{MIN} < V_{DETECT2} < V_{DETECT1}$, where $V_{DETECT1}$ and $V_{DETECT2}$ are the detection voltages of the programmable VD and the glitch-free VD respectively. Table 1 summarizes the four VDs regarding their programmability and glitch-free operation. Figure 6 shows a schematic of the entire circuit of the proposed VD. All MOSFETs operate in the subthreshold region, which enables the ultra-low power consumption of the proposed VD. The body node and the source

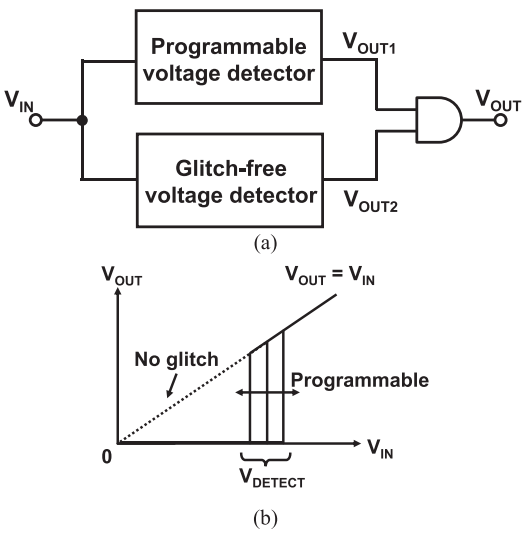


Fig. 5 (a) Block diagram and (b) concept of proposed glitch-free programmable voltage detector.

node are shorted in pMOSFETs in the proposed VD to avoid the body effect. Assuming that the proposed VD is applied to the RF energy harvesting shown in Fig. 1, the output node of the VD (V_{OUTB}) is designed to be high/low when V_{IN} is lower/higher than V_{DETECT}. In the proposed programmable VD, the voltage reference is implemented with two stacked pMOSFETs with different threshold voltages (V_{TH}), which is a similar concept to that in [13], in which two stacked nMOSFETs with different values of V_{TH} are implemented. The V_{TH} difference is approximately 0.4 V. In our design, the target V_{DETECT} is set to 0.7 V. On the other hand, from the corner analysis in the SPICE simulation, the target V_{DETECT} varies ±60 mV with the process variation of the pMOSFETs. Then, the programmability in V_{DETECT} is set to cover the effect of the process variation. To reduce the step of the programmable V_{DETECT}, voltage dividers are added to both V_{IN} and V_{REF}. The MUX in the proposed VD adopts low-V_{TH} MOSFETs as the switches to enable the low voltage operation of the VD and achieve the low voltage V_{DETECT}. When V_{IN} is lower voltage than the V_{TH} of the low-V_{TH} MOSFET, the programmable VD does not operate properly, which causes the glitch in V_{OUT1}. On the other hand, the glitch in V_{OUTB} is removed thanks to the glitch-free VD.

In this work, a glitch-free temperature-variation-tolerant VD is newly proposed. As shown in Fig. 6, the VD is composed of two stacked pMOSFETs M_8 and M_9 with different V_{TH}. When V_{IN} is lower than $V_{DETECT2}$, the current on M_9 (I_9) is much larger than the current on M_8 (I_8), then V_{OUT2} is kept to 0 V. As V_{IN} increases, I_8 increases exponentially, and once I_8 exceeds I_9, the voltage level of V_{OUT2} changes from 0 V to V_{IN}. At the point, the drain to source voltages of M_8 and M_9 are over $3V_T$. The currents of M_8 and M_9 are expressed as follows [17]:

$$I_8 = \mu_8 C_{OX8} \frac{W_8}{L_8} V_T^2 \exp\left(\frac{V_{IN} - |V_{TH8}|}{m_8 V_T}\right), \quad (2)$$

$$I_9 = \mu_9 C_{OX9} \frac{W_9}{L_9} V_T^2 \exp\left(\frac{-|V_{TH9}|}{m_9 V_T}\right), \quad (3)$$

where m_8 (m_9), V_{TH8} (V_{TH9}), and μ_8 (μ_9) are the body-effect coefficient, the threshold voltage of transistor M_8 (M_9), and the mobility of the transistor, respectively. V_T is the thermal voltage (= k_BT/q), k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. W_8

Table 1 Summary of four voltage detectors.

		Glitch-free V_{OUT}	Programmable V_{DETECT}
Conventional	Commercial VD (Fig. 2)	No	No
	Glitch-free VD (Fig. 3)	Yes ✓	No
	Programmable VD (Fig. 4)	No	Yes ✓
Proposed glitch-free programmable VD (Fig. 5)		Yes ✓	Yes ✓

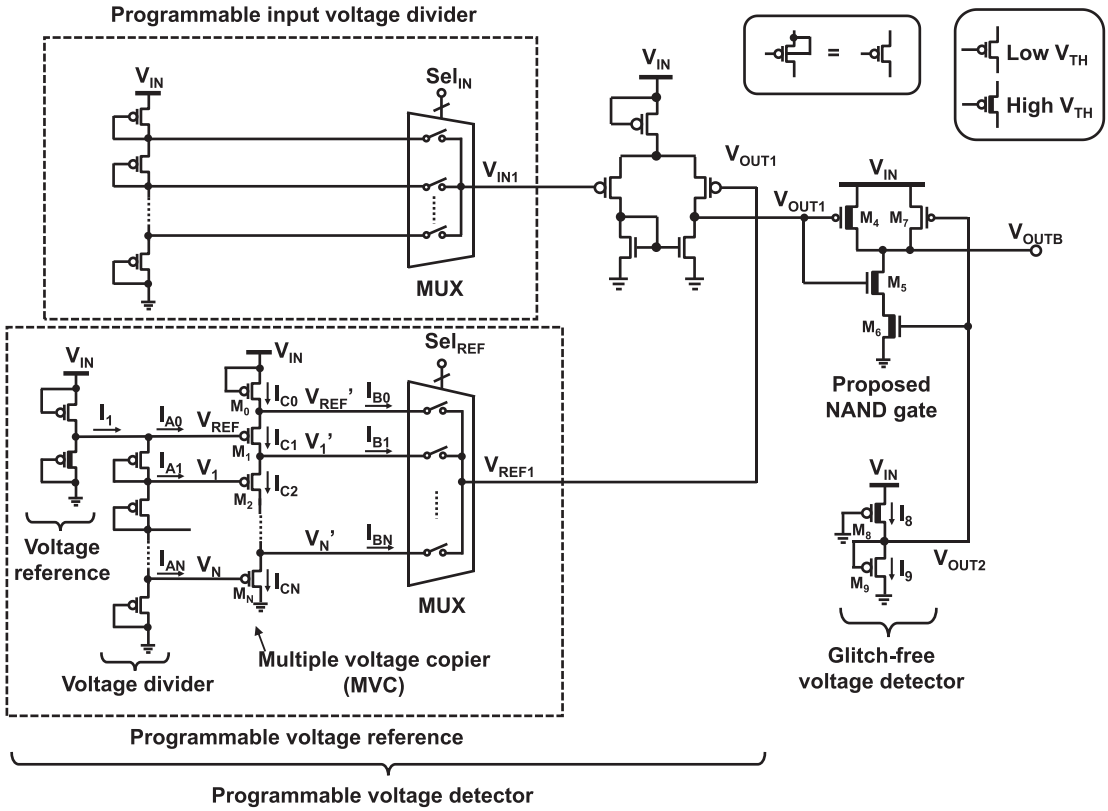


Fig. 6 Schematic of circuit proposed glitch-free programmable voltage detector.

(W_9) and L_8 (L_9) are the gate width and length of each transistor and C_{OX8} (C_{OX9}) is the gate capacitance per unit area of each transistor. From (2) and (3), $V_{DETECT2}$ is calculated as follows.

$$V_{DETECT2} = \left(|V_{TH8}| - \frac{m_8}{m_9}|V_{TH9}|\right) + m_8 V_T \ln\left(\frac{\mu_9 C_{OX9} W_9 L_8}{\mu_8 C_{OX8} W_8 L_9}\right) \quad (4)$$

In (4), by sizing M_8 and M_9 properly, the temperature dependence of the $V_{DETECT2}$ can be mitigated since the TC of the first and the second terms are opposite characteristics [18]. In our design, the sizing ratio of the glitch-free VD (W_9L_8/W_8L_9) is decided by the SPICE simulation to minimize the temperature dependence of the $V_{DETECT2}$. $V_{DETECT2}$ is expressed as about the difference of threshold voltages between high-V_{TH} pMOSFET and low-V_{TH} pMOSFET. Figure 7 shows the input-output characteristics of the glitch-free temperature-tolerant VD obtained by SPICE simulation. The simulated TC of $V_{DETECT2}$ is less than 0.1 mV/°C.

The conventional AND or NAND gate for the VD shown in Fig. 5 (a) has a minimum operating voltage (V_{MIN2}) [19] which may cause a glitch in V_{OUTB}. To eliminate this possibility, a new NAND gate is proposed as shown in Fig. 6. Using the proposed NAND gate, V_{OUTB} is fixed to V_{IN} when $V_{IN} < V_{MIN2}$. The NAND gate is composed of M_4, M_5, and M_6, which are high-V_{TH} transistors, and M_7,

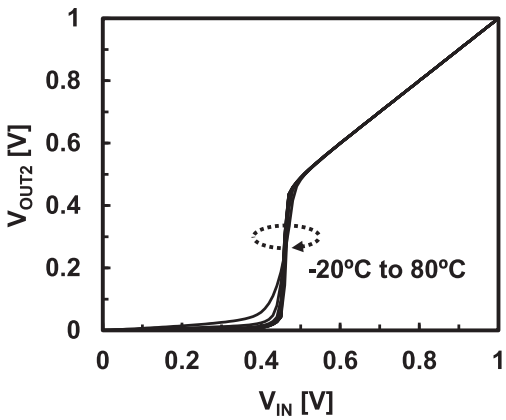


Fig. 7 Input-output characteristics of proposed glitch-free voltage detector obtained by SPICE simulation.

which is a low-V_{TH} transistor. When V_{IN} is 0 V, the gate-to-source voltage of all the transistors is 0 V, then the leakage current of M_7 is much larger than the currents in the other transistors because V_{TH} of M_7 is lower than that for other transistors. While V_{IN} is increasing, the leakage current on M_7 increases V_{OUTB} to V_{IN}. Figure 8 shows the input-output characteristics of the proposed VD with a conventional NAND gate and with the proposed NAND gate, obtained by SPICE simulation. With the conventional NAND gate, a glitch is generated in V_{OUTB} when V_{IN} is less than 0.5 V. In contrast, the glitch in V_{OUTB} is removed with the

proposed NAND gate.

3.2 Multiple Voltage Copier for Low Power and Temperature-Variation-Tolerant Programmable Operation

To solve the tradeoff between the power consumption and the temperature dependence of the programmable voltage detector as described in Sect. 2, a multiple voltage copier (MVC) is newly proposed and inserted between the voltage divider used for the voltage reference and the MUX. The MVC is a multiple-input and multiple-output voltage buffer. In the MVC in Fig. 6, M_0 is the current source with a subthreshold leakage current ($V_{GS} = 0$) of I_{C0}, and the other transistors (M_1, M_2, and M_N) are serially stacked. The source currents (I_{C0}, I_{C1}, I_{C2}, and I_{CN}) are sufficiently larger than the leakage currents (I_{B0}, I_{B1}, and I_{BN}) of the switches to avoid the voltage drop and the temperature dependence of selectable output nodes (V'_{REF}, V'_1, and V'_N). Then, an interesting characteristic of the MVC is that each input voltage is equal to each output voltage ($V_{REF} = V'_{REF}$, $V_1 = V'_1$, and $V_N = V'_N$) because $I_{C0} = I_{C1} = I_{C2} = I_{CN}$ and $V_{GS} = 0$ for all transistors in the MVC. Thus, in the MVC, multiple input voltages are simultaneously copied to multiple output voltages. The power overhead of the MVC is 56 pW at 0.8 V.

In Fig. 4 (a) and Fig. 6, the supply currents for the voltage references must be sufficiently larger than I_1 to eliminate the voltage drop and the temperature dependence of each V_{REF}. By inserting the MVC between the voltage divider and the MUX in Fig. 6, $I_{A0} = I_{A1} = I_{AN} = 0$ and I_1 can be greatly reduced compared with I_1 in Fig. 4 (a), which enables the power reduction in the voltage reference in Fig. 6. Thus, the tradeoff between the power consumed to generate V_{REF1} and the temperature dependence of V_{REF1} in the conventional programmable VD is solved by using the MVC. In the SPICE simulation, the current on MVC is set to 10 times larger than the amount of the leakage currents of the MUX in the target temperature range.

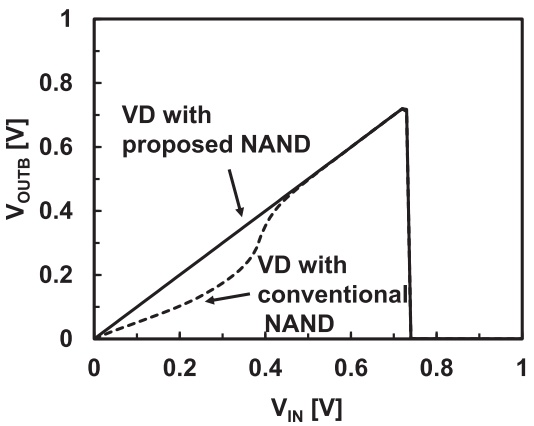


Fig. 8 Input-output characteristic of voltage detector with or w/o proposed NAND obtained by SPICE simulation.

4. Design Consideration and Theoretical Analysis of MVC

In the Sect. 3, the MVC was newly proposed as a multiple-input and multiple-output voltage buffer. Ideally, the MVC copies multiple input voltages to the multiple output nodes simultaneously without any duplication errors. In fact, owing to the load current in each output node, a slight error, which is the difference between the input voltage and output voltage, is generated in the duplication. The duplication error is dependent on the current in the MVC and the load current in each output node. In this section, the design consideration and a theoretical analysis of the MVC are introduced to clarify the relationship between the current in the MVC and the accuracy of the duplication.

The model used for the analysis is shown in Fig. 9. $\Delta V_i = V'_i - V_i$ ($i = 1, 2, \ldots, N$) is the duplication error in each output node. Assuming that each transistor is sufficiently large, the effect of random variation is neglected. To simplify the analysis, each load current is assumed to be the same ($I_{O1} = I_{O2} = \ldots I_{ON} = I_O$). Assuming for V_{DS} of each transistor is sufficiently large ($> 3V_T$), the drain currents of M_0 and M_i are expressed as follows:

$$I_{D0} = I_S \exp\left(\frac{-|V_{TH}|}{mV_T}\right), \tag{5}$$

$$I_{Di} = I_{D0} - \sum_{k=1}^{i} I_{Ok} = I_S \exp\left(\frac{\Delta V_i - |V_{TH}|}{mV_T}\right). \tag{6}$$

where

$$I_S = \mu C_{OX} \frac{W}{L} V_T^2, \tag{7}$$

where μ and C_{OX} are the mobility and gate capacitance of

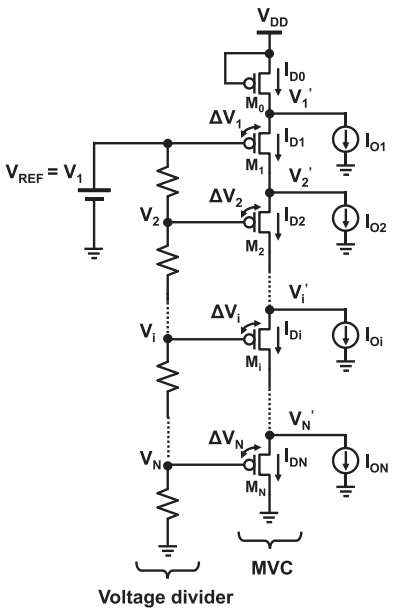


Fig. 9 Circuit schematic of MVC for theoretical analysis.

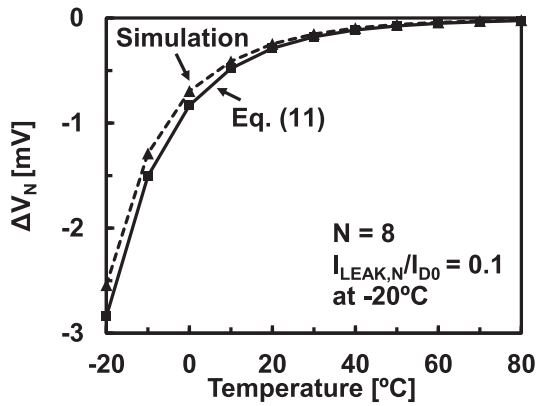


Fig. 10 Comparison of SPICE simulation result and (11) for temperature dependence of ΔV_N when N = 8 and $I_{LEAK,N}/I_{D0}$ = 0.1 at temperature of −20°C.

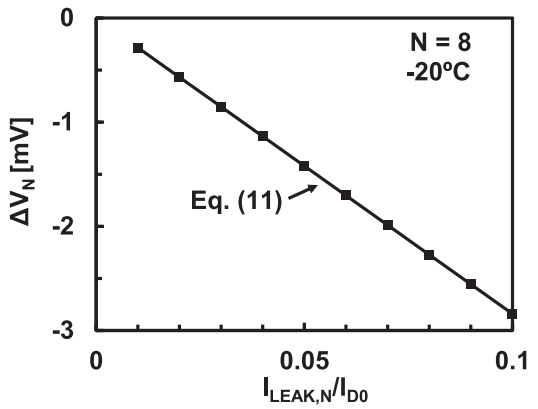


Fig. 11 Dependence of ΔV_N on supply current to load current ratio ($I_{LEAK,N}/I_{D0}$) obtained by SPICE simulation and (11) when N = 8 and temperature is −20°C.

the transistor respectively. From (5) and (6), the ratio of I_{D0} to I_{Di} is

$$\frac{I_{Di}}{I_{D0}} = \exp\left(\frac{\Delta V_i}{mV_T}\right) = 1 - \frac{I_{LEAK,i}}{I_{D0}}, \tag{8}$$

where

$$I_{LEAK,i} = \sum_{k=1}^{i} I_{Ok}. \tag{9}$$

From (8) and (9), ΔV_i is given as follows.

$$\Delta V_i = mV_T \ln\left(1 - \frac{I_{LEAK,i}}{I_{D0}}\right) \tag{10}$$

When $I_{LEAK,i}/I_{D0}$ is sufficiently small (< 0.1), ΔV_i is approximated as

$$\Delta V_i \approx -mV_T \frac{I_{LEAK,i}}{I_{D0}}, \tag{11}$$

From (11), the conditions for the worst ΔV_i are introduced.

1) The absolute value of the duplication error ($|\Delta V_i|$) is the largest when i = N. That is, designers have to consider ΔV_N to evaluate the worst duplication error in the MVC.
2) The TC of ΔV_i is positive as shown in Fig. 10 since the temperature dependence of $-1/I_{D0}$ is dominant in (11). It implies that the $|\Delta V_i|$ is the largest at the lowest temperature in the designer's target temperature range.

To verify the consistency of the analysis, SPICE simulations were conducted. Figure 10 shows a comparison of the SPICE simulation results for the temperature dependence of ΔV_N in the target range of −20°C to 80°C with that given by (11). The body-effect coefficient m is determined from the characteristics of the pMOSFET at −20°C in the SPICE simulation. $I_{LEAK,N}/I_{D0}$ is set to 0.1 at −20°C. The SPICE simulation results are in agreement with (11) within an error of 11%. The simulation results and (11) show that the TC of ΔV_N is positive and that the largest $|\Delta V_N|$ occurs at the lowest temperature in the target range. From (11), ΔV_N and I_{D0} have a tradeoff relationship. Figure 11 shows the relationship between $I_{LEAK,N}/I_{D0}$ and ΔV_N. ΔV_N is proportional to $I_{LEAK,N}/I_{D0}$. This means that to reduce the duplication error in the MVC to within a certain voltage, the MVC requires a sufficient value of I_{D0}. To maintain the duplication error in the MVC (= ΔV_N) below ΔV_{URS}, the following equation must be satisfied:

$$I_{D0} \geq I_{D0,min} = \frac{mk_B T_{MIN} I_{LEAK,N}}{q} \frac{1}{\Delta V_{URS}}, \tag{12}$$

where T_{MIN} is the lowest target temperature and ΔV_{URS} is the acceptable error defined by designers. Equation (12) means that once T_{MIN}, $I_{LEAK,N}$, and ΔV_{URS} are defined by designers, the optimum I_{D0} (= $I_{D0,min}$) is automatically given by (12).

5. Measurement Results

A test chip is fabricated in a 2.5 V 250 nm CMOS process. Figure 12 shows a chip photograph of the proposed VD. The core area is 76 μm by 120 μm.

Figure 13 shows the simulated and measured input-output characteristics of V_{OUT1}, V_{OUT2}, and V_{OUTB} for the proposed glitch-free programmable VD in Fig. 6. When V_{IN} is near 0 V, there is a glitch in V_{OUT1}. Owing to the combination of the glitch-free VD and the programmable VD, the glitch is removed from V_{OUTB}. The voltage level of V_{OUTB} is maintained at V_{IN} when V_{IN} is lower than V_{DETECT}. To clarify the tradeoff between the power consumed to generate V_{REF1} and the temperature dependence of V_{REF1}, Fig. 14 shows the power supply current dependence of the TC for V_{REF1} with and without the MVC. For V_{REF1} without the MVC, the results are obtained by SPICE simulation of the circuits in Fig. 4 (a), where the voltage reference shown in Fig. 6 is used and the transistor gate width of the voltage reference is varied to change I_1 in the simulation. As the power supply current is reduced, the TC increases, which indicates a tradeoff between the power consumption and the TC. A measured result is shown for

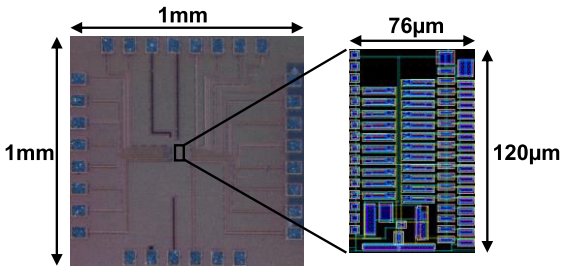


Fig. 12 Die photograph and layout of proposed glitch-free programmable voltage detector fabricated in 250 nm CMOS process.

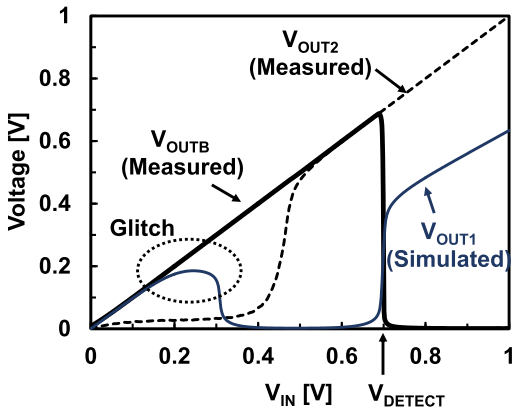


Fig. 13 Simulated and measured input-output characteristics of proposed glitch-free programmable voltage detector.

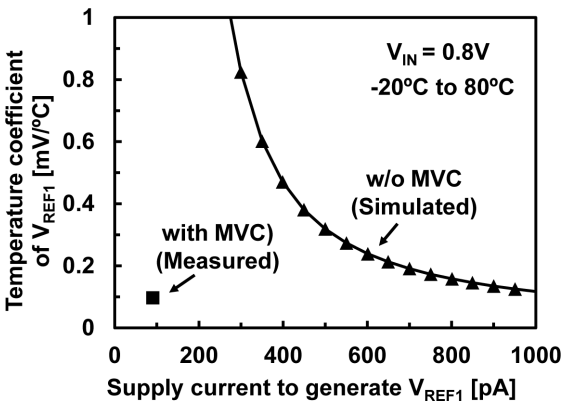


Fig. 14 Power supply current dependence of temperature coefficient for V_{REF1} with and without proposed multiple voltage copier (MVC).

V_{REF1} with the MVC. By introducing the MVC, the trade-off is solved, and both a low supply current (92 pA) and a low TC (0.10 mV/°C) are simultaneously achieved. Figure 15 shows the measured programmable V_{DETECT} in the proposed glitch-free programmable VD. The programmable range of V_{DETECT} is from 0.52 V to 0.85 V in steps of less than 49 mV. The programming step ensures the safe operating tolerance V_{DD} of ±5% in the load circuit. Figure 16 (a) shows the measured temperature dependence of V_{DETECT} for five dies. Figure 16 (b) shows the change of V_{DETECT} normalized by the values at 25°C. The measured TC of V_{DETECT}

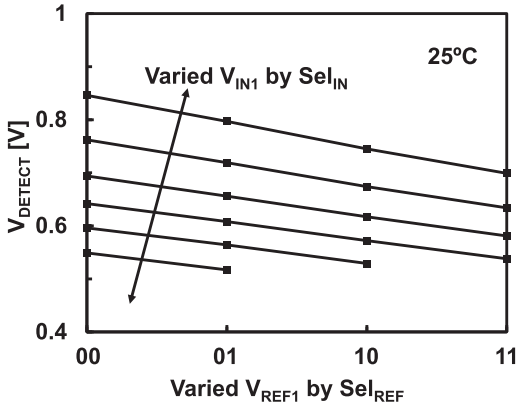
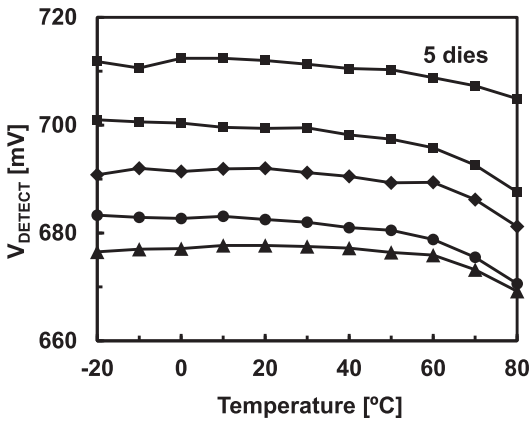
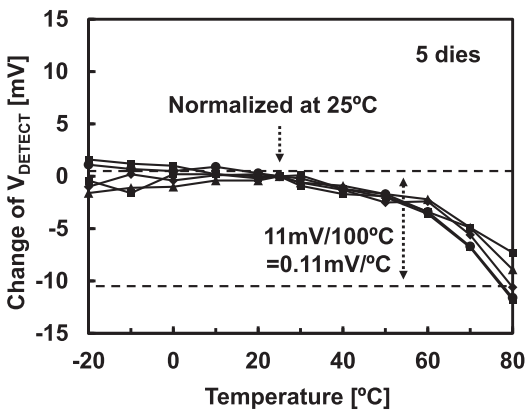


Fig. 15 Measured programmable V_{DETECT} in proposed glitch-free programmable voltage detector.



(a)



(b)

Fig. 16 (a) Measured temperature dependence of V_{DETECT} for five dies of proposed glitch-free programmable voltage detector and (b) change of V_{DETECT} normalized by the values at 25°C.

is 0.11 mV/°C from −20°C to 80°C. The cause of the negative TC is assumed to be the temperature characteristics of the 2-transistors voltage reference. The measured V_{TH} of the pMOSFETs in the VD is slightly higher than it was expected, which causes the negative temperature dependence

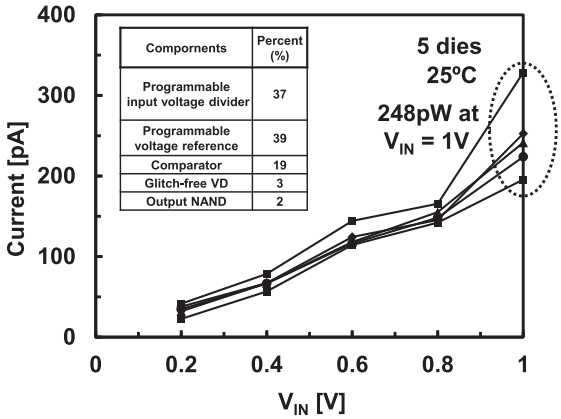


Fig. 17 Measured power consumption for five dies of proposed glitch-free programmable voltage detector.

Table 2 Comparison with conventional VDs.

		TPS3839 [10]	AP4400A [12]	JSSC'12 [14]	VLSI'12 [15]	This Work
CMOS process		N/A	N/A	65nm	180nm	250nm
Operating supply voltage	Max	6.5V	5.5V	N/A	N/A	1.0V
	Min	0.9V	0.8V	0V		0V
Detection voltage (V_{DETECT})	Max	4.38V	4.2V	0.46V (Fixed)	3.58V (Fixed)	0.85V
	Min	0.9V	2.0V			0.52V
	Step	> 150mV (Trimming)	100mV (Trimming)			< 49mV (Programmable)
Power (25°C)		180nW @1.2V	68nW @3.4V	1.6nW @0.46V	286pW @3.6V	248pW @1.0V
Temperature coefficient of V_{DETECT}		0.055mV/°C	0.75mV/°C	2.0mV/°C (Calculated)	1.5mV/°C	0.11mV/°C
Temperature range		-40°C to 85°C	-15°C to 85°C	N/A	0°C to 80°C	-20°C to 80°C

of V_{REF} and V_{DETECT} in our design. Other assumed reason for the negative TC is the mismatch in the comparator. It is improved by enlarging the size of transistors. Figure 17 shows the power consumption of the proposed VD for five dies and the breakdown of the power consumption. The power consumption is 248 pW at V_{IN} = 1.0 V. The current increases almost linearly in 0 V to 1 V range. The V_{IN} dependence is caused by the current in the input voltage divider. The subthreshold current in the voltage divider increases exponentially with the increase of the gate to source voltage of each transistor. On the other hand, by stacking a lot of transistor diodes for the voltage divider, the change of the gate to source voltage of each transistor is slight against the change of V_{IN}. It causes the linear increase of the power consumption of the VD in the range. In Table 2, the results of this work are compared with those for previously published VDs. In this work, the operating supply voltage is defined as the voltage region where the VD does not generate a glitch in the output node. We achieve a minimum operating voltage of 0 V owing to the glitch-free operation, which is essential for energy harvesting. We have demonstrated a programmable VD with steps of less than 49 mV to compensate for a die-to-die variations. The proposed MVC enables a programmable VD with the lowest reported power of 248 pW and a competitive TC of 0.11 mV/°C.

6. Conclusion

In this paper, an ultra-low power, glitch free, and PVT-variation-tolerant voltage detector (VD) is proposed and implemented in a 250 nm CMOS process. This is the first report of an ultra-low power glitch-free programmable VD. The proposed VD is composed of a programmable VD and a glitch-free VD. All MOSFETs operate in the subthreshold region to reduce the power consumption of the VD. Owing to the proposed glitch-free VD and a novel NAND gate, the glitch of the proposed VD is removed. To realize a programmability in the VD with little power loss, a multiple voltage copier (MVC) for the programmable VD is proposed. It operates as a multiple-input and multiple-output voltage buffer, which copies the input voltage level to the output node. It solves the tradeoff between the power consumption of the programmable VD and the temperature dependence of V_{DETECT}. The power consumption of the MVC is 56 pW. From the measurement results, the power consumption decreases without the deterioration of the temperature dependence in the programmable VD when the MVC is used. In this work, the design consideration and a theoretical analysis of the MVC are introduced to clarify the relationship between the current in the MVC and the accuracy of the duplication. From the analysis, a tradeoff between the duplication error and the current of the MVC is demonstrated. Measurement results show that the power consumption of the proposed VD is 248 pW. This is the lowest power consumption ever reported for a VD. The temperature coefficient (TC) has a competitive value of 0.11 mV/°C. The steps of the programmable detection voltage are less than 49 mV while its range is from 0.52 V to 0.85 V. The presented VD is expected to be particularly advantageous for applications that require power consumption of less than 1 nW such as energy-harvesting systems.

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