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Power Electronics 2.0: IoT-Connected and AI-Controlled Power Electronics Operating Optimally for Each User

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***Abstract*—The emerging trend of internet of things (IoT) and artificial intelligence (AI) technologies will bring about a major change in power electronics and create a new generation of the power electronics (Power Electronics 2.0). To enable the IoT- and AI-assisted Power Electronics 2.0, the integration of the sensors, the programmable hardware, and VLSIs for the controller into the power devices/modules is very important. In this paper, a 6-bit programmable gate driver IC with automatic optimization of gate driving waveform for IGBT is presented as the first step toward Power Electronics 2.0. In the proposed gate driver, the 6-bit gate control signals with four 160-ns time steps are globally optimized using a simulated annealing algorithm, reducing the collector current overshoot by 37% and the switching loss by 47% at the double pulse test of 300V, 50A IGBT. The gate driver is also applied to a half-bridge inverter, where the gate driving waveform is changed depending on the load current.**

Keywords—IoT, AI, power electronics, programmable, gate driver, IGBT

I. INTRODUCTION

The emerging trend of internet of things (IoT) and artificial intelligence (AI) technologies will bring about a major change in power electronics and create a new generation of the power electronics (Power Electronics 2.0). Fig. 1(a) shows a conventional power electronics (Power Electronics 1.0). Ready-made power devices are provided from the power device manufacturers to the power device users. The power device manufacturers do not know the real usage conditions of the power devices of each user. Each power device user has no choice but to use the ready-made power devices, which results in the mismatch between the user's real requirements and the specification of the ready-made power devices. IoT and AI technologies will fill the gap between the power device manufacturers and the power device users. Fig. 1(b) shows the proposed Power Electronics 2.0. In IoT area, by embedding a wide variety of massive sensors into the power devices/modules and transmitting the measured data to the power device manufacturers through the Internet, the power device manufacturers and the power device users are directly connected and the power device manufacturers can monitor real operating conditions of the power devices for each user. In AI area, by analyzing the big sensor data from multiple users using AI, the power device manufacturers can provide customer-tailored services for each user, which provides new

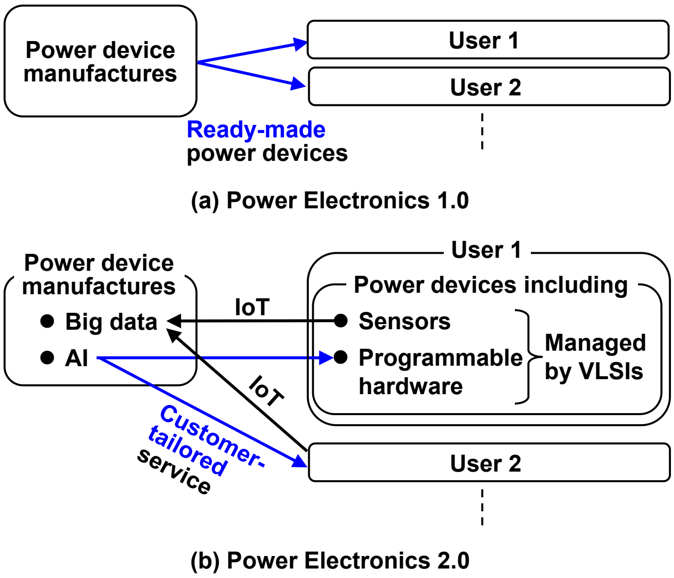

Fig. 1. (a) Conv. Power Electronics 1.0. (b) New Power Electronics 2.0.

business opportunities to the power device manufacturers. Each power device user can enjoy the customer-tailored service and the power devices operate optimally for each user by tuning the parameters in the programmable hardware with digital interfaces. To enable the IoT- and AI-assisted Power Electronics 2.0, the integration of the sensors, the programmable hardware, and VLSIs for the controller into the power devices/modules is very important. In this paper, a 6-bit programmable gate driver IC with automatic optimization of gate driving waveform for IGBT is presented as the first step toward Power Electronics 2.0. The gate driver IC is an important circuit bridging the voltage gap between VLSIs operating less than 5V and the power electronics operating above 100V. In the proposed gate driver, the 6-bit gate control signals with four 160-ns/400-ns time steps are globally optimized using a simulated annealing algorithm. The gate driver is also applied to a half-bridge inverter, where the gate driving waveform is changed depending on the load current.

II. TRADE-OFF IN GATE DRIVERS FOR IGBT

Gate driving waveform optimization of power devices for reducing energy loss without inducing large current or voltage

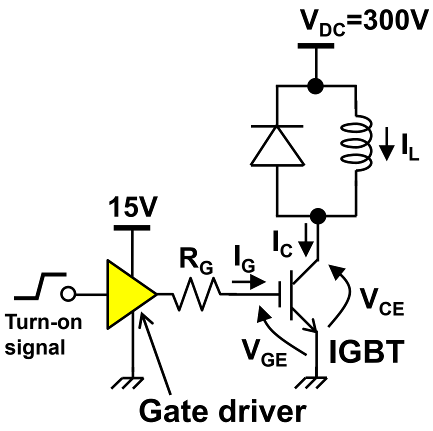

Fig. 2. Conventional gate driver for IGBT.

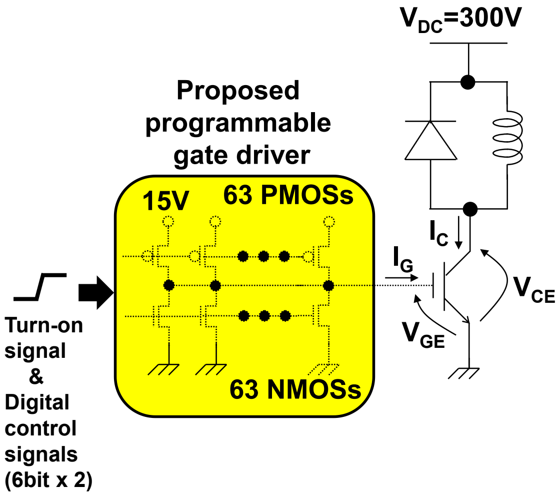

Fig. 3. Proposed programmable gate driver with digital control signals for IGBT.

overshoot has been attracting attention [1-7]. Fig. 2 shows a conventional gate driver with a gate resistor (R_G) for IGBT. Fig. 3 shows the proposed programmable gate driver with digital control signals for IGBT [8]. In order to realize programmable 63-level drivability, 63 parallel drivers are connected to the gate of IGBT and a 6-bit binary control signal is applied to specify the number of activated PMOS (NMOS) driver transistors. Fig. 4 show a trade-off between the switching loss (E_{LOSS}) and the collector current overshoot ($I_{OVERSHOOT}$) at the turn-on of IGBT. In the conventional gate driver, E_{LOSS} and $I_{OVERSHOOT}$ are the trade-off, because large E_{LOSS} and small $I_{OVERSHOOT}$ is obtained at large R_G, while small E_{LOSS} and large $I_{OVERSHOOT}$ is obtained at small R_G. In contrast, in the proposed programmable gate driver, the trade-off is solved by temporally reducing the gate current (I_G) using the programmable I_G to reduce $I_{OVERSHOOT}$. Therefore, the precise control of I_G with a fine timing resolution is required.

III. PROGRAMMABLE GATE DRIVER IC

Fig. 5 shows a circuit schematic of the proposed programmable gate driver IC [8]. A 6-bit binary control signal, B_{PMOS} (B_{NMOS}), is applied to specify the number of activated PMOS (NMOS) driver transistors, n_{PMOS} (n_{NMOS}). A pair of 6-

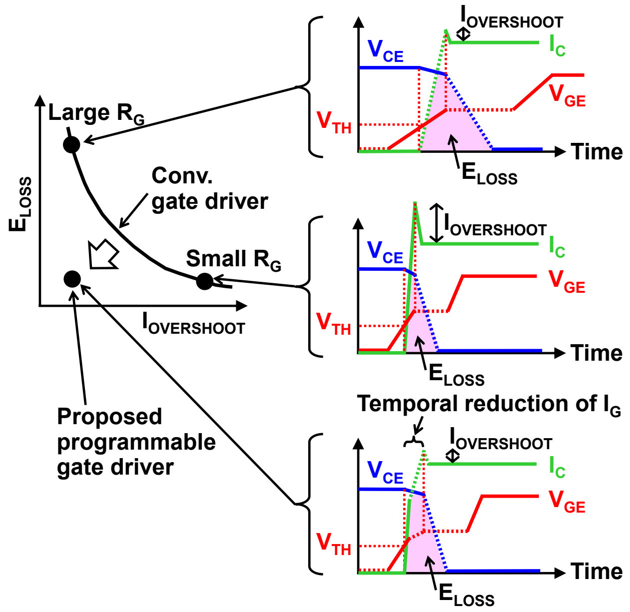

Fig. 4. Trade-off between E_{LOSS} and $I_{OVERSHOOT}$ at turn-on of IGBT.

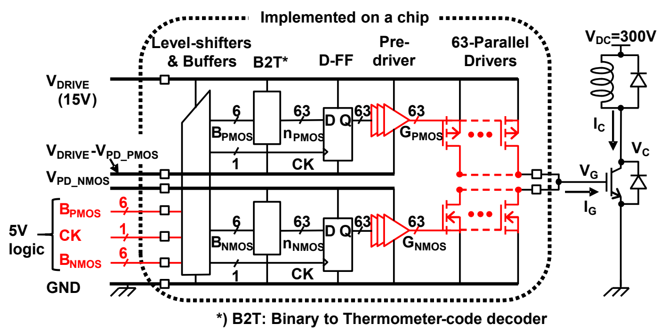

Fig. 5. Circuit schematic of the proposed programmable gate driver IC.

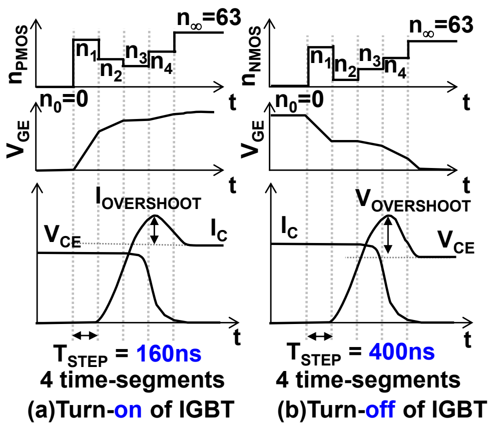

Fig. 6. Schematic of gate driving waveforms. (a) Turn-on. (b) Turn-off.

bit signals (B_{PMOS} and B_{NMOS}) are latched by the clock (CK) and activate the final 63 PMOS (NMOS) transistors. Fig. 6 shows a schematic of gate driving waveforms with 4 time-segments. The programmable gate driver IC accepts a sequence of n_{PMOS} and a sequence of n_{NMOS} as the control inputs and changes the output drivability accordingly. Any strength of drivability from 0 to 63 (x 12-mA for both of PMOS and

NMOS) can be chosen for each of the 4 time-segments, that is, n_1, n_2, n_3, and n_4 in Fig. 6 can be any of integers from 0 to 63. The time step (T_{STEP}) is set to 160ns and 400ns for turn-on and turn-off of IGBT, respectively. A programmable gate driver IC with 150-ps T_{STEP} and 15-bit control is also reported for the fast switching GaN power devices [9-10].

In the waveform optimization process, 64^4 (~1.7 x 10^7) different waveforms need to be tried for an exhaustive search, which is impractical. The machine-based optimization using the simulated annealing algorithm [11] is proposed to make the optimization practical. The details of the automatic optimization method is shown in [12]. The objective is to reduce E_{LOSS} and $I_{OVERSHOOT}$ for the turn-on case (the overshoot of V_{CE}, $V_{OVERSHOOT}$, for the turn-off case). In order to achieve this goal, at first, the energy loss and the overshoot values are normalized as below.

$$E'_{LOSS} = \frac{E_{LOSS} - E_{LOSS,MIN}}{E_{LOSS,MAX} - E_{LOSS,MIN}} \quad (1)$$

$$I'_{OVERSHOOT} = \frac{I_{OVERSHOOT} - I_{OVERSHOOT,MIN}}{I_{OVERSHOOT,MAX} - I_{OVERSHOOT,MIN}} \quad (2)$$

$$V'_{OVERSHOOT} = \frac{V_{OVERSHOOT} - V_{OVERSHOOT,MIN}}{V_{OVERSHOOT,MAX} - V_{OVERSHOOT,MIN}} \quad (3)$$

where ' signifies the normalized quantity and the subscript MIN (MAX) signifies the minimum (maximum) of the corresponding quantity. For example, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate driving waveform is the fastest, that is, all of n_1, n_2, n_3, n_4, and n_∞ are 63. On the other hand, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate drive waveform is the slowest, that is, all of n_1, n_2, n_3, n_4, and n_∞ are 1. After the normalization, all of the normalized quantities vary between 0 and 1. The object functions ($f_{OBJECT(ON)}$ for turn-on of IGBT and $f_{OBJECT(OFF)}$ for turn-off of IGBT) to be minimized in the optimization using the simulated annealing is set as below.

$$f_{OBJECT(ON)} = \sqrt{E'^{\,2}_{LOSS} + I'^{\,2}_{OVERSHOOT}} \quad (4)$$

$$f_{OBJECT(OFF)} = \sqrt{E'^{\,2}_{LOSS} + V'^{\,2}_{OVERSHOOT}} \quad (5)$$

IV. MEASURED IGBT SWITCHING

Fig. 7 shows a photo of the developed programmable gate driver PCB attached on an IGBT module (600V, 100A rating). The proposed programmable gate driver IC is fabricated with 40V, 0.18µm BCD process. The core size is 2300µm by 730µm. Both turn-on and turn-off characteristics of IGBT are measured with a 300-V double-pulse setup with the load current of 50A.

The proposed automatically optimized gate waveforms are compared with the conventional single-step gate waveforms. Fig. 8 shows the measured E_{LOSS} and $I_{OVERSHOOT}$ of the conventional single-step gate waveforms and the proposed automatically optimized gate waveforms at the turn-on of IGBT. The dotted concentric curves show the contour of $f_{OBJECT(ON)}$ defined in Eq. (4). $E_{LOSS,\,MAX}$ and $E_{LOSS,\,MIN}$ in Eq. (1) and $I_{OVERSHOOT,\,MAX}$ and $I_{OVERSHOOT,\,MIN}$ in Eq. (2) are shown in Fig. 8. In the conventional single-step gate waveforms, E_{LOSS} and $I_{OVERSHOOT}$ are the trade-off. In contrast, the proposed automatically optimized gate waveform solves the trade-off. Compared with the conventional waveforms, the proposed

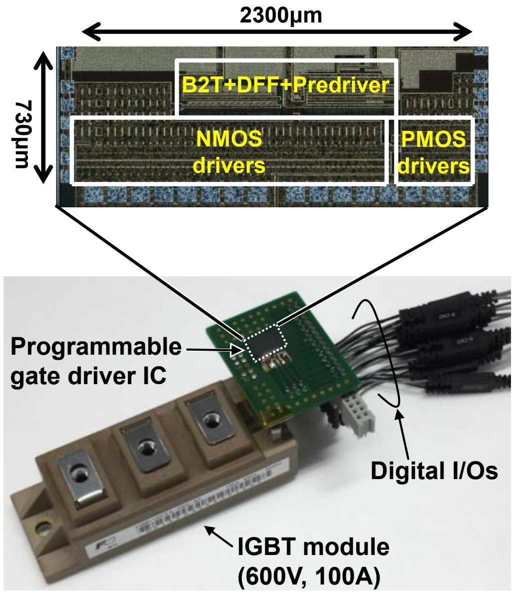

Fig. 7. Photo of developed programmable gate driver attached on IGBT module.

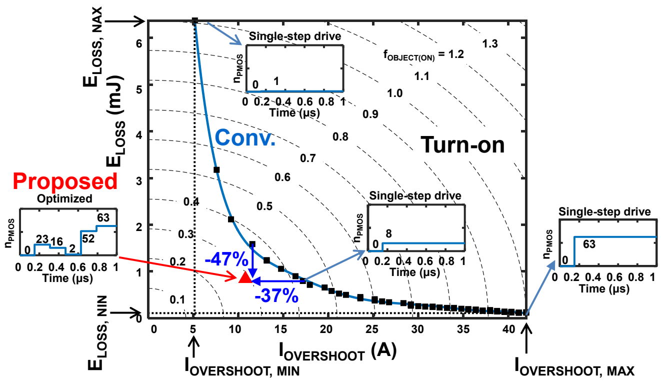

Fig. 8. Measured E_{LOSS} and $I_{OVERSHOOT}$ at turn-on of IGBT.

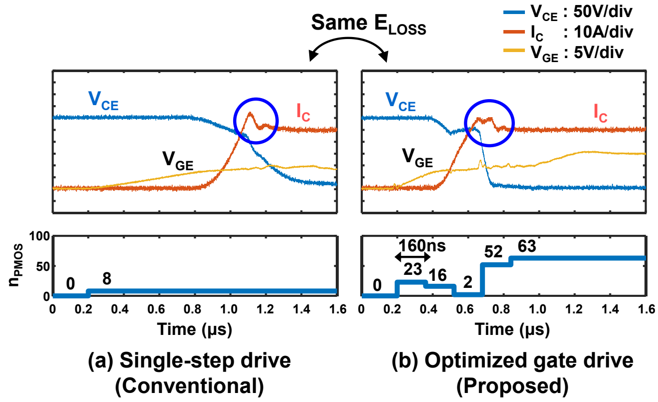

Fig. 9. Measured waveforms at turn-on of IGBT.

waveform reduces E_{LOSS} by 47% at the same $I_{OVERSHOOT}$ and $I_{OVERSHOOT}$ by 37% at the same E_{LOSS}. The latter measured waveforms are shown in Fig. 9. The similar results are obtained in the turn-off of IGBT. Fig. 10 shows the measured E_{LOSS} and $V_{OVERSHOOT}$ of the conventional single-step gate waveforms and the proposed automatically optimized gate waveforms at the turn-off of IGBT. The dotted concentric curves show the contour of $f_{OBJECT(OFF)}$ defined in Eq. (5). $E_{LOSS,\,MAX}$ and $E_{LOSS,}$

$_{MIN}$ in Eq. (1) and $V_{OVERSHOOT, MAX}$ and $V_{OVERSHOOT, MIN}$ in Eq. (3) are shown in Fig. 10. Compared with the conventional waveforms, the proposed waveform reduces E_{LOSS} by 55% at the same $V_{OVERSHOOT}$ and $V_{OVERSHOOT}$ by 53% at the same E_{LOSS}. The latter measured waveforms are shown in Fig. 11.

The programmable gate driver IC is also applied to a half-bridge inverter, where the gate driving waveform is changed depending on the load current [13]. Compared with the conventional single-step gate waveforms, the active gate control increases the efficiency of the half-bridge inverter at the same surge voltage [13].

The optimized parameters for the gate waveform depends on multiple conditions including the load current, the operating voltage, the temperature, and the variations of power devices. Therefore, the parameters should be optimally changed depending the operating conditions. How to change the parameters is the key point of the IoT- and AI-assisted Power Electronics 2.0. When the power device manufacturers and the power device users are not connected through the Internet, the first-step scenario will be to prepare multiple lookup tables before shipment and to change the parameters based on the tables depending on the measured sensor data. When the manufacturers and the users are always connected through the Internet, the second-step scenario will be that the manufacturers determine optimal parameters using AI based on the big data collected by IoT and transmit the parameters to the users through the Internet as shown in Fig. 1(b).

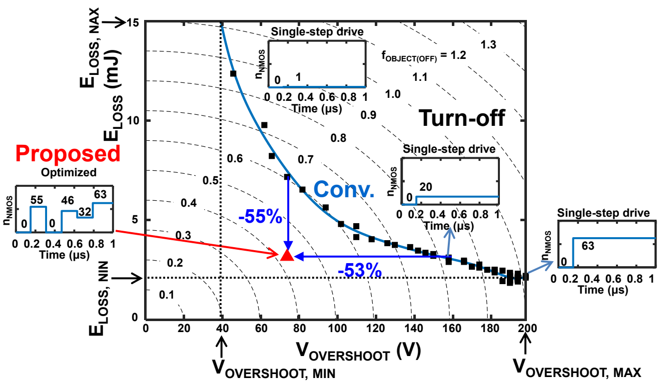

Fig. 10. Measured E_{LOSS} and $V_{OVERSHOOT}$ at turn-off of IGBT.

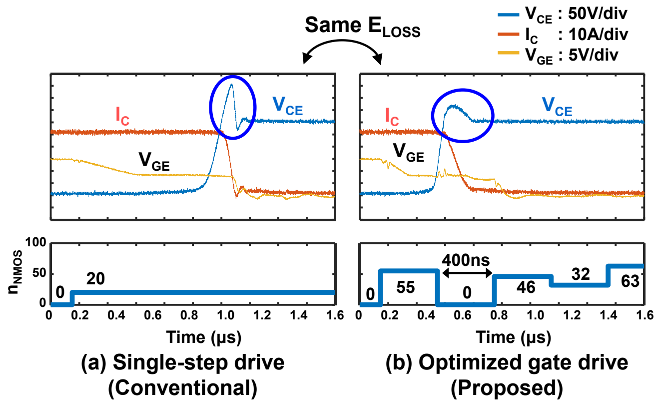

Fig. 11. Measured waveforms at turn-off of IGBT.

V. CONCLUSIONS

As the first step toward Power Electronics 2.0, the 6-bit programmable gate driver IC with automatic optimization of gate driving waveform for IGBT is presented. Compared with the conventional single-step gate waveforms, the proposed automatically optimized gate waveform reduces E_{LOSS} by 47% at the same $I_{OVERSHOOT}$ and $I_{OVERSHOOT}$ by 37% at the same E_{LOSS} at the turn-on of IGBT, and reduces E_{LOSS} by 55% at the same $V_{OVERSHOOT}$ and $V_{OVERSHOOT}$ by 53% at the same E_{LOSS} at the turn-off of IGBT.

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REFERENCES

[1] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," IEEE Trans. on Power Electronics, Vol. 29, No. 7, pp 3720-3732, Jul. 2014.

[2] M. Sasaki, H. Nishio, and W. T. Ng, "Dynamic gate resistance control for current balancing in parallel connected IGBTs," IEEE Applied Power Electronics Conf. and Expo., pp. 244-249, Mar. 2013.

[3] Y. Miki, M. Mukunori, T. Matsuyoshi, M. Tsukuda, and I. Omura, "High speed turn-on gate driving for 4.5kV IEGT without increase in PIN diode recovery current," IEEE Int. Symp. on Power Semiconductor Devices and ICs, pp. 347-350, May 2013.

[4] V. John, B. S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," IEEE Trans. on Industry Application, Vol. 35, No. 5, Sep. 1999.

[5] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," IEEE Trans. on Power Electronics, Vol. 30, No. 6, pp. 3402-3417, Jun. 2015.

[6] A. Shorten, W. T. Ng, M. Sasaki, T. Kawashima, and H. Nishio, "A segmented gate driver IC for the reduction of IGBT collector current over-shoot at turn-on," IEEE Int. Symp. on Power Semiconductor Devices and ICs, pp. 73-76, May 2013.

[7] A. Schindler, B. Koeppl, B. Wicht, and J. Groeger, "10ns variable current gate driver with control loop for optimized gate current timing and level control for in-transition slope shaping," IEEE Applied Power Electronics Conf and Expo., pp. 3570-3575, Mar. 2017.

[8] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, and T. Sakurai, "General-purpose clocked gate driver (CGD) IC with programmable 63-level drivability to reduce Ic overshoot and switching loss of various power transistors," IEEE Applied Power Electronics Conf and Expo., pp. 1640 -1645, Mar. 2016.

[9] H. Dymond, D. Liu, J. Wang, J. Dalton, N. McNeill, D. Pamunuwa, S. Hollis, and B. Stark, "Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns," IEEE Energy Conversion Congress & Exposition, pp. 1-6, Sep. 2016.

[10] J. Dalton, J. Wang, H. Dymond, D. Liu, D. Pamunuwa, B. Stark, N. McNeill, and S. Hollis, "Shaping switching waveforms in a 650 V GaN FET bridge-leg using 6.7 GHz active gate drivers," IEEE Applied Power Electronics Conf and Expo., pp. 1983-1989, Mar. 2017.

[11] T. Sakurai, B. Lin and A. R. Newton. "Fast simulated diffusion: an optimization algorithm for multi-minimum problems and its application to MOSFET model parameter extraction," IEEE Trans. on CAD, pp.228-234, Feb. 1992.

[12] K. Miyazaki, M. Takamiya, and T. Sakurai, "Automatic optimization of IGBT gate driving waveform using simulated annealing for programmable gate driver IC," IEEE Energy Conversion Congress & Exposition, pp. 1-6, Sep. 2016.

[13] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and switching loss," IEEE Applied Power Electronics Conf and Expo., pp. 1153-1159, Mar. 2017.