Buck Converter with Higher Than 87% Efficiency over 500nA to 20mA Load Current Range for IoT Sensor Nodes by Clocked Hysteresis Control

Chung-Shiang Wu, Makoto Takamiya and Takayasu Sakurai
The University of Tokyo, Tokyo, Japan
Email: cswu@iis.u-tokyo.ac.jp

***Abstract*—This paper presents a buck converter that achieves an almost flat conversion efficiency higher than 87% over the load current ranging from 500nA to 20mA. A leakage-based oscillator and a newly proposed double-half frequency control algorithm are introduced to provide a clock signal that triggers a hysteresis control, which is called Clocked Hysteresis Control (CHC). By removing continuously-on comparators in the conventional hysteresis control, the buck converter improves the conversion efficiency under light load current conditions while maintaining a fast transient response. The conversion efficiency of 87.7% at 1mA and 90.4% at 1μA are achieved. Compared with state-of-the-art buck converter, the efficiency at 1μA is improved 12% to 34%.**

I. INTRODUCTION

The growing development of Internet-of-Things (IoTs) pushes the increasing of wireless sensor nodes. Rather than mobile applications, the IoT sensor nodes may stay in a sleep mode for most of the time and quickly wakes up to work only in a short time. Several wireless communication specifications such as Bluetooth low energy (BLE) [1] have been proposed to support these applications. The sleep current indicated in BLE is about 1μA. However, for a wireless sensor node transmitting data in every 60 seconds, the sleep mode consumes much more energy than the active mode. Therefore, the conversion efficiency of a buck converter in a sleep mode becomes increasingly important to extend the battery lifetime.

The conversion efficiency of the previously announced buck converters, such as TPS62736 provided by Texas Instrument [2], drops steeply when the load current, I_{LOAD}, is less than 10μA. A tri-mode buck converter using PWM, PFM, and asynchronous mode proposed by [3] improves the conversion efficiency in the light current load condition, but it is still relatively low compared with the efficiency in the active mode. A buck converter with the conversion efficiency of 87% has been achieved at 1μA in [4], but it cannot supply mA range of the load current. Moreover, in order to realize a quick mode change including a wake-up, the hysteresis control is preferred. Nevertheless, the static current of continuously-on comparator strongly degrades conversion efficiency especially with a low load current. Even though [5] which is based on hysteresis control claims that the quiescent current is only 110nA, but it still limits the conversion efficiency to be 78% when I_{LOAD} is 1μA.

In this paper, a clocked hysteresis control scheme is proposed for a buck converter which inherits the quick response of a hysteresis control while removing the power consumed by continuously-on comparators. By replacing the continuously-on comparators in the conventional hysteresis control by clocked comparators, the buck converter consumes no static current in comparators. A leakage-based oscillator and a double-half control algorithm have also been proposed to track the appropriate system frequency. The target input voltage is 2.4V to 3.3V for high-reliability battery-powered system, and the output voltage is 1.5 to 1.6V for BLE. To indicate the advantage of removing continuously-on comparators, Fig. 1 shows the simulated controller power consumption distribution of the conventional hysteresis control. In order to clarify the power issue in the conventional hysteresis control, a simulation is carried out assuming I_{LOAD} is 1μA, the hysteresis window is 20mV with V_{IN} being 3V, V_{OUT} being 1.6V, and the bias current of the comparator being 1μA. The simulation result shows that 66% power consumption is occupied by the comparator, and the conversion efficiency is only 32%.

This paper is organized as follows: the system architecture is introduced in Section II. The double-half frequency control algorithm and the schematic of leakage-based oscillator are presented in Section III. Section IV shows the experimental results and the comparison with other buck converters. A conclusion is presented in Section V.

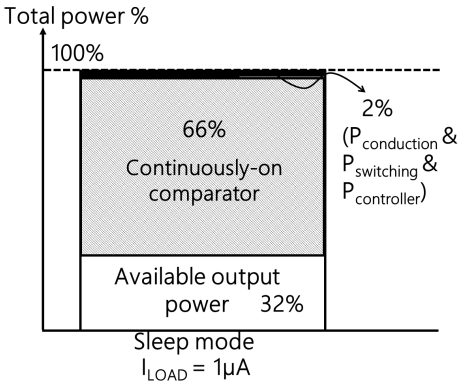

Fig. 1. Simulated power distribution of conventional hysteresis control employing continuously-on comparator.

II. SYSTEM ARCHITECTURE

The system block diagram and the control signal timing of the proposed buck converter are shown in Fig. 2 (a) and (b), respectively. There are 3 comparators, X_1, X_2, and X_3. X_1 and X_2 are employed to stabilize V_{OUT} within the hysteresis

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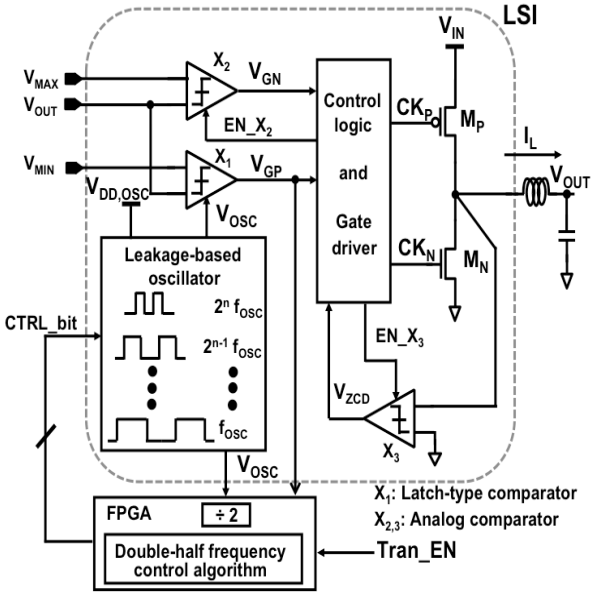
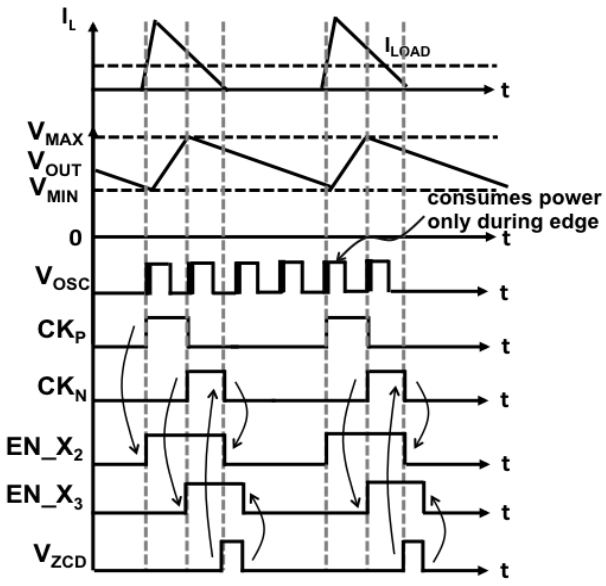
window forming by V_{MIN} and V_{MAX}. X_3 is designed for zero current detection (ZCD) to prevent inverse inductor current. X_1 is a latch-type comparator used to replace the continuously on comparator in the conventional hysteresis control. It consumes no static current and consumes power only at the clock edge. The clock signal V_{OSC} of X_1 is provided by the leakage-based oscillator, and the frequency f_{OSC} is controlled by the output signal, V_{GP}. f_{OSC} becomes double or half once the control signal bus CTRL_bit changes. On the other hand, X_2 and X_3 should operate fast to reduce the output voltage ripple and to prevent the reverse current. An analog comparator topology is chosen. These two comparators, however, are only turned on during designated time interval, as shown in Fig. 2(b), that is, these two comparators are also clocked and do not consume DC power. X_2 is only enabled when PMOS power transistor M_P is turned on, and it is turned off when the inductor current reaches zero. On the other hand, X_3 is only enabled when NMOS power transistor M_N is turned on, and turned off once it outputs a "1" signal. Thus, it is possible to remove normally-on DC current of comparators in the proposed clocked hysteresis control scheme. Moreover, the power consumption of the proposed system can be scaled with f_{OSC}, which is proportional to load current conditions. Therefore, the converter can achieve an almost-flat conversion efficiency over the wide load current range. An FPGA is employed to realize a sequencer which realizes the proposed double-half frequency control algorithm in the current implementation. The FPGA provides the CTRL_bit control signals outside according to V_{OSC} and V_{GP}, and adjusts the system frequency f_{OSC}. Only registers and look-up table (LUT) logic in the FPGA are used [6]. The number of gates used is 700 gates, which is estimated to consume 300pW in the technology used in the implementation for I_{LOAD} equal 500nA and V_{IN} equal to 3V. Consequently, the power consumption for the control logic itself is negligibly small. The algorithm of the double-half control will be described in the next section.



(a)



(b)

Fig. 2. (a) System block diagram of the proposed buck converter with leakage based oscillator and double-half frequency control algorithm. (b) Timing of relative control signals in the buck converter.

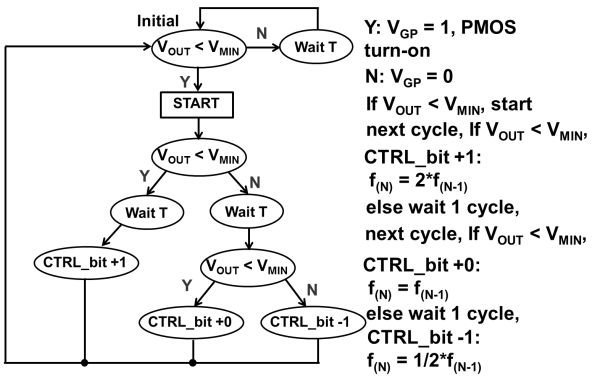


Fig. 3. Flowchart of the proposed double-half frequency control algorithm.

III. Double-Half Frequency Control Implemenation

The flowchart of the proposed double-half frequency control algorithm is shown in Fig. 3. The algorithm starts when V_{OUT} becomes lower than V_{MIN}. Once it starts, it will wait for another 1 clock cycle to monitor whether V_{OUT} is still lower than V_{MIN} or not. If V_{OUT} is still lower than V_{MIN}, meaning the comparator clock frequency is too slow. The control signal CTRL_bit will increase f_{OSC} to 2 f_{OSC}, and the sequencer logic restarts the above-mentioned process. On the other hand, if the next cycle V_{OUT} is higher than V_{MIN}, the sequencer will wait for another 1 cycle to judge that f_{OSC} should be double or half. This process operates continuously until an appropriate f_{OSC} is found that can make the buck converter operate stably. Some may argue that a buck converter with a hysteresis control in general may have an issue that the switching frequency is not fixed and that the harmonics of the switching frequency may interfere with the RF circuits on a chip. This situation can be eliminated by the proposed 'clocked' hysteresis control scheme by using

an external system clock as a base clock for the double-half control instead of the internal leakage-based oscillator output only in the active mode, although this function is not implemented in the current design.

Fig. 4 illustrates the schematic of the leakage-based oscillator. The oscillator should provide the double-half frequency controllability, and consume low power to prevent the conversion efficiency from degrading. Transistor leakage current is designed to bias the current source to achieve low current consumption and low frequency (~Hz) for μ-A I_{LOAD}. 8 NMOS transistors are connected in series to make diode-connected NMOS current mirror, it reduces the total number of NMOS transistors, which is dependent on the current mirror ratio. Moreover, the control bits are separated to control NMOS current mirror ratio and number of charging/discharging capacitors. The multiplier ratio of MSB NMOS transistor can be reduced to 2048. Low $V_{DD,OSC}$ is applied to achieve low power consumption. To fully turn on switches S_P and S_N to charge and discharge the capacitor, additional bootstrap circuit is also designed to boost V_{OSC} when output of the Schmitt trigger is switching.

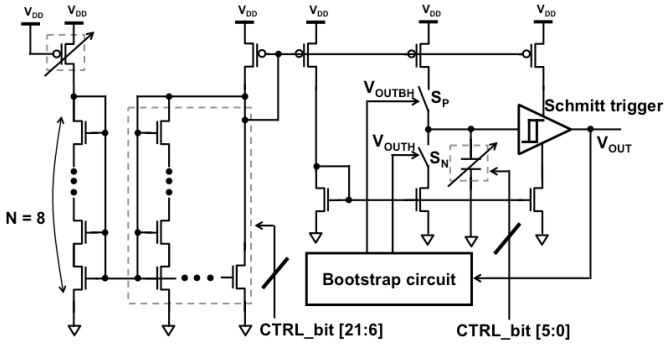


Fig. 4. Circuit schematic of the leakage-based oscillator.

IV. Experimental Results

The proposed buck converter with leakage-based oscillator is implemented in 0.18-μm standard CMOS technology. I/O transistors are used to implement circuits that should endure V_{IN} as high as 3.3V. The chip micrograph is shown in Fig. 5. The total chip size is 2.7mm^2 and the active area including the buck converter, leakage-based oscillator, and voltage level shifter is 0.71mm^2. The off-chip inductor and output capacitor are 4.7μH and 1μF, respectively. The hysteresis window, i.e. the voltage difference between V_{MAX} and V_{MIN}, is set to 20mV. The measured output waveforms under different load current condition are shown in Fig. 6(a) and (b). In Fig. 6(a), the 100-μA load current is applied, and V_{IN} is 3V. The frequency of V_{OSC} is 3.57KHz. The maximum output voltage ripple is less than 100mV, which is about 6% of output voltage. The transient response is measured with a system signal that resets f_{OSC} to the highest value before the load current changes. From Fig .6(c), it can be said that no large voltage drop is observed.

Fig. 7 illustrates the oscillating frequency and the power consumption of the proposed oscillator when $V_{DD,OSC}$ is 0.6V. 3 chips were measured, and the proposed leakage-based oscillator consumes only 3.5nW while the frequency is about 15Hz. The power consumption is less than 1% when I_{LOAD} is 500nA. As is discussed in Section II, the power consumption of the sequencer is negligible.

The measured dependences of the conversion efficiency on the load current are shown in Fig. 8. By removing continuously-on comparators and applying the leakage-based oscillator with the double-half frequency control algorithm, the converter can achieve the almost-flat conversion efficiency and 90.4% when I_{LOAD} is 1μA. The conversion efficiency is higher than 87% all over the range from 500nA to 20mA. The performance comparison with state-of-the-art buck converter for BLE is shown in Table I.

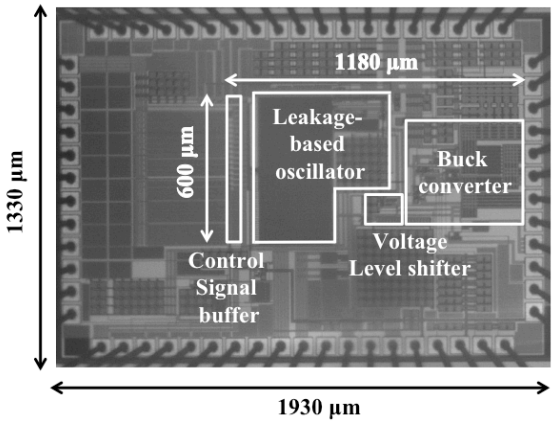
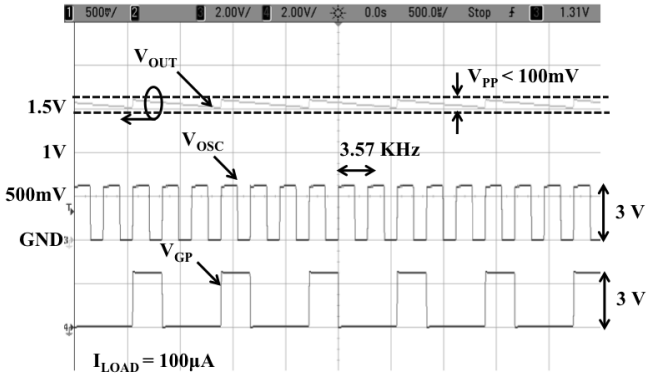
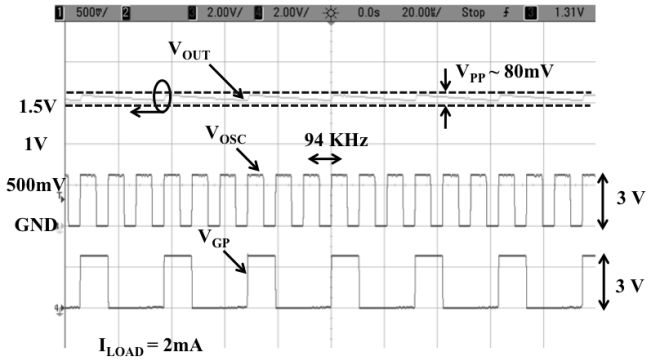


Fig. 5. Chip microphotograph.



(a)



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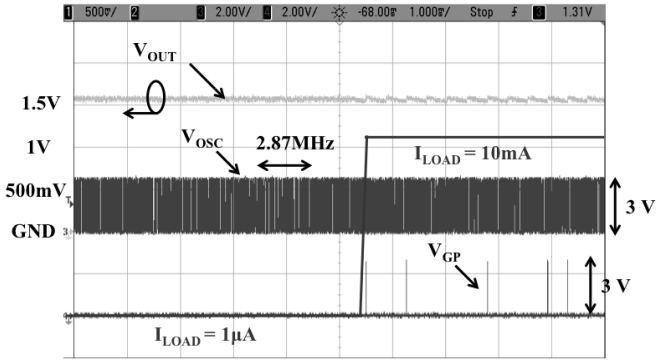

(c)

Fig. 6. Measured waveforms of V_{OUT}, V_{OSC}, and comparator X_1 output V_{GP}. (a) V_{IN} = 3 V, V_{OUT} = 1.58 V, and I_{LOAD} = 100 µA. (b) V_{IN} = 3 V, V_{OUT} = 1.58 V, and I_{LOAD} = 2 mA. (c) Output transient response when I_{LOAD} changes from 1 µA to 10mA.

V. CONCLUSION

A buck converter with a leakage-based oscillator and the double-half frequency control algorithm is developed to remove the static current in the comparators employed in the conventional hysteresis buck converter. The proposed approach improves the conversion efficiency when I_{LOAD} is lower than 1µ A and achieves an almost-flat efficiency of higher than 87% over the range from 500nA to 20mA load current by a uniform control and circuit scheme. In addition, the buck converter maintains a fast transient response of the conventional hysteresis control, making it suitable for IoT sensor node applications.

Table 1. Summary of performance comparison

	ISSCC'15 [3]	VLSI'15 [4]	CICC'15 [5]	VLSI'11 [7]	**This work**
Technology	180nm CMOS	180nm CMOS	350nm CMOS	250nm CMOS	**180nm CMOS**
Die size	1.44mm^2	2.42mm^2	2.88mm^2	0.21mm^2	**0.71mm^2***
V_{IN} (V)	0.6/1.2	3	2.2 – 6	1.2 – 2.5	**2.4 – 3.3**
V_{OUT} (V)	0.35 – 0.5	1	2.5	1	**1.5 – 1.6**
I_{LOAD}	100nA – 20mA	10nA – 1µA	1µA – 100mA	1µA – 100mA	**500nA – 10mA**
Peak eff. η_{PEAK}	92%	87%	95%	95.2	**90.4%**
η @ I_{LOAD}=1µA	75%	87%	78%	65%	**90.4%**
Inductor value L	4.7µH	47µH	2.2µH	1.5µH	**4.7µH**
Control Methodology	PWM, PFM, and AM	Constant on-time	Hysteresis control	Dynamic on/off time	**Clocked hysteresis control**

* Active area

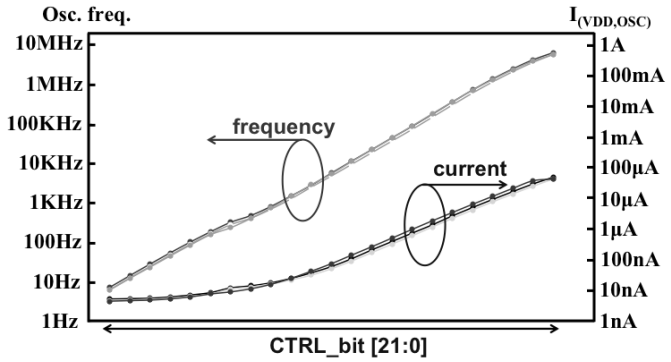

Fig. 7. Measured oscillating frequency and power consumption of the leakage based oscillator.

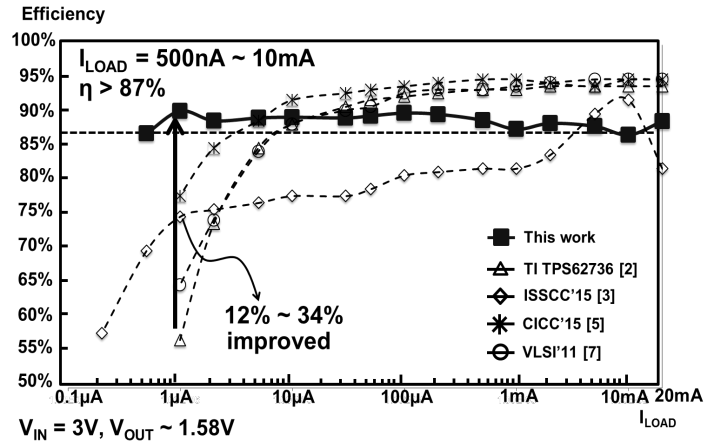

Fig. 8. Measured conversion efficiency of the proposed buck converter and the comparison with state-of-the-art.

REFERENCES

[1] Bluetooth Low Energy (BLE), https://www.bluetooth.com.

[2] Texas Instruments, "Programmable output voltage ultra-low power buck converter with up to 50mA/200mA output current," Texas Instruments, Dallas, TX, USA, TPS62736 Datasheet, Mar. 2013.

[3] P.-H. Chen, C.-S. Wu, and K.-C. Lin, "A 50nW-to-10mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting, " *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 376-378, Feb. 2015.

[4] D. El-Damak, and A. P. Chandrakasan, "Solar Energy Harvesting System with Integrated Battery Management and Startup using Single Inductor and 3.2nW Quiescent Power," *IEEE Symposium on VLSI Circuits*, pp. 280-281, June 2015.

[5] D. Lu, S. Yao, and B. Shao, "A 110nA Quiescent Current Buck Converter with Zero-Power Supply Monitor and Near-Constant Output Ripple, " *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Sep. 2015.

[6] National Instruments, "FPGA Fundamentals", www.ni.com/white-paper/6983/en/#.

[7] C.-Y. Hsieh, Y.-Huei Lee, Y.-Y Yang, T.-C. Huang, K.-H Chen, C.-C. Huang, and Y.-H. Lin, "A Battery-free 225nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control," *IEEE Symposium on VLSI Circuits*, pp. 242-243, June 2011.