P.2.3. Spike Noise Cancelling Circuit for Switched Capacitor DC-DC Converter Mounting MLCCs on CMOS die

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Abstract

In the previous work [1], the switched capacitor (SC) DC-DC converter mounting four 100-nF 0402 (0.4mm x 0.2mm x 0.2mm) multilayer ceramic chip capacitors (MLCCs) on 180-nm CMOS die was presented for integrated voltage regulators and achieved the efficiency of 92.9% at the output power density of 62mW/mm^2. When the SC DC-DC converter is scaled down from 180-nm CMOS to 65-nm CMOS with the same MLCCs, the increase of the spike noise caused by the parasitic inductance of MLCCs is observed due to the increasing di/dt of power transistors. To solve the problem, a new spike noise cancelling circuit, where each power transistor is divided into two transistors with large and small gate width in parallel and the switching timing of the small transistor is delayed than the large transistor, is proposed. A 2-V input 1/2 SC DC-DC converter including the proposed spike noise cancelling circuit mounting three 100-nF 0402 MLCCs on 65-nm CMOS die is fabricated. The measurement results show that the spike noise is reduced from 103mV to less than 10mV thanks to the proposed spike noise cancelling circuit.

Brief Description and Figures

Fig. 1 shows the circuit schematic of the 1/2 SC DC-DC converter and the definition of the spike noise voltage (V_{SPIKE}). In our initial design, a large V_{SPIKE} caused by the parasitic inductance (170pH) of MLCC was observed as shown in Fig. 5 (a). The target of this work is to reduce the large V_{SPIKE}. Fig. 2 shows the implementation of SW_3 in Fig. 1 and the similar applies to SW_1, SW_2, and SW_4. Fig. 2 (a) shows the initial design. Figs. 2 (b) and (c) show the conventional [2] and the proposed design to reduce V_{SPIKE}, respectively. In the proposed spike noise cancelling circuit, a power transistor is divided into two transistors with large and small gate width in parallel and the switching timing of the small transistor is delayed than the large transistor. Fig. 3 show the SPICE-simulated efficiency vs. V_{SPIKE} of the different SC DC-DC converters in Fig. 2. In the conventional design, where C_{SMALL} is varied from 0pF to 7pF with 1-pF step, the trade-off between the efficiency and V_{SPIKE} is observed, that is, when C_{SMALL} is increased to reduce V_{SPIKE}, the efficiency is degraded. To solve the trade-off, the spike noise cancelling circuit achieving both the high efficiency and low V_{SPIKE} is proposed. Fig. 4 shows the fabricated 2-V input 1/2 SC DC-DC converter mounting three 100-nF 0402 MLCCs on 65-nm CMOS die. Figs. 5 (a) and (b) show the measured waveforms of V_{OUT} and the 20-MHz clock signal of the 2-V input 1/2 SC DC-DC converters with the initial design (Fig. 2 (a)) and the proposed design (Fig. 2 (c)), respectively. The output current is 300mA. V_{OUT} is obtained via a source follower. The proposed spike noise cancelling circuit reduces the spike noise from 103mV (Fig. 5 (a)) to less than 10mV (Fig. 5 (b)).

Key Contributions

The proposed spike noise cancelling circuit reduces the spike noise from 103mV to less than 10mV in the measurement of the 2-V input 1/2 SC DC-DC converter in 65-nm CMOS.

References

[1] T. Sai, Y. Yamauchi, H. Kando, T. Funaki, T. Sakurai, and M. Takamiya, "2/3 and 1/2 Reconfigurable Switched Capacitor DC-DC Converter with 92.9% Efficiency at 62mW/mm² Using Driver Amplitude Doubler," IEEE Transactions on Circuits and Systems II: Express Briefs (Early Access).
[2] J. Liu, et al., "Slew-Rate Controlled Output Stages for Switching DC-DC Converters," IEEE, ICICDT, pp. 1-4, 2011.

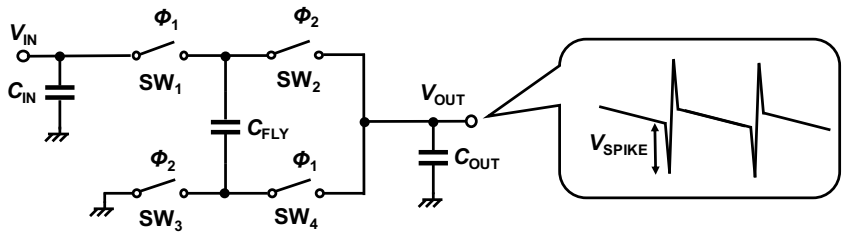


Fig.1 Circuit schematic of 1/2 SC DC-DC converter and definition of spike noise voltage (V_{SPIKE}).

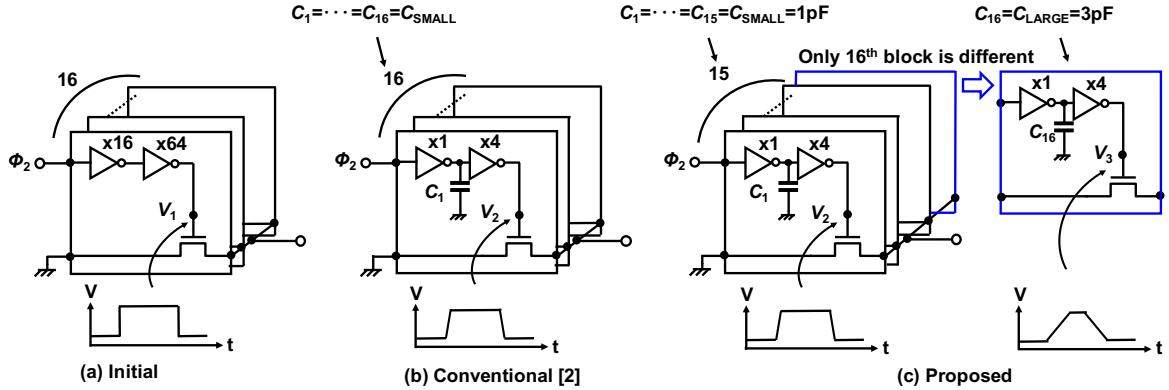


Fig.2 Implementation of SW_3 in Fig. 1. (a) Initial and (b) conventional design [2]. (3) Proposed spike noise cancelling circuit.

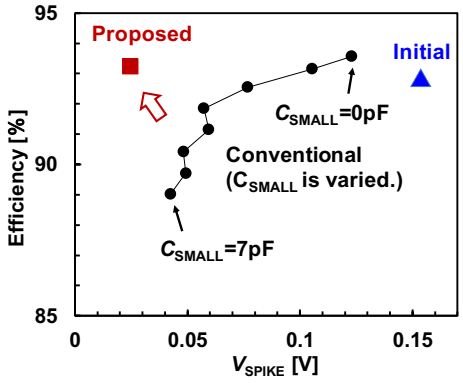


Fig.3 Simulated efficiency vs. V_{SPIKE} of different SC DC-DC converters in Fig. 2.

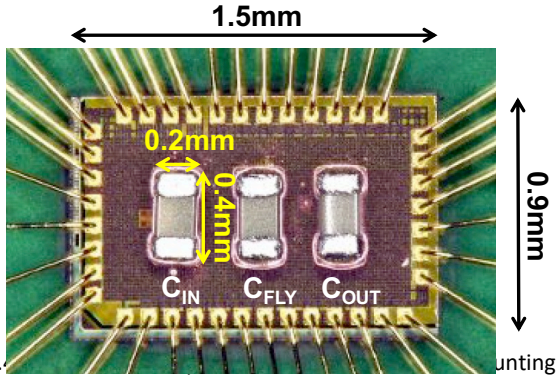
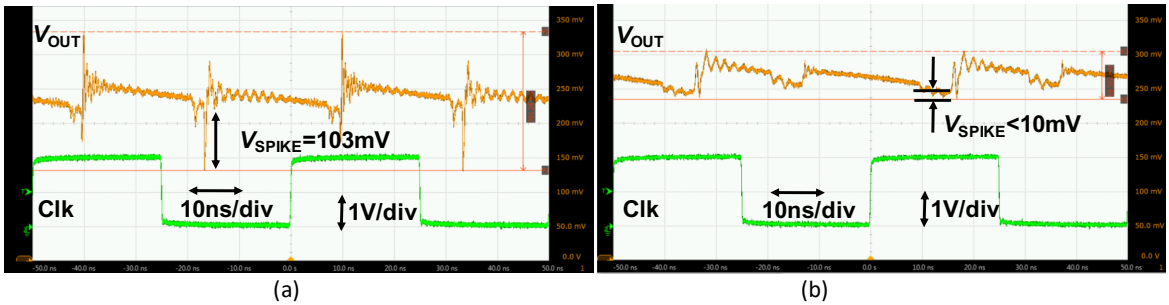


Fig. … unting three 100-nF 0402 MLCCs on 65-nm CMOS



(a) (b)

Fig.5 Measured waveforms of SC DC-DC converter with initial design (Fig. 2 (a)) and proposed design (Fig. 2 (c)).