Clocked Hysteresis Control Scheme With Power-Law Frequency Scaling in Buck Converter to Improve Light-Load Efficiency for IoT Sensor Nodes

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Abstract— A clocked hysteresis control scheme with power-law frequency scaling is proposed to improve the conversion efficiency at a light load current, and it is applied to a buck converter design. By replacing a continuously on comparator used in conventional hysteresis control by a clocked comparator with power-law frequency scaling, the buck converter consumes no direct current (dc) in the comparators. Almost flat efficiency over a load current ranging from 500 nA to 20 mA is achieved. In addition, a quick wakeup feature is maintained because of the inherent hysteresis control. As for the theoretical aspect, expressions for the frequency stability condition, power consumption, and output voltage ripple of the proposed power-law frequency scaling scheme are derived and analyzed. A leakage-based digitally controlled oscillator, which consumes only 3.5 nW when the frequency is 15 Hz for 500-nA load current, is designed to provide a clock signal to the clocked comparator. Experimental results show that the buck converter implemented with the power-law frequency scaling scheme achieves a 90.4% peak efficiency and higher than 87% efficiency over a load current range from 500 nA to 20 mA.

Index Terms— Clocked hysteresis control (CHC), discontinuous conduction mode (DCM) buck converter, hysteresis control, power-law frequency scaling, wide-load-range buck converter.

I. INTRODUCTION

WITH the rapid growth of Internet-of-Things (IoTs) applications, demand for the development of wireless sensor nodes is increasing. Many applications such as smart cities/buildings, healthcare, and even those in industrial fields require sensors operating for a long time without the need to replace the battery. A direct current to direct current (dc–dc) converter used in IoT sensor nodes to convert the battery input voltage to a well-regulated output voltage for large-scale integrated (LSI) circuits should provide a high conversion efficiency to prolong the battery lifetime. Unlike mobile applications, the wireless sensors employed in IoT applications stay in a sleep mode for most of the time and quickly wake up to transmit data for only a short period of time. It has been shown by calculation [1] that the energy consumption of the sleep mode is 10 times that of the active mode when the sleep current is 1 μA, as specified in the Bluetooth low energy (BLE) specifications [2]. Therefore, the conversion efficiency in the sleep mode is becoming increasingly important to reduce overall energy consumption.

Thus far, several commercial products and publications on buck converters for IoT sensor node applications have been reported. The conversion efficiency, however, degrades rapidly when the load current decreases to microampere order [3]. A tri-mode buck converter consisting of a digital pulsewidth modulation, a pulse-frequency modulation (PFM), and an asynchronized mode (AM) [4] improves the conversion efficiency and extends the possible load range to 100 nA. The conversion efficiency, however, is still lower than 80% when the converter operates in the AM for a 1-μA load. An adaptive application of bias current for analog circuits depending on the loading conditions [5] improves the conversion efficiency when the load current is low. The quiescent current in [5] was as low as 110 nA with low output voltage ripple performance. The conversion efficiency, however, was still limited to 78% when the load current was 1 μA. In contrast, the buck converter proposed in [6] achieved 87% conversion efficiency at 1 μA, but it did not supply sufficient load current in an active mode and did not support a fast wakeup operation required for IoT applications.

For IoT applications, because of the low load current in a sleep mode and a limited area for an inductor, the buck converter operating in a discontinuous conduction mode (DCM) is required. There are two basic control schemes for a buck converter operating in the DCM: constant-on-time (COT) control and hysteresis control. These two schemes are shown in Fig. 1(a) and (b), respectively. In COT control [7], a high-speed comparator is employed to compare the output voltage with a reference voltage V_{REF}. A pulse signal with a fixed pulsewidth is applied to the power stage triggered by the comparator output signal. The output voltage is regulated as $V_{\text{OUT}} = V_{\text{REF}}$, and the voltage error between V_{REF} and V_{OUT} is monitored continuously. On the other hand, hysteresis control uses hysteresis comparators to regulate the output voltage within a designed hysteresis voltage window. In addition, hysteresis control inherently provides a high
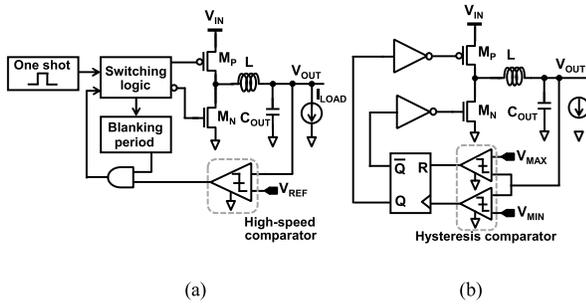
Fig. 1.   Conventional control schemes for buck converter operating in DCM. (a) COT control. (b) Hysteresis control.

output voltage response speed when I_{LOAD} changes [8]. This is preferable, especially in IoT applications when a quick wake-up operation is required to conserve the energy of a system. Both schemes, however, consume dc current because they require continuously on comparators to monitor the output voltage. A typical circuit schematic of the continuously on comparator in Fig. 1(a) and (b) is shown in Fig. 2(a) [9], [10]. To clarify the power distribution of the typical hysteresis buck converter shown in Fig. 1(b), a simulation assuming that V_{IN} is 3 V and V_{OUT} is 1.6 V with a 20-mV hysteresis voltage window and 1-μA bias current is conducted. Fig. 3(a) shows the power distribution in a sensor node in an active mode when I_{LOAD} is 10 mA. In a sleep mode where I_{LOAD} is 1 μA, as specified by BLE, the power consumption of the continuously on comparator accounts for 63% of the total power consumption, limiting the conversion efficiency is only 34%, as shown in Fig. 3(b), even though the power consumption of the reference voltage can be reduced to 10-nA order [11].

To improve the conversion efficiency in the sleep mode, a clocked hysteresis control (CHC) buck converter with a power-law frequency scaling scheme is proposed in this paper. Replacing the continuously on comparator used in conventional hysteresis control by a clocked comparator, as shown in Fig. 2(b) [12], the buck converter consumes no dc current in the comparators. The proposed power-law frequency scaling scheme dynamically adjusts the clock frequency for the clocked comparator depending on the load current to stabilize the output voltage. As a result, the comparator power consumption becomes proportional to the load current. The buck converter can achieve almost flat conversion efficiency over the whole load current range specified by BLE while inheriting a quick wakeup response of hysteresis control. This paper is organized as follows. Section II describes the system architecture of the proposed CHC buck converter employing a power-law frequency scaling scheme operating in DCM. The power-law frequency scaling scheme, including the frequency stability, the output voltage ripple, and the effect of the load fluctuation, is analyzed in Section III. Circuit implementations are illustrated in Section IV. Experimental results are shown in Section V. Finally, conclusion is presented in Section VI.

II. SYSTEM ARCHITECTURE

A system block diagram of the proposed CHC buck converter is shown in Fig. 4. The target input voltage ranges
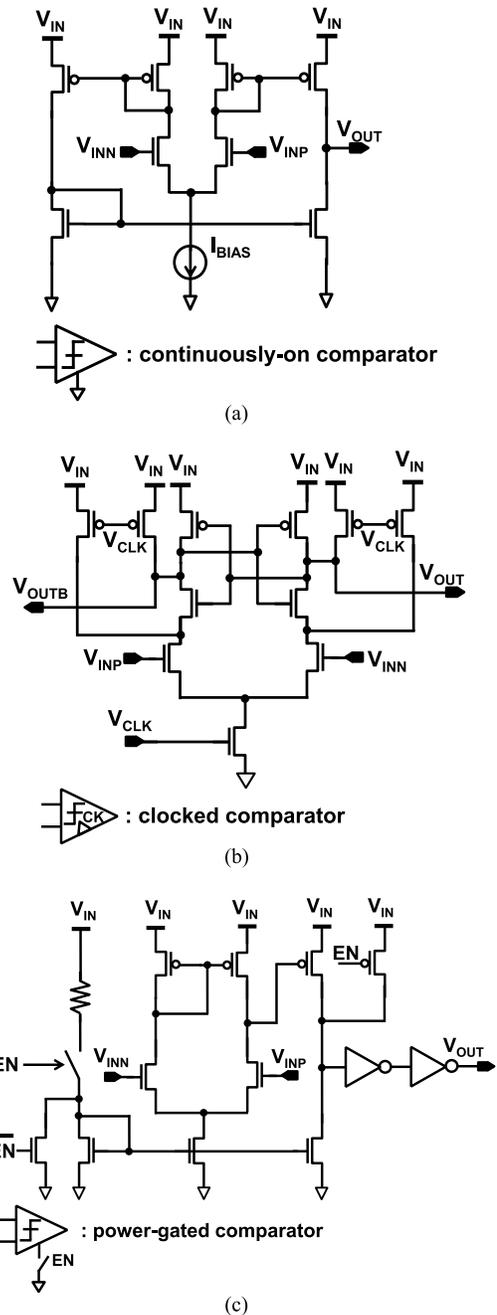
Fig. 2.   Circuit schematic and symbol of comparator. (a) Continuously on comparator. (b) Clocked comparator. (c) Power-gated comparator. (This topology is used in Fig. 4.)

from 2.4 to 3.3 V, allowing it to be a battery-based system. The output voltage is set to be 1.5–1.6 V to power LSI circuits in sensor nodes with BLE communication. For typical sensor node applications, the buck converter operates in DCM because of the low load current while using an inductor with small inductance. Compared with the conventional hysteresis buck converter, the continuously on comparator is replaced by a clocked comparator X_1. Comparators X_2 and X_3 are power-gated comparators whose circuit schematic and symbol are shown in Fig. 2(c). We note that for X_3, a topology consisting of a pMOS input differential pair with an nMOS active load is
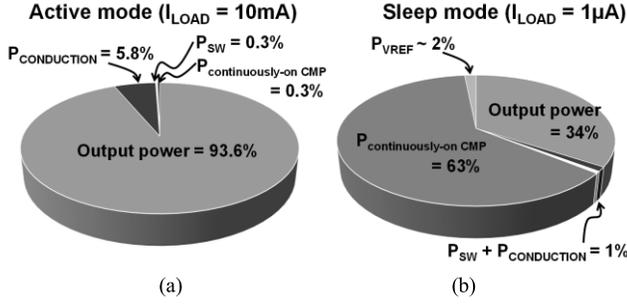
Fig. 3. Simulated power dissipation of typical hysteresis buck converter in active and sleep modes. (a) Active mode. (b) Sleep mode. $P_{\text{CONDUCTION}}$ and P_{SW} denote the conduction and switching losses of the converter, respectively. P_{VREF} denotes the power consumption of a reference voltage generator V_{REF}.

Fig. 5. (a) Operating timing diagram and relative control signals in CHC buck converter. (b) Load wakeup operation.

Fig. 4. System block diagram of the proposed CHC buck converter with power-law frequency scaling scheme.

applied because X_3 compares V_X with ground. Using an enable signal, X_2 and X_3 are turned ON in a short period of time in every switching cycle. The bias points of the current mirror and the output are reset to ground and logic "1," respectively, by the enable signal EN. Therefore, no dc current is consumed when the comparators are disabled. X_1 and X_2 are designed to regulate V_{OUT} within a hysteresis voltage window specified by voltage references V_{MAX} and V_{MIN}. The dependence of the output voltage ripple on the hysteresis voltage window will be discussed in Section III. In addition, comparator X_3 is used for zero-current detection (ZCD), preventing reverse inductor current loss. X_3 compares V_X with ground and generates a signal to turn OFF the nMOS power transistor M_N when the inductor current reaches zero. An analog-type comparator is necessary because X_2 and X_3 should operate sufficiently quickly to reduce the output voltage ripple and to prevent reverse inductor current, respectively. Since there is no need for X_2 and X_3 to be turned ON all the time, they are activated for a short time when the enable signal for each comparator is ON.

A leakage-based digitally controlled oscillator (DCO) is implemented to provide a clock signal V_{CLK} to X_1. The frequency of V_{CLK}, f_{CLK}, can be adjusted from $2^0 f_{\text{CLK,MIN}}$ to $2^{21} f_{\text{CLK,MIN}}$ by 22-bit clock frequency control signals named $F_{\text{CLK\_CTRL}}$ [21:0], where $f_{\text{CLK,MIN}}$ denotes the lowest clock frequency. $F_{\text{CLK\_CTRL}}$ [21:0] are provided by a

field-programmable gate array (FPGA) for an experiment but can easily be implemented on a chip. The power-law frequency scaling scheme is implemented by the FPGA. V_{CLK} and the output signal of X_1, $V_{\text{OUT\_LOW}}$, are applied to the FPGA to generate $F_{\text{CLK\_CTRL}}$. If f_{CLK} is too slow considering the load condition, $F_{\text{CLK\_CTRL}}$ is increased by 1 bit, making f_{CLK} double. On the other hand, if f_{CLK} is too fast for the load condition, $F_{\text{CLK\_CTRL}}$ is decreased by 1 bit, making f_{CLK} a half. The exact meanings of "too slow" and "too fast" are described later. Therefore, f_{CLK} is controlled in accordance with the load conditions. Only basic logic elements are used on the FPGA. By a simple calculation [13], the employed gate count on the FPGA is about 700 gates, which consume less than 1 nW when I_{LOAD} is 500 nA, f_{CLK} is 15 Hz, and V_{IN} is 3 V, which is negligible compared with the power loss in a sleep mode.

Fig. 5(a) shows the operating timing diagram of the proposed CHC buck converter. When V_{OUT} becomes lower than V_{MIN}, which is detected by X_1, $V_{\text{OUT\_LOW}}$ is logic "1" and pMOS power transistor M_P is turned ON, which conducts an inductor current and charges up the output voltage. At the same time, comparator X_2 is enabled and starts comparing V_{OUT} with V_{MAX}. Once V_{OUT} reaches V_{MAX}, M_P is turned OFF and nMOS power transistor M_N is turned ON. The turn-ON signal for M_N is also used to disable X_2 and enable X_3. M_N is turned OFF when the inductor current reaches zero, which is detected by the ZCD comparator X_3. X_3 is disabled automatically when M_N is turned OFF. X_2 and X_3 are turned ON during $T_{\text{ON,X2}}$ and $T_{\text{ON,X3}}$, respectively, in every power stage switching period T_{SW}. Therefore, applying the proposed control scheme, comparators X_1, X_2, and X_3 are all "clocked" and consume no dc power.

The conduction and switching losses in the buck converter are estimated as follows:

$$P_{\text{conduction}} = I_{L,\text{RMS}}^2 \cdot (R_{\text{DS,ON}} + R_{\text{ESR}}) \qquad (1)$$

$$P_{\text{switching}} = \alpha \cdot f_{\text{SW}} \cdot C_{\text{TOTAL}} \cdot V_{\text{IN}}^2 \qquad (2)$$

where $I_{L,\text{RMS}}$ is the root mean square of the inductor current, $R_{\text{DS,ON}}$ is the ON resistance of power transistors M_P and M_N, R_{ESR} is the equivalent series resistance of the inductor, f_{SW} is the switching frequency of the power stage, V_{IN} is the

input voltage, C_{TOTAL} is the total capacitance at the gates of M_P and M_N, and α is the average activity factor. In addition, the power consumption of X_2 and X_3 can also be estimated as

$$P_{\text{comp.,X2,3}} = \frac{1}{T_{\text{SW}}} \int_0^{T_{\text{ON,X2,3}}} V_{\text{IN}} \, I(t) \, dt \qquad (3)$$

where $1/T_{\text{SW}}$ is the switching frequency of the power stage f_{SW}, $T_{\text{ON,X2}}$, and $T_{\text{ON,X3}}$ are the turn-ON time of comparators X_2 and X_3, respectively, and $I(t)$ is the current consumed by the comparator. As indicated in (1)–(3), by adopting PFM in DCM operation, the conduction loss, switching loss, and power consumption of X_2 and X_3 can be scaled with I_{LOAD} because all of them are proportional to f_{SW}. The power consumption of clocked comparator X_1, however, is proportional to the clock frequency f_{CLK}. An appropriate clock frequency is required to regulate the output voltage while keeping the power consumption of X_1 low. Using a higher clock frequency results in higher power consumption of X_1 and the controller circuits, thus losing the benefit of using the clocked comparator. On the other hand, applying a lower clock frequency induces a large voltage ripple at V_{OUT}. A power-law frequency scaling scheme is proposed to adjust the clock frequency f_{CLK} in the CHC buck converter, making f_{CLK} also proportional to I_{LOAD}. Therefore, the conduction loss and switching loss of the power stage, and the controller power consumption including the comparators are all scaled with I_{LOAD}. Thus, the CHC buck converter can achieve almost flat conversion efficiency over a wide range of loads including a sleep mode.

For IoT sensor node applications, the buck converter must support quick wakeup operation when the system operation changes from a sleep mode to an active mode. The wakeup operation of the CHC buck converter is illustrated in Fig. 5(b). The load current as the wakeup threshold can be set depending on applications for power and output voltage drop optimization. When the system is woken up, an external wakeup signal WAKE_UP synchronized with a change in I_{LOAD} is applied to the FPGA or a controller on the chip if the logic is implemented on a chip. The current frequency control bits, $F_{\text{CLK\_CTRL}}$ [21:0], are reset by WAKE_UP, making f_{CLK} changes from the current frequency f_1 to the highest frequency $f_{\text{CLK,MAX}}$, that is, $2^{21} f_{\text{CLK,MIN}}$. With the proposed frequency scaling scheme, the clock frequency f_{CLK} gets half and half step by step, and automatically settles to a new value f_2 according to the loading condition. Therefore, the buck converter can achieve fast wakeup operation.

III. POWER-LAW FREQUENCY SCALING SCHEME

A flowchart of the proposed frequency scaling scheme is shown in Fig. 6. At the start of the control, the clock frequency f_{CLK} is set to the highest value, $2^{21} f_{\text{CLK,MIN}}$, and the V_{OUT} checking counter implemented on the FPGA is reset to 0. If $V_{\text{OUT}} > V_{\text{MIN}}$ at the clock edge, meaning that $V_{\text{OUT\_LOW}}$ is logic "0," the counting number n increases by 1, and the process restarts. On the other hand, if $V_{\text{OUT}} < V_{\text{MIN}}$ at the clock edge, $V_{\text{OUT\_LOW}}$ is logic "1," making the buck converter starts a new switching cycle. At the same time, the counter number
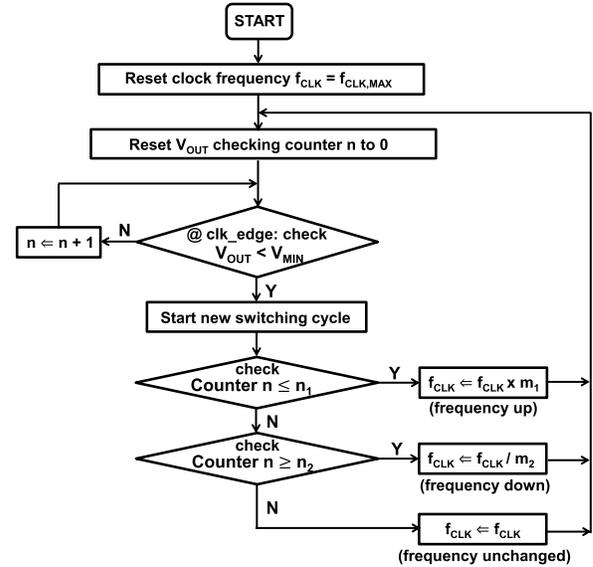
Fig. 6. Frequency control flowchart of the proposed frequency scaling scheme.

TABLE I
FREQUENCY SCALING OF f_{CLK} AND DEPENDENCE OF f_{CLK} ON I_{LOAD} EXPRESSED USING n, n_1, AND n_2

V_{OUT} checking counter n @$V_{\text{OUT}} < V_{\text{MIN}}$	Current f_{CLK} @ I_{LOAD}	Frequency multiply/divide
$n \leq n_1$	Too low	$\times m_1$
$n_2 > n > n_1$	Appropriate	unchanged
$n \geq n_2$	Too high	$\div m_2$

n is read out and compared with two preset boundaries, n_1 and n_2, where $n_2 > n_1$. $n \leq n_1$ indicates that the output voltage V_{OUT} crosses V_{MIN} earlier than expected, that is, I_{LOAD} is high but the clock frequency f_{CLK} is too low. M_P should be turned ON frequently to transfer energy from V_{IN} to V_{OUT}. Therefore, f_{CLK} is multiplied by m_1 and the algorithm restarts. $n > n_1$ and $n > n_2$ mean that f_{CLK} is too high. Clocked comparator X_1 checks V_{OUT} several times and turns ON M_P only once. In this case, f_{CLK} is divided by m_2. This process operates continuously, and the V_{OUT} checking counter number n settles to a value larger than n_1 and smaller than n_2, i.e., $n_2 > n > n_1$. In the steady state, an appropriate f_{CLK} is found by the proposed power-law frequency scaling scheme that can stabilize the output voltage of the buck converter, and f_{CLK} is a multiple of the switching frequency f_{SW}. Therefore, the power consumption of X_1 is also proportional to I_{LOAD} because f_{CLK} is proportional to f_{SW}. These three conditions of n including the frequency scaling and the relation between f_{CLK} and I_{LOAD} are summarized in Table I. An example of implementation showing the output waveform, the clock signal, $V_{\text{OUT\_LOW}}$, and the V_{OUT} checking counter n in the time domain when $m_1 = m_2 = 2$, $n_1 = 2$, and $n_2 = 5$ is illustrated in Fig. 7. In Fig. 7(a), V_{OUT} is lower than V_{MIN} when $n = 2 \leq n_1$ in the first switching period. This is the case when the initial f_{CLK} is too low possibly generating a larger output voltage ripple. Thus, f_{CLK} is doubled ($\times m_1$). On the
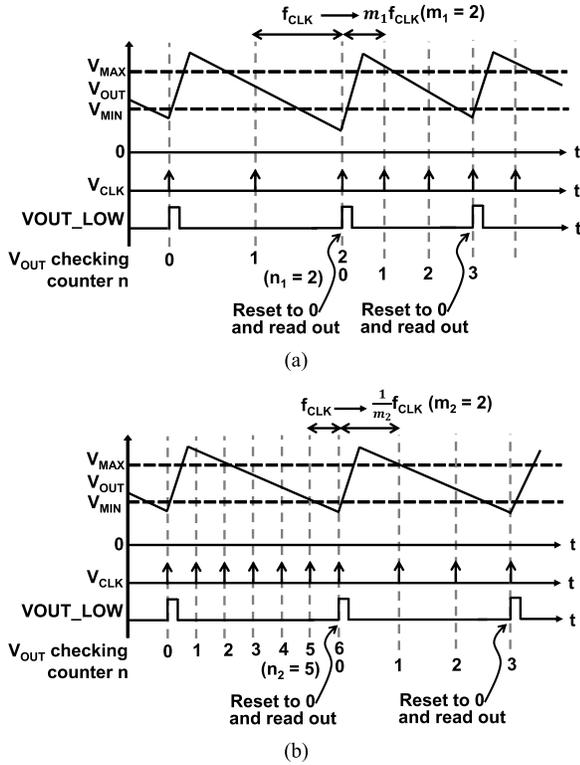
Fig. 7. (a) When the initial f_{CLK} is too low, f_{CLK} is doubled. (b) When the initial f_{CLK} is too high, f_{CLK} is halved.

other hand, when the initial f_{CLK} is too high, V_{OUT} is lower than V_{MIN} when $n > n_2$, resulting in the consumption of more power than appropriate, which is the case shown in Fig. 7(b). f_{CLK} becomes halved ($\div m_2$) to reduce the power consumption of the comparator. In Sections III-A–III-C, the design parameters that make the CHC buck converter works properly are determined. Then, the frequency stability, the output voltage ripple, and the effect of the load current fluctuation on V_{OUT} are derived theoretically.

A. Frequency Multiply/Divide Ratio Decision

Parameters m_1, m_2, n_1, and n_2 illustrated in Fig. 6 should be determined to make the frequency scaling scheme operates properly. As indicated by Fig. 6, f_{CLK} can be expressed as

$$f_{CLK} = \frac{m_1^q}{m_2^p} f_{CLK,MIN} \tag{4}$$

$$m_1 = m_2^\gamma \tag{5}$$

where p and q denote the corresponding decision cycles and m_1, m_2, p, and q are natural numbers. Considering that the frequency scaling scheme may induce harmonics that interfere with other sensitive circuits such as RF blocks on the same chip, the relation between m_1 and m_2 is expressed as (5), where γ is designed as a natural number, that is, larger than or equal to 1. Therefore, the harmonics generated by the frequency scaling scheme are located at integral multiples of $f_{CLK,MIN}$ in the frequency spectrum. Replacing m_1 in (4) by (5), f_{CLK} can be expressed as

$$f_{CLK} = m_2^N f_{CLK,MIN}, \quad N = \gamma q - p \tag{6}$$
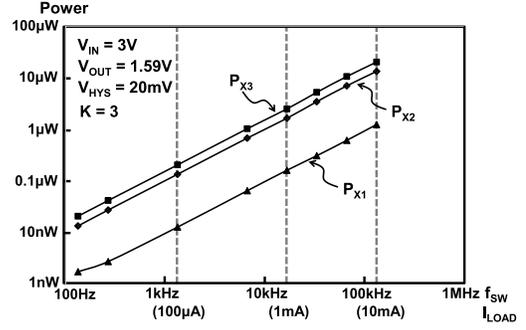
Fig. 8. Simulated dependence of power consumption of comparators (X_1, X_2, and X_3) on f_{SW} and I_{LOAD}.

where N is also a natural number. As indicated by (5), any natural numbers m_1, m_2, and γ can be chosen for the power-law frequency scaling scheme. A higher m_1 results in a high tracking speed for the I_{LOAD} wakeup operation, but dissipates more power in every frequency transition. On the other hand, a higher m_2 can reduce power consumption during the transient. However, according to the analysis in Section III-C, a higher value of m_2 rapidly reduces the clock frequency, which induces a large output voltage drop and an unacceptable output voltage ripple. Therefore, except 1, the minimum value of a natural number, 2, is chosen for m_2, resulting in frequency scaling of 2^N. Depending on the application, m_1 can be designed to be 8 or higher for a high response speed of load changing. In a sleep mode, however, a minimum value of 2 is designed for m_1 to reduce the power overhead. The combination of $(m_1, m_2) = (2, 2)$ results in double-half-frequency scaling [14], which is a special case in the proposed power-law frequency scaling scheme.

n_1 and n_2 should be designed to prevent f_{CLK} oscillation between $f_{CLK} \times m_1$ and $f_{CLK} \div m_2$. The constraints on n_1 and n_2 can be represented as

$$n_2 \times \frac{1}{m_2} > n_1 \tag{7}$$

$$n_1 \times m_1 > n_2. \tag{8}$$

Therefore, f_{CLK} is stable between n_1 and n_2, and its relation with f_{SW} in the steady state can be expressed as

$$f_{CLK} = K \times f_{SW} \tag{9}$$

where K is a natural number and a function of n_1 and n_2. f_{CLK} is determined by the power-law frequency scaling scheme according to the load conditions, making the CHC buck converter able to operate stably without f_{CLK} oscillation. Under the same I_{LOAD} condition, choosing a larger value of K results in a higher f_{CLK}. An additional benefit here compared with a conventional hysteresis control is that the switching frequency f_{SW} is fixed to $1/K \cdot f_{CLK}$. Using the frequency scaling scheme, the power consumption of the clocked comparator can be adjusted to be proportional to I_{LOAD}. The simulated dependence of the power consumption of X_1, X_2, and X_3 on f_{CLK} when $K = 3$ is shown in Fig. 8. Obviously, the power consumption of X_1, X_2, and X_3 can all be scaled with I_{LOAD}.
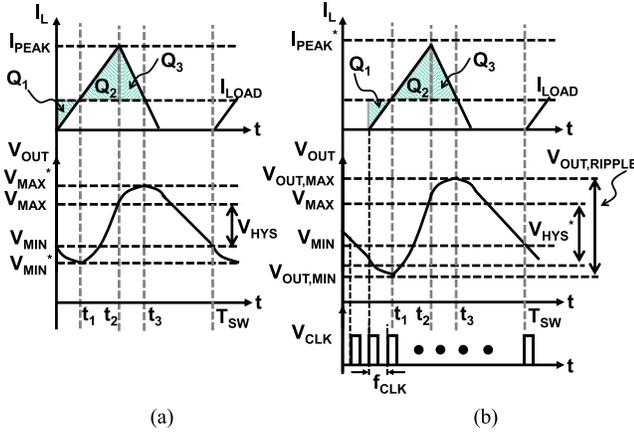
Fig. 9. Inductor current and output voltage waveforms. (a) Conventional hysteresis buck converter. (b) Proposed CHC buck converter with clock timing.

Fig. 10. Simulated and calculated T_{SW} and I_{PEAK} by (13) and (14) under different load conditions.

B. Analysis of Output Voltage Ripple

By applying the proposed power-law frequency scaling scheme in the CHC, the buck converter employs no continuously on comparators, resulting in no consumption of dc current by the comparators. The output voltage ripple $V_{OUT,RIPPLE}$, however, is enlarged because comparator X_1 only compares the output voltage with V_{MIN} at the clock edge. In addition, the "real" minimum output voltage level $V_{OUT,MIN}$, which is lower than V_{MIN}, should be analyzed to ensure that the lowest output voltage level is not lower than the specification value. By the proposed theoretical analysis, design guidelines for V_{MAX} and V_{MIN} are provided so that the CHC buck converter can achieve competitive performance with a conventional buck converter while improving the conversion efficiency in a sleep mode.

To analyze the voltage ripple of the CHC buck converter, the voltage ripple of conventional hysteresis control is derived first. The inductor current waveforms I_L, I_{LOAD}, and V_{OUT} for a conventional hysteresis control buck converter are illustrated in Fig. 9(a). I_{PEAK} is the peak inductor current value, $V_{MAX} - V_{MIN}$ is the hysteresis window, denoted by V_{HYS}, and I_{LOAD} is the load current. Because of the time delay between the inductor current and the output voltage, the maximum and minimum output voltages, denoted by V_{MAX}^* and V_{MIN}^*, are higher and lower than V_{MAX} and V_{MIN}, respectively. Therefore, $V_{MAX}^* - V_{MIN}^*$ represents the output voltage ripple. When the output capacitor equivalent series resistance is neglected for simplicity, the peak inductor can be expressed as [15]

$$I_{PEAK} = I_{LOAD} + \sqrt{I_{LOAD}^2 + 2C_{OUT}\alpha_1 V_{HYS}} \quad (10)$$

where $\alpha_1 = (V_{IN} - V_{OUT})/L$ and $V_{HYS} = V_{MAX} - V_{MIN}$. Using charge balance analysis [16] in combination with (10), the output voltage ripple can be expressed in terms of only the given specification parameters of the system such as V_{IN}, V_{OUT}, V_{HYS}, L, C_{OUT}, and I_{LOAD}

$$V_{OUT,RIPPLE} = \frac{1}{2C_{OUT}}\left(I_{LOAD}^2 + 2C_{OUT}\alpha_1 V_{HYS}\right)\frac{V_{IN}}{V_{OUT}}\frac{1}{\alpha_1}. \quad (11)$$
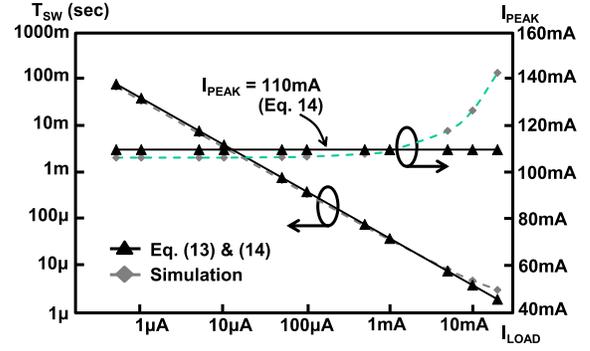
A similar equation can also be found in [17] although it involves the switching period and cannot refer to the specification parameters directly.

For IoT sensor node applications, the maximum I_{LOAD} usually ranges from milliampere to 10-mA order. In this case, the $2C_{OUT}\alpha_1 V_{HYS}$ term in (10) is much larger than I_{LOAD}^2 term when a microfarad output capacitor and a microhenry inductor are applied. Therefore, (11) can be simplified to

$$V_{OUT,RIPPLE}(0) = V_{HYS} \times \frac{V_{IN}}{V_{OUT}}. \quad (12)$$

Equation (12) provides a simple estimation of the output voltage ripple that is only dependent on V_{IN}, V_{OUT}, and V_{HYS}. Equation (12) is defined as the intrinsic output voltage ripple of a hysteresis buck converter, indicating the theoretical minimum output ripple that it can achieve. In addition, the switching period T_{SW} and I_{PEAK} can also be simplified as follows when $\sqrt{2C_{OUT}\alpha_1 V_{HYS}} > I_{LOAD}$:

$$T_{SW} = \frac{C_{OUT}}{I_{LOAD}}V_{HYS}\frac{V_{IN}}{V_{OUT}} \quad (13)$$

$$I_{PEAK} = \sqrt{2C_{OUT}\alpha_1 V_{HYS}}. \quad (14)$$

Equations (12)–(14) can be used to calculate the output voltage ripple, switching period, and peak inductor current very simply when the load current is relatively small compared with I_{PEAK}, which is the usual case in IoT applications. The values of T_{SW} and I_{PEAK} calculated by (13) and (14) compared with simulation results under different I_{LOAD} are shown in Fig. 10. Equations (13) and (14) match the simulation results well and provide a simple means of calculating T_{SW} and I_{PEAK} for a conventional hysteresis buck converter when I_{LOAD} is much lower than I_{PEAK}. In addition, on the basis of (12)–(14), the voltage ripple of the proposed CHC buck converter can be calculated.

Fig. 9(b) shows the inductor current waveform I_L, I_{LOAD}, V_{OUT}, and the clock signal V_{CLK} when CHC is applied. The clocked comparator compares V_{OUT} and V_{MIN} at every clock edge. The effective hysteresis window V_{HYS}^*, however, is enlarged by a limited clock frequency f_{CLK} and K as indicated by (9). The worst case of $V_{OUT,RIPPLE}$ is when the clock arrives but V_{OUT} is slightly higher than V_{MIN}. Therefore, V_{HYS}^* is effectively enlarged by a factor
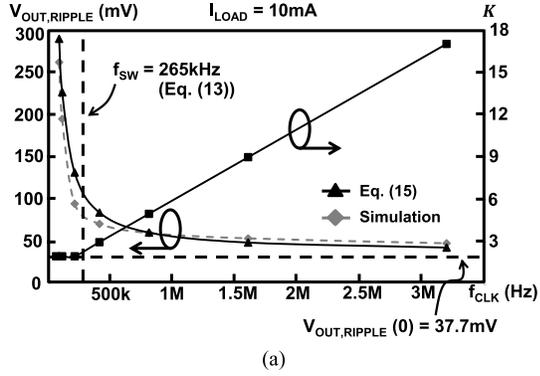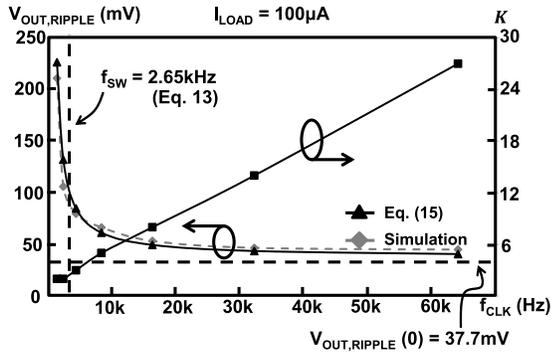
Fig. 11. Simulated and calculated dependences of output voltage ripple on clock frequency f_{CLK}. (a) $I_{LOAD} = 10$ mA. (b) $I_{LOAD} = 100$ μA.

Fig. 12. Simulated and calculated output voltage ripple for I_{LOAD} with a fluctuation varying from 5% to 30% in a stepped manner with different values of K. (a) $I_{LOAD} = 10$ mA. (b) $I_{LOAD} = 100$ μA.

of $T_{OSC} \times I_{LOAD}/C_{OUT}$. Therefore, $V_{OUT,RIPPLE}$ can be calculated as

$$V_{OUT,RIPPLE}(CHC) = \frac{V_{IN}}{V_{OUT}}\left(V_{HYS} + \frac{I_{LOAD}}{C_{OUT}}T_{CLK}\right). \quad (15)$$

The calculated and simulated dependences of $V_{OUT,RIPPLE}$ on f_{CLK}, including the simulated K under $V_{IN} = 3$ V, $V_{OUT} = 1.6$ V, $V_{HYS} = 20$ mV, $C_{OUT} = 1$ μF, $L = 4.7$ μH, and $I_{LOAD} = 10$ mA and 100 μA, are shown in Fig. 11(a) and (b), respectively. When f_{CLK} is closed to the switching frequency f_{SW} calculated by (13), the output voltage ripple increases steeply. On the other hand, when a higher f_{CLK} is applied, $V_{OUT,RIPPLE}$ becomes smaller and close to the intrinsic output voltage ripple calculated by (12) at the cost of higher power consumption.

C. $V_{OUT,RIPPLE}$ and $V_{OUT,MIN}$ Under I_{LOAD} Fluctuation

The lowest output voltage level $V_{OUT,MIN}$ and the maximum voltage ripple $V_{OUT,RIPPLE}$ of the proposed CHC buck converter under time-dependent I_{LOAD} fluctuation should be calculated. Unlike a conventional buck converter only depending on the output capacitor and the converter loop bandwidth, f_{CLK} and K determine $V_{OUT,MIN}$ and $V_{OUT,RIPPLE}$. Considering that the I_{LOAD} fluctuation is not sufficiently large to change f_{CLK} to $m_1 \times f_{CLK}$, a large value of K is required to keep the minimum output voltage level above the system specifications. Equation (15) gives the worst ripple voltage, and K is determined by preset numbers n_1 and n_2. Fig. 12(a) and (b) shows the simulated dependences of

the output voltage ripple performance of the proposed CHC buck converter on K under $I_{LOAD} = 10$ mA and 100 μA, respectively. The load current is assumed to have a fluctuation of up to 30%. The calculation results obtained from (15) and a PFM control with an adaptive on-time buck converter [18] are also illustrated in Fig. 12(a) and (b) for comparison. The simulation is carried out with $V_{IN} = 3$ V, $V_{OUT} = 1.6$ V, $V_{HYS} = 20$ mV, $L = 4.7$ μH, and $C_{OUT} = 1$ μF. A larger value of K indicates that a higher f_{CLK} is applied as shown in Section III-A. When $K = 2$, the output voltage is easily affected by load fluctuation. In addition, when $K = 3$, the CHC buck converter achieves competitive voltage ripple performance with the adaptive on-time control buck converter. Applying $K = 5$, the voltage ripple of the CHC buck converter is lower than that of the conventional one when the I_{LOAD} fluctuation varies from 5% to 30%. Therefore, $K = 3$ is chosen for low-power consumption with acceptable output voltage ripple.

To ensure that the minimum output voltage is higher than the value specified by the system, the lower bound of the voltage hysteresis window V_{MIN} should be designed so that is satisfies

$$V_{OUT,MIN}(CHC) = V_{MIN} - \frac{I_{LOAD}}{C_{OUT}}T_{CLK} - \frac{Q_L}{C_{OUT}} \quad (16)$$

where Q_L can be expressed as

$$Q_L = \frac{I_{LOAD} \times t_D}{2}, \quad t_D = \frac{I_{LOAD} \times L}{V_{IN} - V_{OUT}} \quad (17)$$

and the comparator delay is neglected for simplicity. When I_{LOAD} is 10 mA, $V_{IN} = 3$ V, and $V_{OUT} = 1.6$ V,
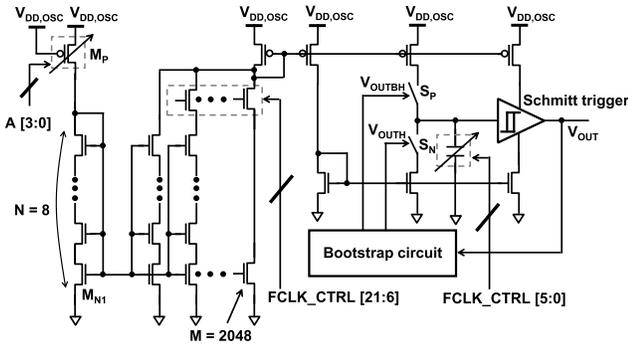
Fig. 13.   Circuit schematic of the leakage-based DCO.

V_{MIN} = 1.57 V gives the CHC buck converter with a minimum output voltage no lower than 3.4% of V_{OUT}, and $V_{\text{OUT,RIPPLE}}$ < 6% of V_{OUT} when K = 3. Therefore, the design parameters m_1 = m_2 = 2, n_1 = 2, and n_2 = 5, resulting in K = 3, which is the case shown in Fig. 7(a) and (b), are chosen to implement the proposed CHC buck converter.

IV. CIRCUIT IMPLEMENTATION

A. Leakage-Based Digitally Controlled Oscillator (DCO)

An on-chip DCO is implemented to provide a clock signal to the clocked comparator X_1. The clock frequency is able to be controlled digitally using a factor of 2 and ranges from hertz to megahertz order for both active and sleep modes. A circuit schematic of the DCO is shown in Fig. 13. As the DCO is the only continuously on circuit block in the CHC buck converter, the power consumption should be minimized so that it does not limit the sleep mode conversion efficiency. The transistor leakage current is designed as the bias current provided to the current mirror. The 4-bit signals A [3:0] are used to control the transistor size of M_P and the leakage current according to the process, voltage, and temperature (PVT) variation. A [3:0] can be generated by additional calibrations or implementing a PVT sensors on a chip [19], [20]. This current is mirrored to charge and discharge the capacitors, generating a sawtooth voltage waveform. A current-starved Schmitt trigger is used as a comparator and output buffer so that there is no need to use an additional reference. Therefore, a square clock waveform can be obtained at the output of the Schmitt trigger. The frequency tuning is separated to control both the transistor multiplier ratio and the number of capacitors. The 22-bit thermometer codes, $F_{\text{CLK\_CTRL}}$ [21:0], are used to adjust the clock frequency monotonically over a frequency tuning range of 10^6. In addition, stacked transistor technology is employed to design M_{N1} to dramatically reduce the transistor area. Therefore, the MSB nMOS transistor multiplier ratio can be reduced to 2048, which can be implemented on a test chip.

To reduce the oscillator power consumption, a supply $V_{\text{DD,OSC}}$ with a lower voltage is preferred. A bootstrap circuit employing the concept in [21] is designed to boost the voltage level of V_{OUT} when the Schmitt trigger is switching. Therefore, switches S_N and S_P can be fully turned ON to charge and discharge the capacitor even when $V_{\text{DD,OSC}}$ is as

low as 0.6 V. An additional low-dropout regulator (LDO) or a switched capacitor (SC) dc–dc converter can be employed to generate this supply voltage. The measurement results show that the DCO consumes only 5.6 nA at 15 Hz and 50.4 μA at 6 MHz when $V_{\text{DD,OSC}}$ is 0.6 V. Therefore, it is possible to design the LDO or the SC dc–dc converter [22] on a chip with high conversion efficiency and a compact area although this has not been implemented in the current design.

The frequency scaling scheme applied to the DCO may generate interference that interferes with sensitive circuits on the chip. In the sleep mode, however, the clock frequency is only 10-Hz order, which is far from the usual RF signal frequency. In addition, there are no RF circuits enabled in the sleep mode. On the other hand, in the active mode, a system clock with a higher frequency, for example, 32 MHz, can be applied as a base frequency for the power-law frequency scaling scheme instead of using the internal leakage-based DCO.

B. Clocked Comparator and Analog Comparator With Enable Signal

A circuit schematic of clocked comparator X_1 is shown in Fig. 2(b). A clocked comparator with a latch load [14] is employed to compare V_{OUT} with V_{MIN}. The output followed by a D flip-flop generates a control signal to turn ON the power transistor M_P. The input differential pair is designed with a large transistor width and length to reduce the offset voltage. The 1-sigma simulated and calculated offset voltages [23] are less than 2 mV, which does not have a large effect on the voltage hysteresis window.

Fig. 2(c) shows a circuit schematic of the power-gated comparator with an enable signal. Comparator X_2 compares V_{OUT} with V_{MAX}, and is enabled when V_{OUT} is lower than V_{MIN} and turned OFF when V_{OUT} becomes higher than V_{MAX}. Similarly, a p-type input differential pair with an nMOS active load power-gated comparator is designed for X_3 because the comparator compares the V_X node with the ground. X_3 is turned ON when V_{OUT} becomes higher than V_{MAX} and turned OFF when the inductor current reaches zero. The settling time due to the enable signal in the comparators is not an issue because the bias points in the comparators only need to settle in a time of 100-ns order. To demonstrate the benefit of the proposed CHC, the power distribution of the comparators is simulated. The simulation shows that the power consumptions of X_1, X_2, and X_3 are all lower than 1% of the output power when applying f_{CLK} = 100 Hz under I_{LOAD} = 1 μA.

C. Voltage Level Shifter

The proposed CHC buck converter targets BLE applications for which the input voltage could be a battery with a voltage ranging from 2.4 to 3.3 V. However, a lower supply voltage is preferred for the leakage-based DCO to reduce the power consumption. A conventional level shifter with a short current reduction topology [24] cannot convert a clock signal with a low voltage such as 0.6–3.3 V when the clock frequency is in the megahertz order. Fig. 14 shows the designed voltage level shifter. An auxiliary bootstrap circuit is designed to
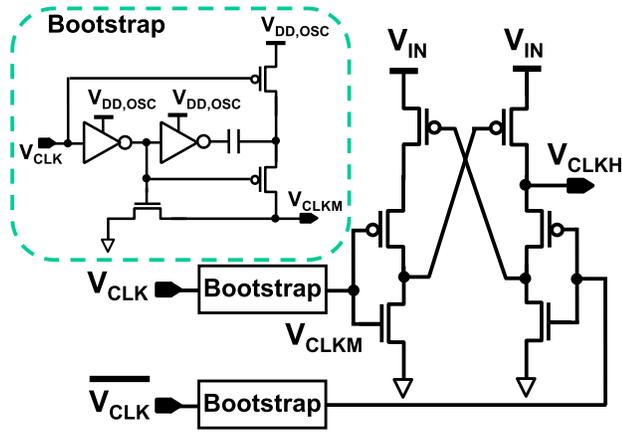
Fig. 14. Schematic of the voltage level shifter, which converts 0.6–3.3 V with the frequency ranging from 1 Hz to 5 MHz.
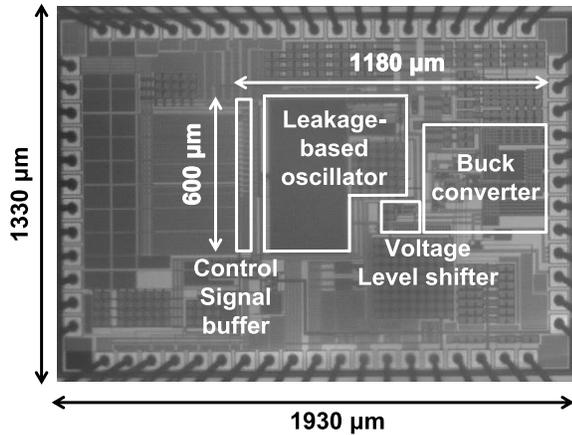
Fig. 15. Chip micrograph of the proposed CHC buck converter.

(a)

(b)

Fig. 16. Measured waveforms of V_{OUT}, V_{CLK}, and V_{OUT_LOW} under different loading conditions. (a) $V_{IN} = 3$ V, $V_{OUT} = 1.6$ V, $V_{HYS} = 20$ mV, and $I_{LOAD} = 100$ μA. (b) $V_{IN} = 3$ V, $V_{OUT} = 1.6$ V, $V_{HYS} = 20$ mV, and $I_{LOAD} = 2$ mA.

boost the amplitude of the input clock signal V_{CLK} to nearly $2V_{DD,OSC}$ ($\sim$1.2 V), and the voltage level shifter can shift V_{CLKM} to V_{CLKH} functionally. The worst case is when the clock frequency is low. In this case, the bootstrap circuit cannot boost the input voltage for a long period. Simulation results show that the voltage level shifter can convert the input signal from 0.6 to 3.3 V when the frequency ranges from 1 Hz to 5 MHz. The voltage level shifter consumes 380 pW at 1 Hz and 44.5 μW at 5 MHz.

V. EXPERIMENTAL RESULTS

The proposed CHC buck converter implemented with the double-half-frequency scaling scheme ($m_1 = 2$ and $m_2 = 2$) is fabricated by a 0.18-μm standard CMOS process for verification. I/O transistors are used to design buck converter core circuits that should withstand an input voltage of 3.3 V, and switches providing a low leakage current. Fig. 15 shows the chip micrograph. The active area including the buck converter core circuits, leakage-based DCO, voltage level shifter, and buffers is 0.71 mm². The test chip is measured with a 4.7-μH off-chip inductor and a 1-μF off-chip capacitor, and the frequency scaling scheme is realized using an Altera Cyclone V FPGA. Fig. 16(a) and (b) shows the

steady-state waveforms of V_{OUT}, V_{CLK}, and V_{OUT_LOW} under $V_{IN} = 3$ V, $V_{MIN} = 1.57$ V, and $V_{MAX} = 1.59$ V when $I_{LOAD} = 100$ μA and 2 mA, respectively. The voltage hysteresis window V_{HYS} is set to 20 mV for all measurements. The frequency scaling scheme is designed to minimize the power consumption of the comparator and controller. Therefore, $n_1 = 2$ and $n_2 = 5$ are used, resulting in $K = 3$ in (9). As shown in Fig. 16, the pMOS power transistor M_P is turned ON every three V_{CLK} clock cycles. As discussed in Section III, m_1, m_2, n_1, and n_2 can be changed easily according to the specifications for different applications, such as a high wakeup response speed or a low output voltage ripple. The measurement results show that the output voltage is regulated at 1.6 V with a voltage ripple lower than 100 mV, which is about 6% of the output voltage. Using the frequency scaling scheme, the clock frequency of V_{CLK} automatically settles to 3.57 and 94 kHz when $I_{LOAD} = 100$ μA and 2 mA, respectively.

To verify the load wakeup operation, I_{LOAD} changed from 30 μA to 2 mA is applied to the output. The signal WAKE_UP resets the clock frequency to the highest value, and the clock frequency is settled in the steady state by the frequency scaling scheme as shown in Fig. 17(a). Fig. 17(b) shows the detailed waveforms of V_{OUT}, V_{CLK}, and WAKE_UP. The clock frequency changes from 780 Hz to 55 kHz at 2-mA loading without an obvious voltage drop.

Fig. 18 shows the measured clock frequency and power consumption versus F_{CLK_CTRL} [21:0] for the leakage-based

(a)

(b)
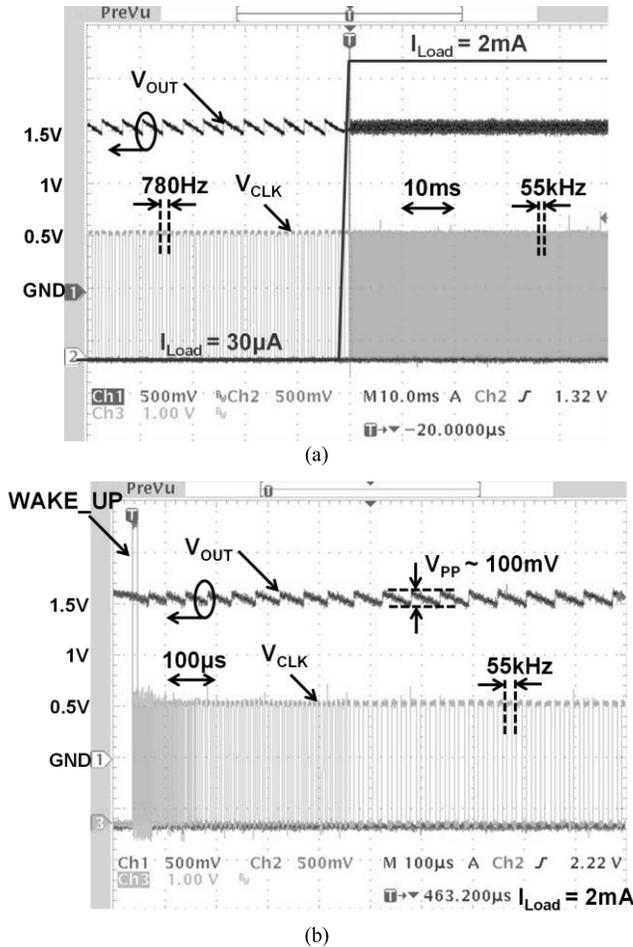
Fig. 17. Measured load wakeup operation when I_{LOAD} is changed from a sleep mode (30 μA) to an active mode (2 mA). (a) Time scale = 10 ms. (b) Time scale = 100 μs.
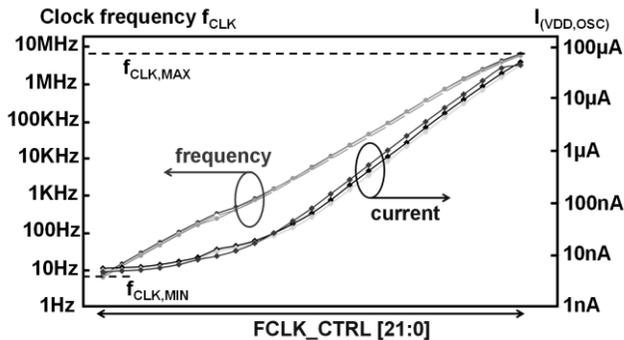
Fig. 18. Measured clock frequency and power consumption relationship for the proposed DCO in Fig. 13 when digital bit of F_{CLK_CTRL} is changed.

DCO. The clock frequency is controlled by a 22-bit thermometer code with 16 bits in the transistor multiplier ratio and 6 bits in the capacitor bank. Three chips are measured, showing that the frequency can be adjusted monotonically without large frequency and power variations. Upon applying a 0.6-V supply voltage, the DCO consumes 3.4 nW and 30.2 μW when the clock frequency is 15 Hz and 6.3 MHz, respectively. In addition, the DCO power consumption is also
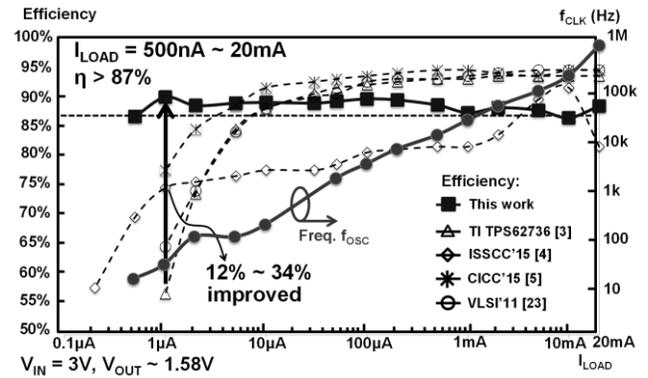
Fig. 19. Measured conversion efficiency and clock frequency f_{CLK} versus I_{LOAD} and comparison with state-of-the-art low-power buck converters.

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED CHC BUCK CONVERTER AND COMPARISON WITH STATE-OF-THE-ART BUCK CONVERTERS

	ISSCC'15 [4]	CICC'15 [5]	VLSI'15 [6]	VLSI'11 [25]	This work
Technology	180nm CMOS	350nm CMOS	180nm CMOS	250nm CMOS	**180nm CMOS**
Die size	1.44mm²	2.88mm²	2.42mm²	0.21mm²	**0.71mm² ***
V_{IN} (V)	0.6/1.2	2.2 − 6	3	1.2 − 2.5	**2.4 − 3.3**
V_{OUT} (V)	0.35 − 0.5	2.5	1	1	**1.5 − 1.6**
I_{LOAD}	100nA − 20mA	1µA − 100mA	10nA − 1µA	1µA − 100mA	**500nA − 20mA**
Peak eff. η_{PEAK}	92%	95%	87%	95.2	**90.4%**
η @ I_{LOAD} =1µA	75%	78%	87%	65%	**90.4%**
Inductor value L	4.7µH	2.2µH	47µH	1.5µH	**4.7µH**
Control methodology	PWM, PFM, and AM	Hysteresis control	Constant on-time	Dynamic on/off time	**Clocked hysteresis control**

* Active area

proportional to the loading current because the frequency is mainly controlled by the transistor multiplier ratio in the current mirror. The power distribution of the DCO accounts for less than 1% of the output power of the CHC buck converter when operating in both the sleep and the active modes.

The measured dependence of the efficiency and clock frequency f_{CLK} on the load current is shown in Fig. 19. The proposed CHC buck converter achieves almost flat conversion efficiency by removing continuously on comparators and applying the double-half-frequency scaling scheme. The frequency scaling scheme is also verified on the y-axis on the right-hand side of Fig. 19. Higher than 87% conversion efficiency is achieved over a load current ranging from 500 nA to 20 mA. When I_{LOAD} = 1 μA, which is defined as the sleep current in BLE, efficiency is improved by 12%–34% compared with that of state-of-the-art low-power buck converters. A comparison of performance with state-of-the-art buck converters is shown in Table II. The proposed CHC buck converter achieves higher than 87% conversion efficiency over 500 nA–20 mA with a peak efficiency of 90.4%. In addition, compared with the state-of-the-art buck converters, a higher efficiency at 1 μA is also achieved. The input voltage, output voltage, and loading current are designed for

BLE applications. CHC with the double-half-frequency scaling scheme was also proposed to remove the continuously on comparators in the conventional hysteresis buck converter. The frequency scaling scheme is also suitable for other converters that employ continuously on comparators.

VI. CONCLUSION

A CHC buck converter operating in DCM with a power-law frequency scaling scheme is developed to remove the continuously on comparators used in conventional hysteresis control, resulting in no dc current being consumed by the comparators. The frequency of the clocked comparator is dynamically adjusted in accordance with the load conditions. Therefore, the conduction loss, switching loss, and comparator power consumption in the converter can all be scaled with the load. By applying the proposed topology, the CHC buck converter achieves almost flat conversion efficiency over the entire load current range. The frequency stability, output voltage ripple, and minimum output voltage level of the buck converter when the power-law frequency scaling scheme is applied are analyzed to provide design guidelines for the system. A CHC buck converter with the double-half-frequency scaling scheme is implemented to verify the power-law frequency scaling. Experimental results demonstrate that the buck converter achieves conversion efficiency of higher than 87% over I_{LOAD} ranging from 500 nA to 20 mA with a peak value of 90.4%. The conversion efficiency is particularly improved when I_{LOAD} is 1 μA. The I_{LOAD} wakeup operation with the frequency scaling scheme is also verified. The proposed buck converter achieves high conversion efficiency in a sleep mode with a quick wakeup response, making it extremely suitable for IoT sensor node applications.

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