A 500-Mbps Digital Isolator Circuits using Counter-Pulse Immune Receiver Scheme for Power Electronics

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***Abstract*—A 500-Mbps digital isolator with the isolation voltage more than 1kV is described, which is the fastest high-voltage isolator ever reported. The high-speed feature is achieved by a newly proposed Counter-Pulse Immune Receiver (CPIR) scheme based on a cross-coupled Schmitt-trigger circuit. The isolator is manufactured in a widely-used high-voltage 0.18-µm CMOS technology and thus can be integrated with smart digital driver circuits for power electronics.**

Keywords-digital isolator, power electronics, inductive coupling, high-speed

I. INTRODUCTION

Recently in power electronics, a digital gate driver has been proposed to improve switching characteristics of power devices [1]. By driving the gate of the power device with an optimized waveform, the digital gate driver is shown to reduce voltage/current overshoot noise while keeping the power loss at the same level, compared with the conventional resistor driver. Although the digital gate driver improves the system performance, more digital bits are to be provided in the same amount of time than the conventional resistor driver as shown in Fig.1. For example, in the implementation in [1], 6-bit of digital data is to be provided in every 25-ns period, and the digital data should go across the high-voltage isolator at the rate of 240-Mbps. The higher speed is needed for the higher resolution (ex. 8-bit) or for the faster power devices (ex. SiC devices). Such high band-width of data may be transferred through multiple of digital isolators in parallel but then the cost and module volume increase. Consequently, higher-speed digital isolators are looked for in the next-generation power electronics.

In order to meet the requirement, this paper describes a 500-Mbps digital isolator based on an inductive coupling using two-chips configuration. A transmitter, TX, is implemented on one chip and the receiver, RX, is on the other chip. Both chips are made with a 0.18-µm BCD high-voltage process with >0.5-µm channel length, which is inherently much slower than the standard low-voltage short-channel CMOS and thus it is much more difficult to achieve high speed. In order to achieve high speed, a new circuit scheme is employed, namely, Counter-Pulse Immune Receiver (CPIR) scheme, where a pair of Schmitt trigger circuits are properly coupled to eliminate a counter-pulse problem. To ensure the isolation voltage higher than 1kV, a careful design of coils is carried out considering technology-circuit interaction, which is discussed in section III.

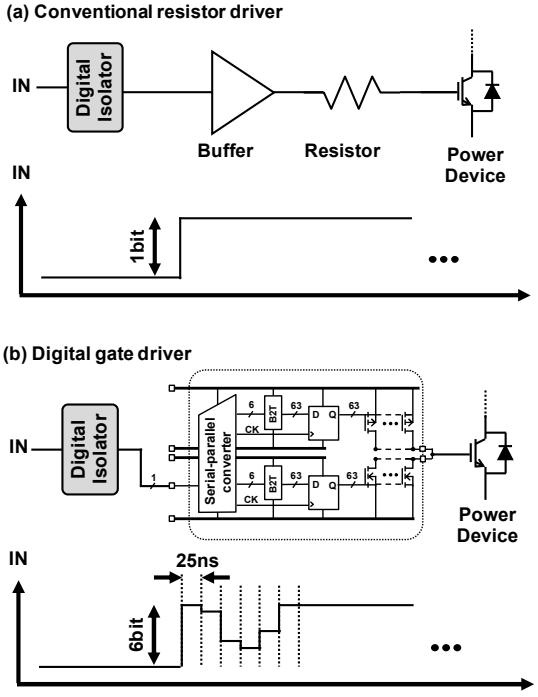

Fig. 1. Two different driving schemes for power devices

II. PREVIOUS ISOLATOR CIRCUITS

The fastest digital isolator for power electronics previously reported is described in [2]. The isolator uses an inductive coupling principle and an edge-detection scheme as opposed to a carrier-base on-off keying scheme. Thus, we adopt the inductive coupling and the edge detection concept, but the signaling protocol and the associated circuits are completely different to realize the higher speed. The conventional signaling protocol [2] is shown in Fig.2. Each edge in input data, IN, is translated to a unique current wave in TX-coil (I_{TX}). Then, a signal pulse and a counter pulse appear on the RX-coil (V_{RX}) corresponding to the unique I_{TX} wave as shown in Fig.2. The TX needs to blunt the falling edge of I_{TX} so that the counter pulse at RX should not translated as a signal. This requirement of blunting the I_{TX} falling edge slows down the signaling process and hence decreases the speed. On the other hand, the newly proposed scheme excludes this requirement for blunting by introducing novel RX circuits as described in Section III and thus achieves the higher speed.

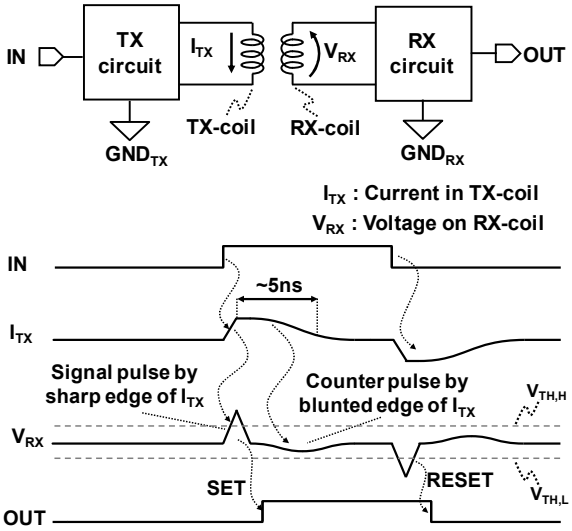

Fig. 2. Conventional signaling protocol for high-speed data transmission

A similar transceiver based on an inductive coupling has been reported for an inter-chip signaling among 3D stacked chips, which achieves very high-speed data transmission [3]. Although the concept of the data transmission using an inductive coupling is the same, the inter-chip signaling circuit doesn't need to integrate with a 15-V gate driver. That is, there is no need to use very long-channel BCD devices, which is orders of magnitude slower than the cutting-edge short-channel device. Moreover, there is no need to consider high-voltage isolation nor Common Mode Transition Immunity (CMTI). Thus, there is no meaning to compare the high-voltage digital isolator circuits with the inductive signaling circuits for inter-chip communication among 3D stacked chips.

III. Counter-Pulse Immune Receiver Scheme

A. Overall architecture

The overall architecture of the proposed digital isolator is shown in Fig.4. The isolator consists of two Si chips ensuring the high-voltage isolation. Since the TX must use low-resistance coil to increase current, I_{TX}, for higher speed, the top thick metal (metal layer 5: M5) is employed for the TX-coil. Then, the RX-coil must use the bottom metal (M1) to ensure the high-voltage isolation. Now that the RX-coil is made with M1, the RX-coil must not be close to the TX chip surface. Otherwise the high breakdown voltage cannot be achieved. As to the diameter of the coils, 250-μm is employed. In order to increase the speed, the bigger coil is preferable because it maximizes the received signal strength but if more than 250-μm diameter is used, the dummy metal should be laid out in the coil which negatively impact the signal strength.

The counter pulse problem is taken care at the RX side, being different from the previous scheme in Fig.2 where the problem is taken care at the TX side. The proposed signaling protocol is depicted in Fig.4. The detailed discussions are in Chapter B and C.

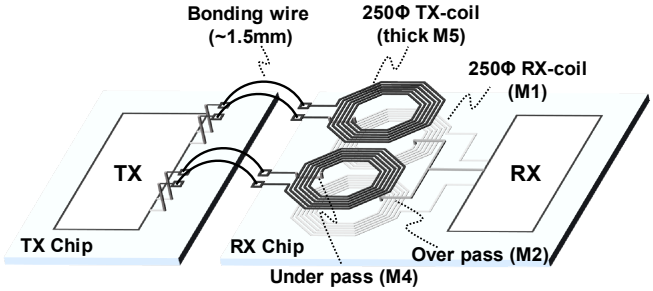

Fig. 3. Overall implementation of proposed digital isolator

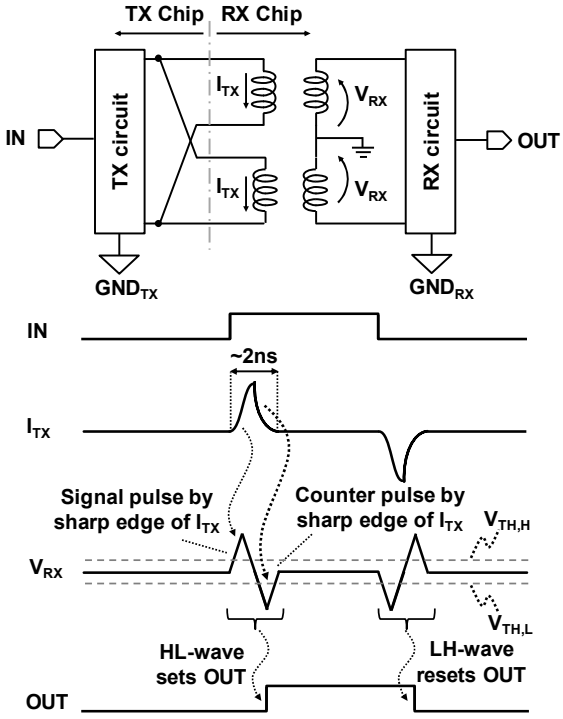

Fig. 4. Proposed signaling protocol for high-speed data transmission

B. Transmitter

The circuit diagram of the TX is shown in Fig.5. Being different from the previous scheme, there is no need to suppress the counter pulse on the TX side, the TX generates the fastest current pulse achievable by the slow BCD process. When input digital data (IN) comes in, the edges of IN are detected by edge detectors. When a rising edge of IN is detected, the coil driver DR1 outputs "H" (High) while DR2 outputs "L" (Low). The current in TX-coil, I_{TX}, starts increasing. This phase continues about 1ns. Then, DR1 outputs "L" and DR2 outputs "H", which starts decreasing I_{TX}. This phase should end when I_{TX} becomes zero. In order to fulfill this condition, the timing of the rising edge of the driver input, V_{C1}, can be tuned by 4 levels using the programmable fall-edge detector (P-FED). After all, a short positive current pulse of I_{TX} is generated as shown in Fig.5.

On the other hand, when a falling edge of IN is detected, similar circuit operation generates a negative current pulse of I_{TX} with a pulse width of about 2-ns.

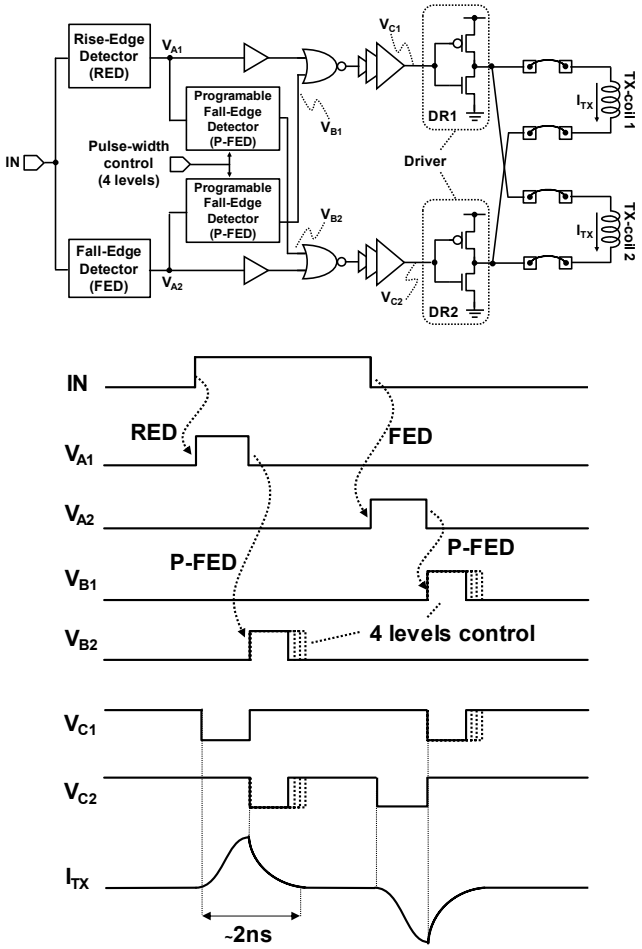

Fig. 5. Schematic and operation diagram of proposed TX circuit

C. Receiver: Counter-Pulse Immunity

The circuit diagram of the receiver is shown in Fig.6. When the positive current pulse of I_{TX} is transferred to the RX side, a voltage waveform like "HL-wave" in Fig.6 (b) is generated on RX-coil1 designated as V_{D1}, while a voltage waveform like "LH-wave" is generated at RX-coil2 designated as V_{D2}. First, these waves go through high pass filters (HPF) consisting of C and R in Fig.6(a). C is designed around 400-fF and R is chosen to be about 6.5-kΩ. This high pass filter eliminates slow voltage noise generated by Common-Mode Transition of GND_{TX} and GND_{RX} described in Chapter D to improve the CMT immunity.

The voltage waveform of V_{E1} is the same as V_{D1} while the DC voltage is shifted so that V_{E1} stays about a half V_{DD} in a signal waiting phase. In the signal waiting phase, Schmitt trigger circuit does not change its state unless an input noise goes beyond the range between $V_{TH,H}$ and $V_{TH,L}$, which does not happen. $V_{TH,H} - V_{TH,L}$ is set around 2 x 0.33-V. When "HL-wave" is applied to the Schmitt trigger, ST1, a negative pulse is generated at V_{F1}. The pulse length is properly enlengthened to result in V_{G2} pulse whose width is about 1-ns and this activates PMOS pull-up, PU2. When PU2 is activated, Schmitt trigger ST2 cannot output low, making ST2 dead for a while and neglect the positive pulse part in "LH-wave" of V_{E2}. This means that the RX neglects the counter pulse realizing a counter-pulse immune receiver.

Similarly, when "HL-wave" is applied to the Schmitt trigger, ST2, V_{F2} negative pulse is generated and it kills ST1 so that ST1 output pulse is suppressed. After all, the counter-pulse immunity is achieved even though the counter pulse is high, being different from the previous system. This ensures a fast digital signaling excluding intentionally blunted signal in the previous scheme. In essence, two Schmitt trigger circuits are cross-coupled so that a preceding signal pulse kills the succeeding counter pulse to realize the fast Counter-Pulse Immune Receiver.

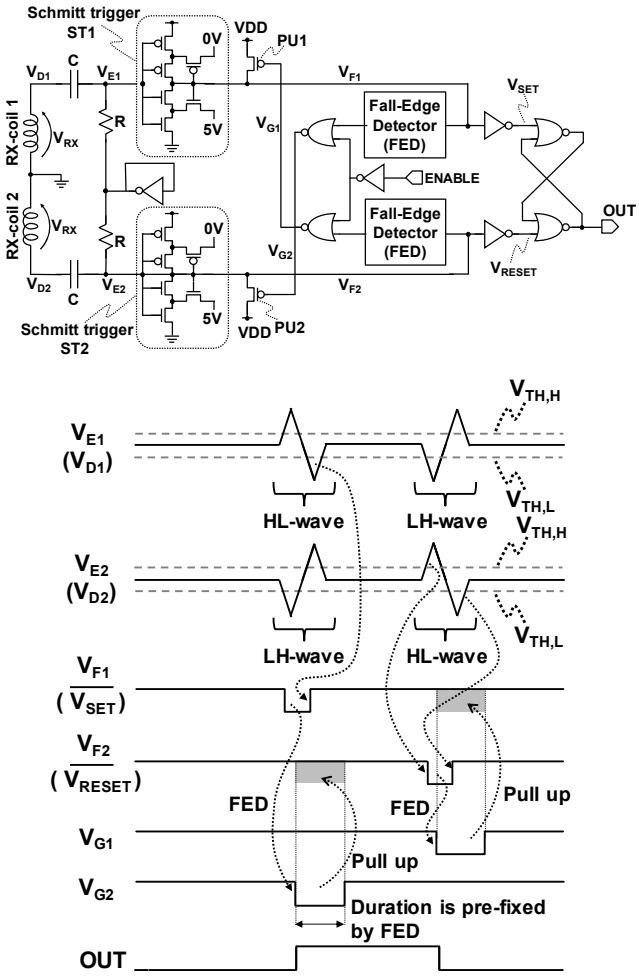

Fig. 6. Schematic and operation diagram of proposed RX circuit

D. Receiver: Common-Mode Transition Immunity

Common-Mode Transition Immunity (CMTI) is another important consideration for a digital isolator. The signaling should be carried out even when TX ground (GND_{TX}) and RX ground (GND_{RX}) is changing at the rate of dv/dt (kV/μs), the maximum value of which without an error is called CMTI. By inserting a proper high pass filter (HPF) at the

front of the RX circuit, the CMT noise can be mitigated. Fig.7 is the simulation results for the CMTI. The simulated CMTI for the proposed circuit is 130 kV/µs.

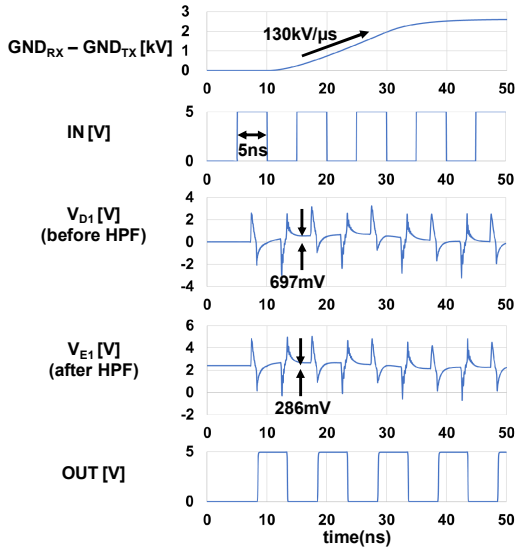

Fig. 7. Common-Mode Transition Immunity Simulation

IV. Measurement Results and Discussions

The chip has been manufactured with the 0.18-µm BCD process. The maximum gate voltage is 5V and the technology allows to implement 15-V output voltage driver needed for power devices such as IGBT's on the same chip. The photo of the assembled digital isolator with the proposed two-chips configuration is shown in Fig.8. 500-Mbps operation is demonstrated in Fig.9.

Table I shows a comparison with the prior publications. The proposed digital isolator circuit provides the fastest digital isolator. As a conclusion, a high-speed operation is achieved by the proposed CPIR scheme. Added to the high-speed operation, the proposed scheme is can be integrated with a smart digital driver needed in the next-generation power electronics.

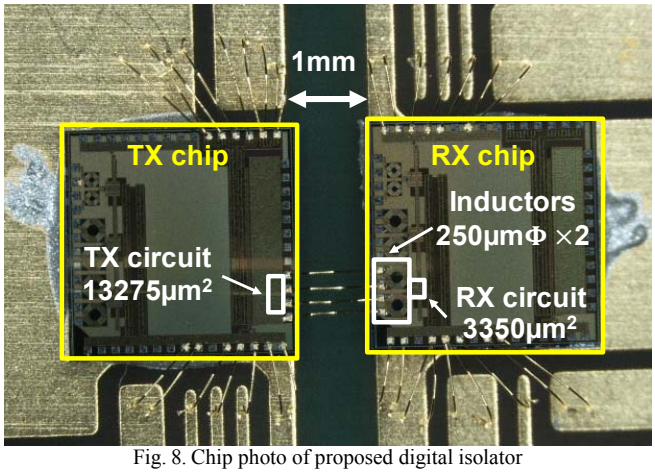

Fig. 8. Chip photo of proposed digital isolator

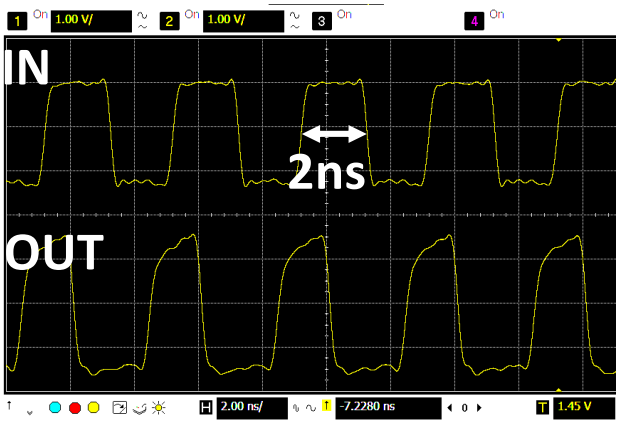

Fig. 9. Measured 500Mbps operation

Table 1. Comparison with prior publication

	This work	Ref. 2	Ref. 4	Ref. 5
Architecture	Edge detection	Edge detection	OOK	OOK
Process	5V 0.18µm CMOS (L_P=0.5µm ,L_N=0.6µm)	5V standard CMOS (L=0.54µm)	5V 0.18µm CMOS	-
Max data rate	500Mbps	250Mbps	-	150Mbps
IDD@1Mbps, 5V	1.16mA	1.6mA	2.8mA	3.3mA
Energy per bit @100Mbps, 5V	1.52nJ/bit	5nJ/bit	-	335pJ/bit
Number of transformers	2	1	2	2
Transformer Φ	250µm	230µm	-	500µm (estimated)
Isolation rating	>1kV (*)	2.5kV	20kV	2.5kV
Common-mode transition immunity	130kV/µs (simulation)	35kV/us	200kV/us	100kV/us

(*) Higher voltage experiments could not be conducted due to equipment limit.

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