Gate Waveform Optimization in Emergency Turn-off of IGBT Using Digital Gate Driver

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***Abstract*— IGBTs need to be immediately turned off when a short circuit occurs [1]. This paper discusses the optimized gate control in this emergency turn-off process. The optimized gate waveform minimizes the energy loss, hence the heat generation, while keeping the maximum collector-emitter voltage overshoot within a certain allowable value. The optimized waveform is found by theoretical analysis and is verified by measurements for the first time. Analytical expressions are derived for the optimized control, which explains well the experimental results. The optimized gate waveform is realized only by a digital gate driver (DGD) whose output drivability is programmable over 64 strength levels. The DGD decreases the energy loss by 22% compared with the conventional resistor gate driver [2,3,4].**

***Index Terms*—Gate driver, short-circuit, IGBT, Active gate control.**

I. Introduction

When a short circuit occurs in a leg of IGBTs, IGBT should be turned off immediately before it is broken by abnormal heat. The short circuit detection can be done in 20-ns [5], which is sufficiently fast, but the turn-off should be relatively slow to keep the collector-emitter voltage overshoot, Vov, within a tolerable level. Three ways to turn off the IGBT are investigated in this paper, namely a resistor drive, a single MOS drive, and Digital Gate Drive (DGD) as shown in Fig.1. The DGD chip was reported in the previous paper [6], which controls the gate waveform for power devices digitally by changing the number of switching MOS transistors dynamically up to 64 levels.

II. Theory for Optimum Waveform

In this section, an analysis is carried out to find the optimum gate drive waveform for the emergency turn-off. First, the current-voltage characteristics of an IGBT should be modeled using a simple expression for the analytical treatment. In this emergency turn-off process, IGBT is operated in the active region (constant-current region). In recent IGBTs, the collector current, I_C, in the active region is found not to follow the square-law model but rather can be modeled by the alpha-power law model [7], that is, $I_C=B(V_G - V_{TH})^{\alpha}$ where V_G is a gate voltage, V_{TH} is a threshold voltage of IGBT, B is constant, and α is current index ($1 < \alpha < 2$). This α-power model shows an excellent agreement with the measurement as shown in Fig.2. Since the short-circuit state is an operation in the active region of the IGBT, the α power law in the saturation region of the MOS (active region in the IGBT), which is a behavioral model taking into consideration the effects of velocity saturation and short channel effects, was applied for analysis. Using this model, the differential equations, Eq.1, should hold. This is to keep the voltage overshoot at the allowable maximum voltage, $V_{OV,MAX}$. C_G is gate

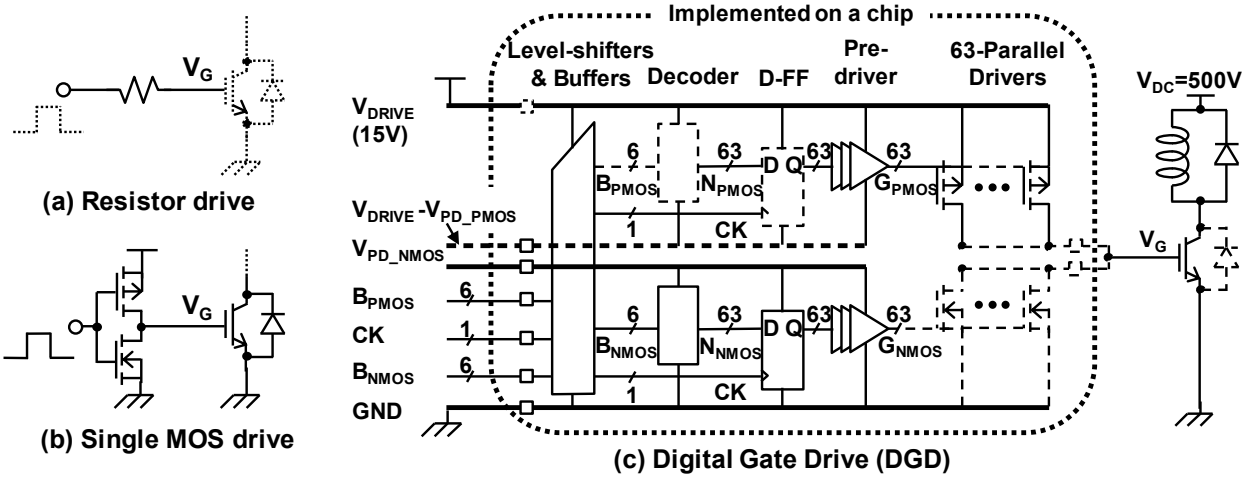


Fig. 1 Three ways to drive gate of IGBT: (a) conventional resistor drive, (b) single MOS drive, and (c) Digital Gate Drive (DGD) with 64-level of programmable current drivability [6].

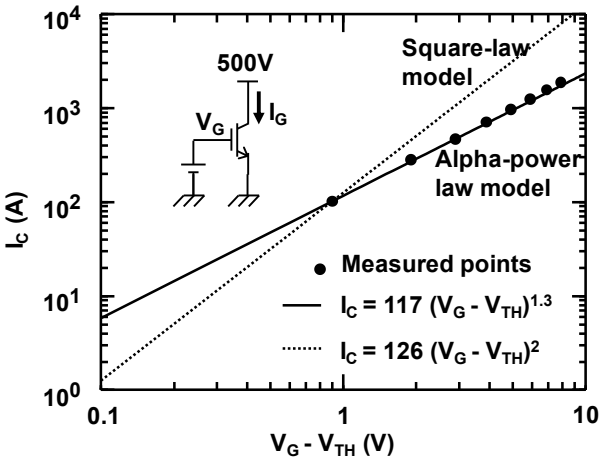


Fig. 2 α-power current model fits very well to measure.

$$\begin{cases} I_C = B\left(V_G - V_{TH}\right)^{\alpha} \\ C_G \dfrac{dV_G}{dt} = -I_G \\ -L\dfrac{dI_C}{dt} = V_{OV,MAX} \end{cases} \quad \text{(Eq.1)}$$

$$\begin{cases} V_G(t) = V_{TH} + \left[\left(V_{DD} - V_{TH}\right)^{\alpha} - \dfrac{V_{OV,MAX}}{BL}t\right]^{1/\alpha} \\ I_G(t) = \dfrac{C_G V_{OV}}{\alpha BL} \dfrac{1}{\left[\left(V_{DD} - V_{TH}\right)^{\alpha} - \dfrac{V_{OV,MAX}}{BL}t\right]^{(\alpha-1)/\alpha}} \end{cases} \quad \text{(Eq.2)}$$

with $\begin{cases} L = 105nH, \\ V_{DD} = 15V \\ C_G = 25nF \\ V_{OV,MAX} = 120V \\ B = 128,\ V_{TH} = 7.1V,\ \alpha = 1.3 \end{cases}$

capacitance of IGBT, I_G is gate current, I_C is collector current, and L is power supply bus inductance as shown in Fig.4. The differential equations, Eq.1, can be solved in terms of the optimum gate voltage, $V_G(t)$, and the optimum gate current, $I_G(t)$, as in Eq.2

Although the expressions seem complicated, if α is set to 2, V_G and I_G have the forms, $V_{TH} + \sqrt{a - bt}$ and $c/\sqrt{a - bt}$, which are a gradually decreasing and increasing function, respectively.

Considering the above discussions, the optimum gate drive current waveform, I_G, is as follows. First, the gate should be strongly pulled down using a high gate current. In this process, since V_{OV} is below $V_{OV,MAX}$ the faster turn-off is better in terms of energy loss. Then, after V_{OV} reaches $V_{OV,MAX}$, the gate current should follow the gradually increasing function as shown in Eq.2 to keep the V_{OV} at $V_{OV,MAX}$. This is the fastest turn-off process within the tolerant overshoot level while making the energy loss minimum.

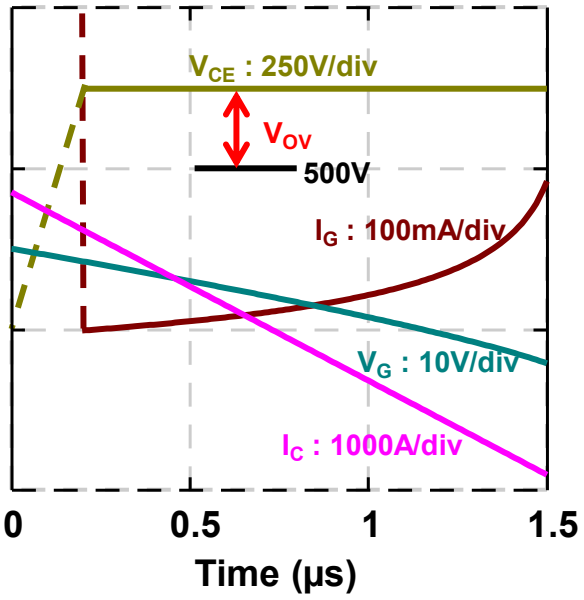
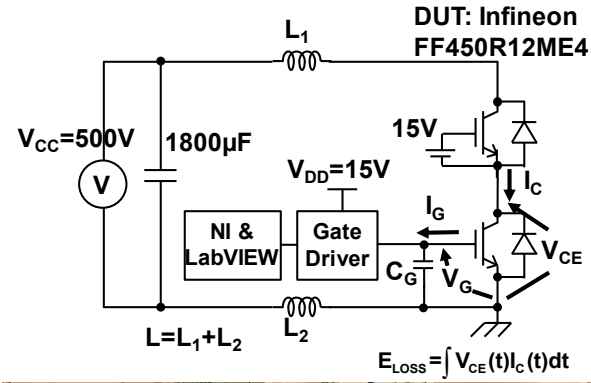


Fig. 3 Calculated optimum waveforms using theoretical expressions in Eq.2.



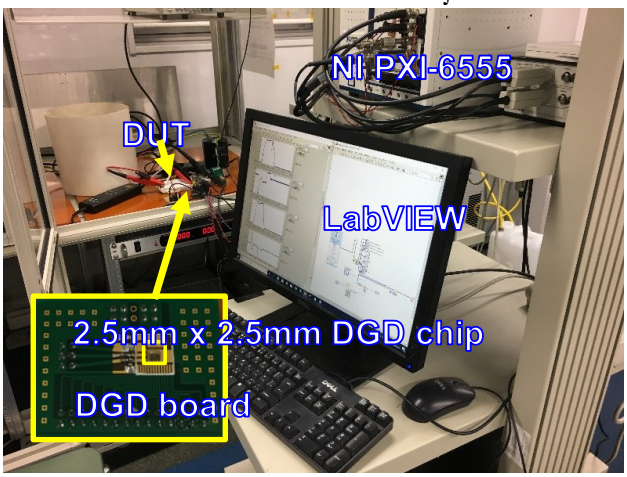


Fig. 4 Circuit scheme and equipment setup for measurements.

The optimized waveforms calculated by Eq.2 is shown in Fig.3 using the parameter values given on the right of Eq.2. These parameters correspond to the experiment in the next Section. It is not possible to realize the optimum I_G waveform by using a resistor [2,3,4] nor a single MOSFET. Thus, the DGD is used to verify the theory in Section III.

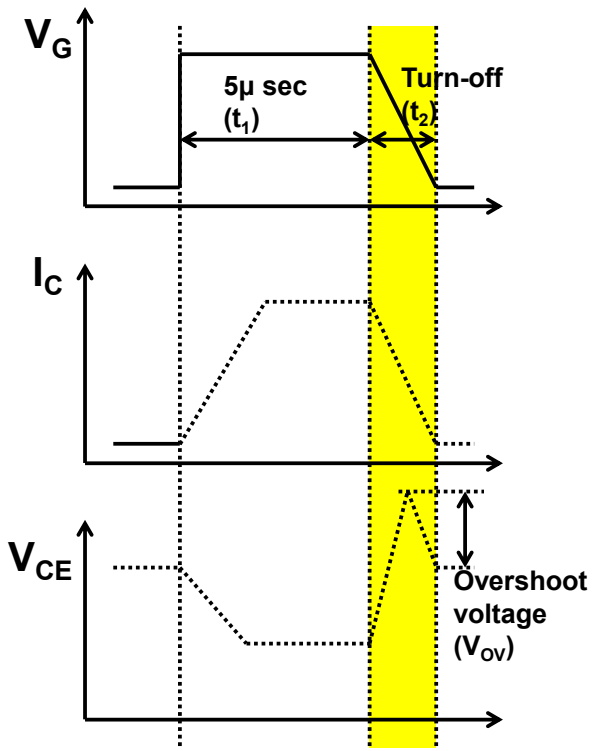


Fig. 5 schematic diagram of switching waveform.

III. Experimental Setup

The experimental setup shown in Fig.4 is used to measure the voltage and current of important points. The circuit for short-circuit measurement is composed of the IGBT module (Infineon FF450R12ME4) with a high side always on and a DGD board equipped with the DGD chip manufactured by TSMC 180nm BCD process. The measurement is performed by inputting a digital signal generated from the LabVIEW program on the PC through the NI PXI-6555 to the DGD board and measuring the switching waveform of the low-side IGBT.

A schematic diagram of the DGD output waveform and the IGBT switching waveform is shown in Fig.xx. First, the driver outputs high during t_1 to turn-on and cause a short-circuit. In this measurement, the period of t1 is fixed to 5 μ sec. After the short-circuit period of 5 u seconds, a turn-off signal is generated at time t_2, and overshoot voltage Vov and loss E_{LOSS} generated at this time are measured. The digital signal from LabVIEW dynamically changes the DGD output current I_G during t_2 to generate an arbitrary turn-off waveform.

In order to improve the trade-off relationship between V_{OV} and E_{LOSS} at the time of short-circuit protection, the turn-off waveform derived from the theory described above is generated to compare conventional resistance drive and single MOS drive.

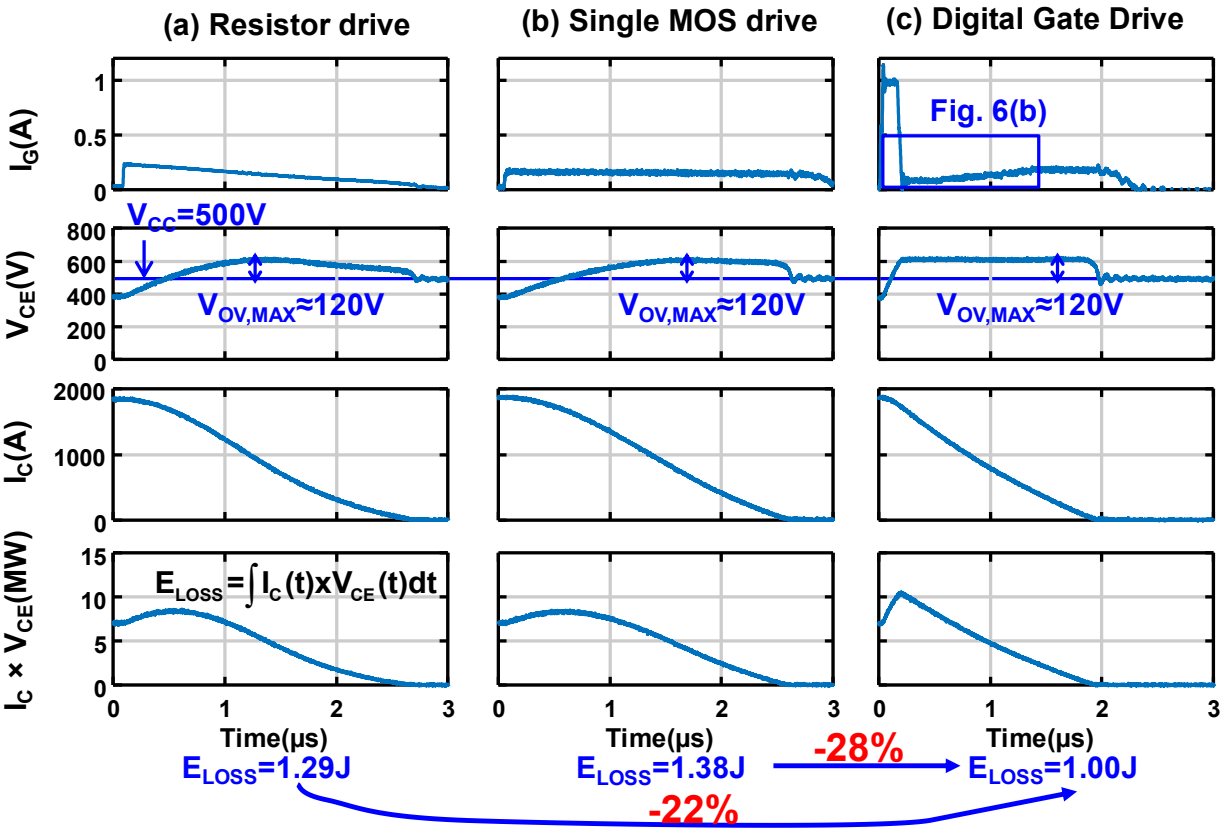


Fig. 6 Comparison among various drive methods. Optimum gate drive waveform realized by Digital Gate Drive reduces energy loss by 22% compared with the conventional resistor drive.

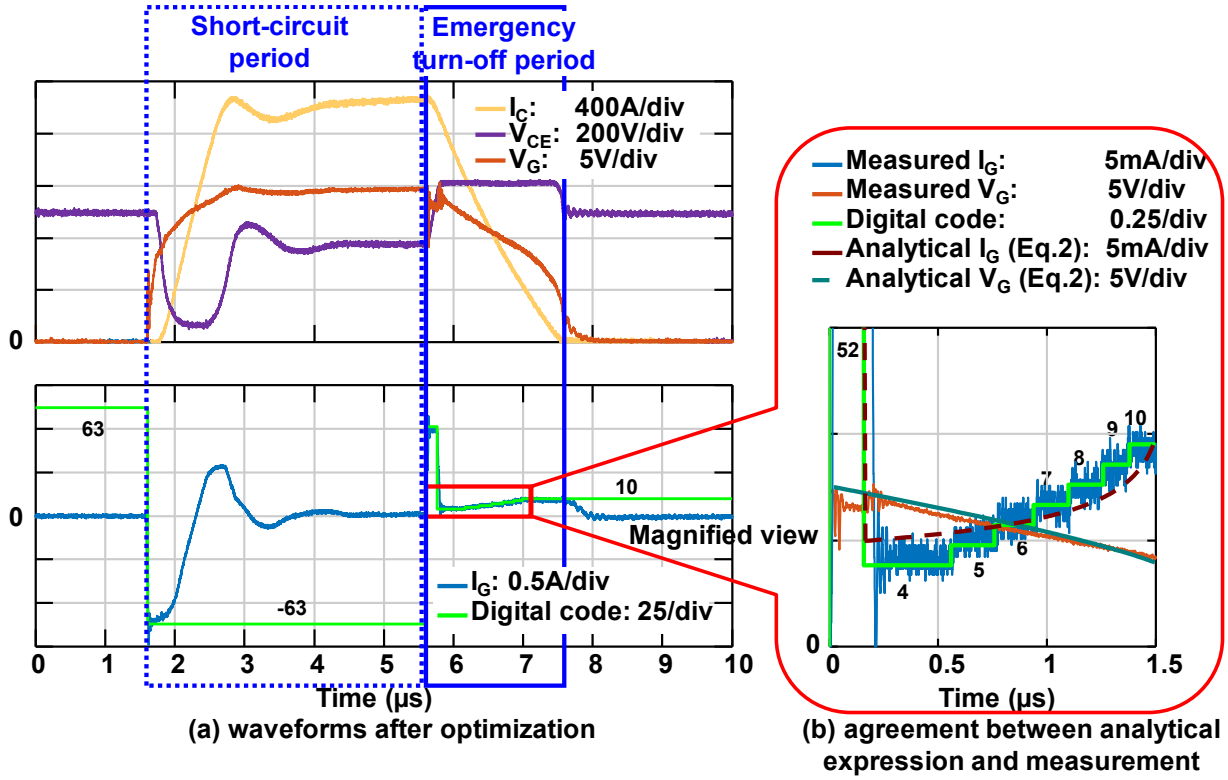


Fig. 7 Overall waveforms in optimized case using DGD corresponding to the case in Fig.4(c). Digital code means the number of turned-on MOS transistors (positive for NMOS and negative for PMOS). Numbers in the figure signify digital code in DGD.

IV. Measurement Results

E_{LOSS}, and V_{OV} can be calculated from the measured data. The experimental results are shown in Fig.6. Three kinds of gate drivers in Fig.1 are employed. V_{OV} is controlled to be within the allowable maximum, $V_{OV,MAX}$, set at 120V this time by tuning the resistor value in Fig. 6(a), by tuning the size of the driver MOSFET in Fig.6(b), and by manually tuning the current waveform through dynamically changing the number of turned-on MOSFETs in Fig. 6(c).

The DGD shows the energy loss 22% less than that for resistor drive and 28% less than MOSFET drive while keeping the peak $V_{OV,MAX}$ around 120V. The optimum gate drive by using DGD is to drive down V_G very strongly first as shown in Fig.6(c). When V_{OV} approaches the allowable maximum, the gate current is reduced to a low level and then is increased gradually to keep V_{OV} at $V_{OV,MAX}$ as shown in the upper-right corner in Fig.6.

Fig. 7 shows the overall measured waveforms in the optimized case using DGD. In Fig.7(b), the calculation results using Eq.2 are also overlaid on the experimental results. It is seen that the theory well explains the measurement results. In practice, the optimum waveform, that is, the digital code pattern for DGD for the emergency turn-off should be provided before the short circuit occurs. This can be done by using theoretical calculation and experiments using the device under consideration in the development phase of a system. Although there are variations in parameters, the worst case occurs when V_{CC} is maximum, temperature is maximum and the V_{TH} is minimum. The optimized drive waveform has nothing to do with the collector current in the normal operation. Thus, assuming the worst case condition, the unique optimized waveform can be obtained, which means that this approach is practically executable.

V. Conclusions

The optimum gate drive waveform during the emergency turn-off of IGBT is analyzed and experimentally verified by using Digital Gate Drive. 22% energy loss saving can be achieved over the conventional resistor drive, which in turn reduces 22% temperature increase of the IGBT, leading to the safer turn off. The optimum gate control is to drive down V_G strongly first followed by a sudden fall of gate current and then to gradually increase the gate current. The optimized I_G waveform for the emergency turn-off is different from that for the normal turn off in that much more precise control in the gradual increase period is needed in the turn-off since the V_{CE} overshoot peak cutoff is critically important.

The theoretical base for this gradual control is established for the first time. In the modeling of IGBT, the collector current of IGBT in the active region is found to follow the alpha-power law, not the conventional square-law. The optimum control method can be applicable to other types of power devices such as power MOS devices, since the I-V characteristic in power MOS devices can also modeled by alpha-power law.

This type of technology becomes increasingly important

as the IGBT current density increases and the temperature rise issue gets severer. In the future, when DGD is used in a normal switching of power devices, the same DGD can be used in the case of emergency turn-off for free.

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