A 0.90–4.39-V Detection Voltage Range, 56-Level Programmable Voltage Detector Using Fine Voltage-Step Subtraction for Battery Management

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***Abstract*— A programmable voltage detector (PVD) for battery management is proposed to achieve the programmability of the detection voltage (V_{DETECT}). Thanks to the programmability, users can set an appropriate V_{DETECT} for battery management considering the operating voltage of the battery. For batteries including Li-ion and NiMH batteries, a PVD is required to achieve wide programmed V_{DETECT} range from 1.0 to 4.35 V with a fine voltage step of ±42 mV. Furthermore, the power consumption of the PVD must be minimized since the PVD is always operating in battery management. To achieve both the target programmability of V_{DETECT} and the low power consumption of the PVD, a programmable voltage reference (PVREF) using a fine voltage-step subtraction (FVS) method is proposed. The FVS is a combination of fine and coarse programming for the output of the PVREF, which achieves a fine voltage step and a wide programmable range of V_{DETECT} achieving both a low temperature coefficient of V_{DETECT} and low power consumption of the PVD. The measurement results of the PVD fabricated in a 250-nm CMOS process show a current consumption of the PVD of 1.2 nA at 3.5 V and a temperature coefficient of V_{DETECT} of 0.28 mV/°C. The PVD enables the widest programmable range of V_{DETECT} from 0.90 to 4.39 V, fine V_{DETECT} resolution of ±31.5 mV, and 56-level linear, monotonic programmability of V_{DETECT}.**

***Index Terms*— Voltage detector, programmable voltage detector, voltage reference, programmable voltage reference, low power.**

I. Introduction

THE Internet of Things (IoT) is expected to enhance the quality of our lives by using information gathered from IoT sensor nodes. In an IoT sensor node, a voltage detector (VD) is one of the key circuits for battery management. As shown in Fig. 1, the VD is connected to a battery to monitor its terminal voltage (V_{BAT}) and prevent the battery from being damaged by overcharge or overdischarge. Since the VD is always on, the low-power operation of the VD is indispensable to an energy-limited IoT node. A challenge of the VDs for battery management is to improve the accuracy of the detection voltage (V_{DETECT}) since the lifetime of the battery is sensitive to its charging voltage. For example, the battery management of lithium-ion batteries (LiBs) requires the precise control of V_{DETECT} with inaccuracy of less than ±1 % of the charge voltage (= ±42 mV) to maximize their performance [1]. Another challenge for the VDs is to achieve the programmability of V_{DETECT}. Since the operating voltages vary among batteries (e.g., 3.0 to 4.35 V [2], [3], 1.0 to 1.5 V [4], 1.8 to 2.7 V [5], and 2.0 to 3.3 V [6]), an appropriate V_{DETECT} must be set for the operating voltage of the battery. Recently, many low-power VDs have been proposed [7]–[10] and made commercially available [11]–[13]. However, their V_{DETECT} for the VDs are fixed at certain voltages. As a result, VDs require special factory trimming to tune V_{DETECT} to meet the user requirements, increasing the cost and delivery time. Although V_{DETECT} of VDs in a battery management IC [14] can be programmed using external resistors, the method increases the cost and area because several bulky resistors are required for the programming. Furthermore, resistor-based programming is not suitable for the sub-10 nA operation of VDs because the resistance exceeds 100 MΩ. In [15], a 248 pW programmable VD that can program V_{DETECT} to mitigate the effect of process variation is presented although the range of the programmed V_{DETECT} is only from 0.52 to 0.85 V, making it unsuitable for the use in battery management.

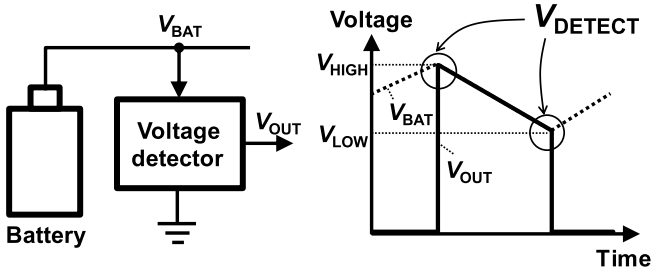

Fig. 1. Voltage detector for battery management.

In this work, an ultra-low-power programmable VD (PVD) is newly presented that allows users to program V_{DETECT}

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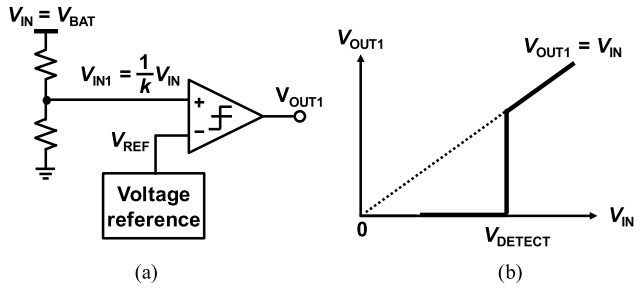


Fig. 2. (a) Circuit schematic of a typical VD and (b) its input-output characteristics.

freely in accordance with a battery in an IoT node. Although the PVD in [16] does not cover the target V_{DETECT} range of 1.0 to 4.35 V which is determined based on the operating voltages of the batteries [2]–[6], the PVD in this work shows a programming range of 0.90V to 4.39 achieving the resolution of the programmed V_{DETECT} of ±31.5 mV that is less than ±1 % of the typical charge voltage of a LiB (= ±42 mV). The PVD in this work is more suitable for various types of battery management than [16].

This paper is organized as follows. In Section II, conventional PVDs are described with emphasis on the problems with their programmability. In Section III, an overview of the proposed PVD is introduced. Section IV shows measurement results of the proposed PVD fabricated in a 250-nm CMOS process. Section V concludes this paper.

II. Conventional Programmable Voltage Detector

Fig. 2 (a) and (b) show a circuit schematic of a typical VD and the input-output characteristics, respectively. The VD comprises a voltage reference that generates a constant standard voltage (V_{REF}), a voltage divider composed of resistors, and a comparator. In the schematic, some additional circuits such as a feedback circuit to add some hysteresis to V_{DETECT}, and a delay cell to ensure that the VD is stabilized before the load system starts their operation, are removed to simplify the discussion. When V_{IN}(= V_{BAT} in Fig. 1) is lower than a predefined voltage (V_{DETECT}), the output voltage of the VD (V_{OUT1}) is 0 V. When V_{IN} exceeds V_{DETECT}, V_{OUT1} changes into the voltage level of V_{IN}. In the circuit topology, V_{DETECT} is described as

$$V_{DETECT} = kV_{REF}, \tag{1}$$

where $1/k$ (<1) is the division ratio of the voltage divider. One simple way to attain the programmability of V_{DETECT} is to incorporate the programmability of V_{REF} as shown in Fig. 3 (a). A resistive ladder and a selector are added to enable the programmable V_{DETECT}. The method achieves linear V_{DETECT} programmability and fine programmed V_{DETECT} steps by increasing m. However, the TC of V_{DETECT} deteriorates as m increases owing to the temperature dependence of V_{REF1} originating from the voltage drop at the input of the MUX ($V_1^{'}$, $V_2^{'}$, …$V_m^{'}$). The voltage drop is caused by the leakage currents of the transistor switches [17] in the MUX

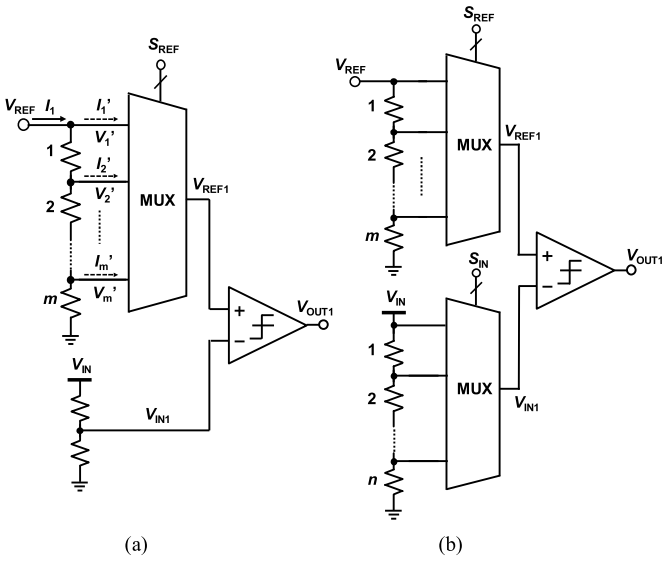


Fig. 3. Concept of the programming of V_{DETECT}. (a) Typical implementation to achieve the programmability of V_{DETECT}. (b) Implementation proposed in [15].

($I_1^{'}$,$I_2^{'}$, …$I_m^{'}$). Since the leakage current is a strong function of the temperature, the voltage drop becomes temperature-dependent that increases the TC of V_{DETECT}. The TC of V_{DETECT} is determined by the ratio of I_1 to the amount of leakage currents in the MUX I_{SUM}(= $I_1' + I_2' + \ldots + I_m$'). Fig. 4 shows the simulated m dependence of the TC of V_{DETECT} in the PVD shown in Fig. 3 (a) when $V_{REF} = 0.5$ V and $I_1 = 200$ pA. Due to the increase in the leakage current of the MUX, the TC of V_{DETECT} exceeds 0.6 mV/°C when $m = 32$, which results in a ±18 mV error of V_{DETECT} in the typical battery operating temperature range of 0 to 60 °C. This result indicates a tradeoff relation between the resolution of the programmed V_{DETECT} and the TC of V_{DETECT}. One way to solve the tradeoff is to increase I_1 so that I_{SUM} become negligible, although it increases the power consumption of the PVD. The concept of the PVD proposed in [15] is shown in Fig. 3 (b). By adding the programmability into both V_{REF1} and V_{IN1}, the resolution of the programmed V_{DETECT} is improved. On the other hand, the conventional PVD [15] does not achieve linear V_{DETECT} programmability. Fig. 5 shows the operation principle of the conventional PVD [15]. The offset of V_{REF1} is varied by changing m and the gradient of V_{IN1} is varied by changing n. Points at the intersection of V_{REF1} and V_{IN1} voltages are the obtained programmed voltages of V_{DETECT}. As shown in Fig. 5, V_{DETECT} changes nonlinearly and non-monotonically with the number of control bits. Furthermore, some points overlap, which reduces the number of the programmed voltages and resolution of V_{DETECT}. As the same way to the PVD shown in Fig. 3 (a), the resolution can be improved by increasing m and n at the cost of the TC of V_{DETECT} or the power consumption of the PVD. As described so far, the programming methods shown in Fig. 3 (a) and (b) have the tradeoff relationship between the resolution and TC of programmed V_{DETECT}. The only way to solve the problem is to increase the power consumption of the PVD. In the next

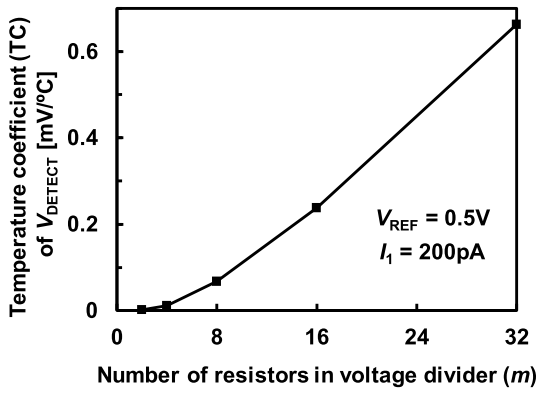


Fig. 4. Simulated m dependence of the TC of V_{DETECT} in the PVD in Fig. 3 (a).

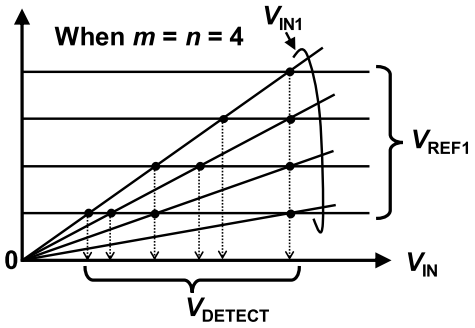


Fig. 5. Operation principle of the conventional PVD [15].

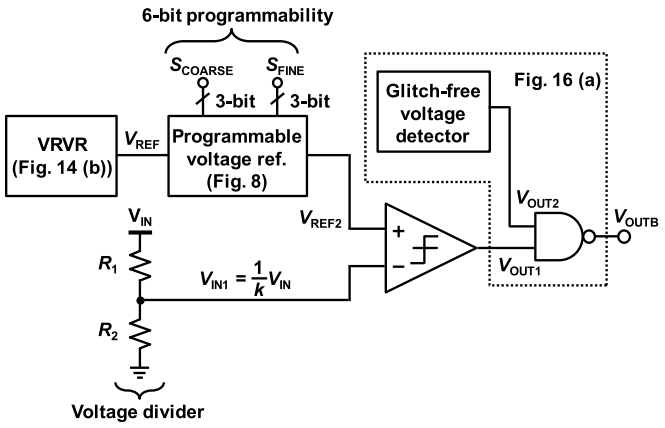


Fig. 6. Block diagram of the proposed PVD.

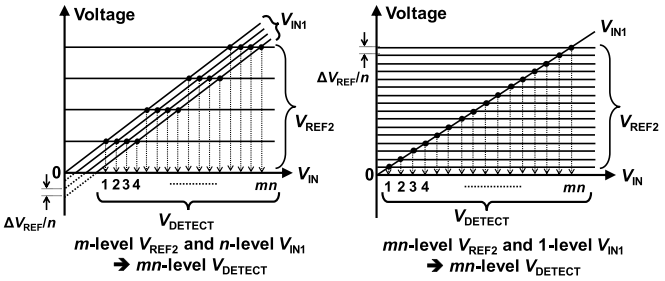


Fig. 7. Concept of the programmability of the PVD. (a) PVD in [16]. (b) PVD in this work.

section, the way to solve the tradeoff without increasing the power consumption of the PVD is proposed.

III. Proposed Programmable Voltage Detector

Fig. 6 shows a block diagram of the proposed PVD. The proposed PVD solves the tradeoff described in Section II by utilizing the proposed programmable voltage reference (PVREF) that supplies a programmed reference voltage V_{REF2}. By applying proper digital codes into S_{COARSE} and S_{FINE}, users can program V_{REF2}, which leads the programmability of V_{DETECT}. The PVREF achieves both low-power operation (= 0.63 nA) and a low TC of V_{REF2} (= 21 μV/°C) while enabling the fine voltage-step programmability of V_{REF2} thanks to the proposed fine-voltage-step subtraction (FVS) method. As a voltage reference, a V_{DD}-regulated voltage reference (VRVR) is also newly proposed in Fig. 6. The VRVR improves the linearity of the programmed V_{DETECT} in the PVD by reducing the supply voltage (= V_{IN}) sensitivity of V_{REF}. The voltage divider composed of R_1 and R_2 is implemented with stacked diode-connected pMOSFETs. The current of the voltage divider is reduced to sub-100 pA, which is negligible compared with the total current of the PVD. The proposed PVREF is inserted between the VRVR and the comparator. The PVD shown in Fig. 6 includes a glitch-free, short-circuit-current-free output stage. The proposed output stage removes a glitch in V_{OUTB} [15] even though V_{IN} is as low as 0 V. The glitch-free operation is indispensable for the PVD applied to a system where V_{IN} drops to near 0 V such as battery management for energy harvesting [18]–[22]. In addition, short-circuit-current is also reduced in the output stage. During a transition of V_{OUT1}, there is a period when both pull-up pMOSFET and pull-down nMOSFET conduct a current in the NAND gate in Fig. 6. The energy loss caused by large short-circuit-current is critical for the battery management since the transition of V_{IN} is relatively slow that the short-circuit-current flows from V_{IN} to GND for a long time. The proposed output stage reduces the short-circuit-current in the output stage to save the energy in the battery.

Figs. 7 (a) and (b) show the concept of the programmability of the PVDs in [16] and in this work. In [16], m-level V_{REF2} and n-level V_{IN1} achieves mn-level programmable V_{DETECT} while mn-level V_{REF2} and 1-level V_{IN1} achieves mn-level programmable V_{DETECT} in Fig. 6. Both topologies achieve mn-level V_{DETECT} with almost identical characteristics. On the other hand, the programming concept in Fig. 7 (b) is selected in this work because we expect the PVREF used in this work can be applied to various circuits as well as the PVD. Therefore, the analysis and the measured results of the proposed PVREF are also described in detail in this work.

A. Programmable Voltage Reference Using Fine Voltage-Step Subtraction Method

Users can program V_{DETECT} in the PVD shown in Fig. 6 by programming the output of the PVREF (V_{REF2}) with suitable digital codes for S_{COARSE} and S_{FINE}. The proposed PVD using

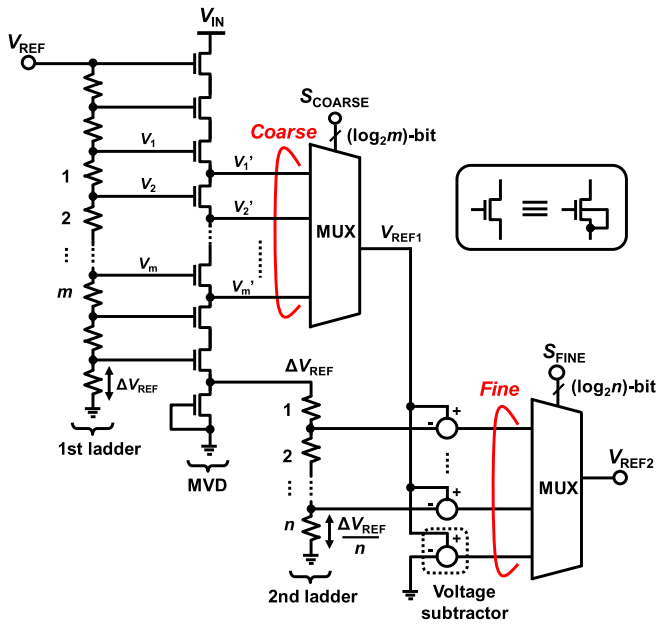


Fig. 8. Circuit schematic of the proposed PVREF with the fine voltage-step subtraction (FVS) method.

the PVREF achieves both fine-resolution programming and a low TC of V_{DETECT} at the same time while covering the target V_{DETECT} range of 1.0 to 4.35 V with the current consumption of 1.2 nA. As shown in Section II, a large number of transistor switches for a MUX increases the TC of the output voltage of the PVREF and V_{DETECT}. The proposed FVS method in the PVREF reduces the number of the transistor switches for a MUX while maintaining the fine resolution of the programmed V_{REF2}. The reduction of the number of the switches for each MUX leads to a lower TC of V_{DETECT} without increasing the power consumption.

Fig. 8 shows the circuit schematic of the proposed PVREF using the FVS method. The circuit implementation of the resistors for the voltage dividers, the MUXs, and the comparator is similar to that in [15]. The multiple voltage duplicator (MVD) works as a multiple-input and multiple-output voltage buffer that copies each input voltage to each output node as $V_1 = V_1$', $V_2 = V_2', \ldots, V_m = V_m$' reducing the current consumption of the voltage reference preceding the PVREF [15]. The FVS method used in the PVREF is a combination of coarse and fine programming of V_{REF2} that results in a fine-step, monotonically programmed V_{REF2}. In Fig. 8, ΔV_{REF} is the coarse voltage-step and $\Delta V_{REF}/n$ is the fine voltage-step for the programming. In the FVS, the fine V_{REF2} steps are achieved by subtracting the fine voltage-steps of $\Delta V_{REF}/n$ from the coarsely varied V_{REF1}. Linear and monotonic V_{REF2} programmability is achieved because the fine voltage-step is generated from the coarse voltage step. An equation for V_{REF2} is derived below.

$$\Delta V_{REF} = \frac{V_{REF}}{m+4} \tag{2}$$

$$V_{REF1} = \frac{i+2}{m+4} V_{REF} \ (i = 1, \ldots, m) \tag{3}$$

$$V_{REF2} = V_{REF1} - \frac{j}{n} \Delta V_{REF} \ (j = 0, 1, \ldots, n-1) \tag{4}$$

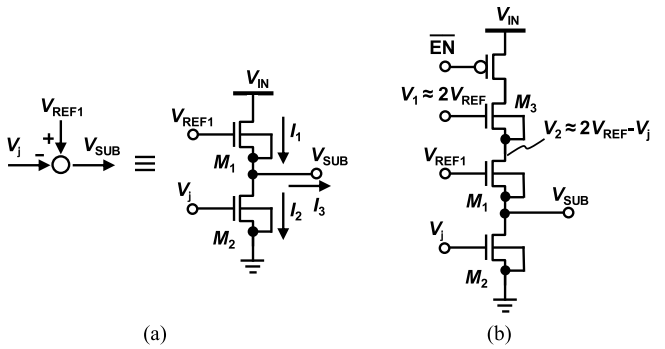


Fig. 9. (a) Operation principle and (b) schematic of the proposed voltage subtractor.

Substituting (2) into (4),

$$V_{REF2} = V_{REF1} - \frac{j}{(m+4)n} V_{REF} \tag{5}$$

Substituting (3) into (5)

$$V_{REF2} = \frac{1}{m+4}\left(i + 2 - \frac{j}{n}\right) V_{REF} \tag{6}$$

As shown in (6), by subtracting the fine voltage-step of $V_{REF}/(m+4)n$ from the coarse voltage step of $V_{REF}/(m+4)$, both linear V_{REF2} programmability and fine V_{REF2} steps are achieved. The programmability of V_{REF2} enables the PVD shown in Fig. 6 to have linear and monotonic programmability of V_{DETECT} as follows:

$$V_{DETECT} = k\frac{1}{m+4}\left(i + 2 - \frac{j}{n}\right) V_{REF}. \tag{7}$$

In our design, k, m, and n are determined to be 12, 8, and 8, respectively, to achieve 6-bit programmability of V_{DETECT}. The conventional PVD shown in Fig. 3 (a) requires 2^6 transistors for the MUX to achieve the 6-bit programmability of V_{DETECT} while the proposed PVD requires 2^3 transistors for each MUX. The reduction of the transistor switches for the MUX improves the TC of V_{DETECT} without increasing the power consumption.

In the FVS, the low-power voltage subtractors are the key building blocks. Fig. 9 (a) shows the operation principle of the proposed voltage subtractor. M_1 and M_2 are the identical transistors operating in the subthreshold region and $I_3 = 0$ because the input impedance of the MUX is sufficiently large. When the drain-to-source voltages of M_1 and M_2 are over $3V_T$, the gate-to-source voltages of M_1 and M_2 becomes V_j since $I_1 = I_2$. Then, $V_{SUB} = V_{REF1} - V_j$ and the voltage subtraction is achieved. A problem with the subtractor shown in Fig. 9 (a) is, however, that the result of the subtraction is dependent on V_{IN}. Since the drain node of M_1 is directly connected to V_{IN}, M_1 suffers from the drain-induced barrier lowering (DIBL) effect. Therefore, the threshold voltage of M_1 changes with V_{IN}, which results in the V_{IN}-dependence of the subtraction results. Fig. 9 (b) shows a circuit schematic of the proposed voltage subtractor. The concept of the voltage subtraction is based on Fig. 9 (a). Compared with the subtractor shown in Fig. 9 (a), M_3 is added to the drain node of M_2 (V_2) to keep V_2 constant regardless of V_{IN}. M_3 works as a voltage regulator

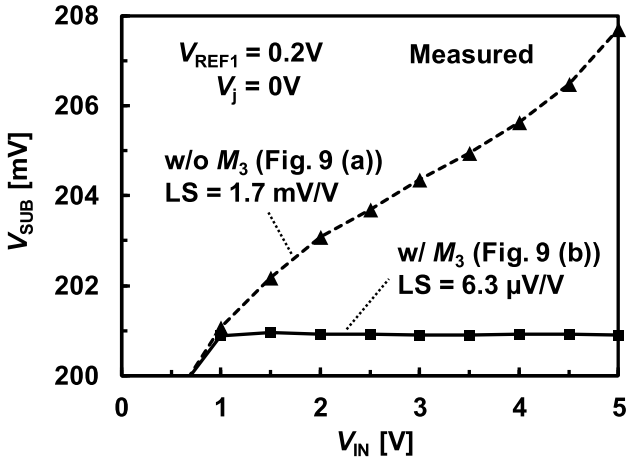


Fig. 10. Output of the voltage subtractors when $V_{REF1} = 0.2$ V, $V_j = 0$ V.

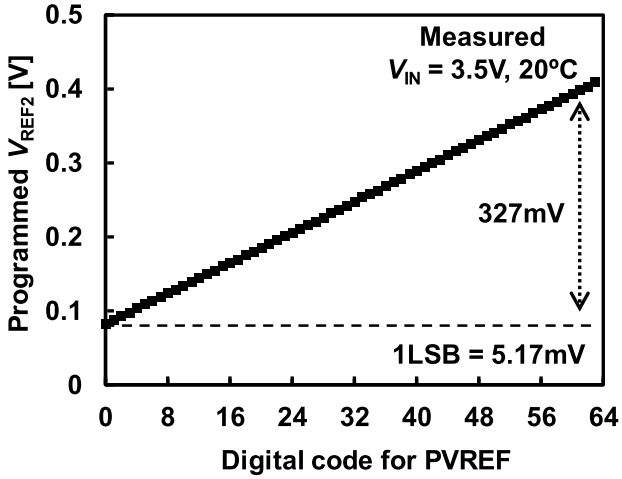


Fig. 11. Measured V_{REF2} dependence on the digital code of the PVD.

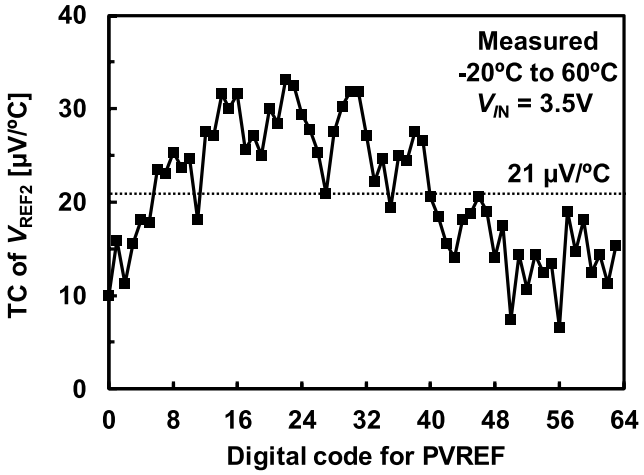


Fig. 12. Measured TC of the programmed V_{REF2}.

and regulates V_2 to $V_1 - V_j$. $2V_{REF}$ for V_1 is obtained from the proposed VRVR shown later in Fig. 14 (b). The regulation technique makes V_2 less sensitive to V_{IN} and removes the V_{IN} dependence of the subtraction result. Furthermore, a power gating switch is added to turn off the non-selected voltage subtractors. Fig. 10 shows the output characteristics of the voltage subtractors shown in Figs. 9 fabricated in a 250-nm CMOS process when $V_{REF1} = 0.2$ V and $V_j = 0$ V. To verify the efficacy of M_3 shown in Fig. 9 (b) in reducing the line sensitivity (LS) of the subtraction result, the subtractor without M_3 shown in Fig. 9 (a) is also implemented and measured as well as the subtractor shown in Fig. 9 (b) under the same conditions. The measured LS of the subtractors shown in Fig. 9 (a) and (b) are 1.7 mV/V and 0.006 mV/V, respectively. Thanks to M_3, the LS of the subtractor becomes sufficiently small not to affect the linearity of the proposed PVREF. The proposed voltage subtractor is designed to have a current of 0.2 nA at 20 °C.

The proposed PVREF shown in Fig. 8 is fabricated in a 250-nm CMOS process and verified by measurements with V_{REF} of 500 mV supplied by a voltage source, externally. The ideal V_{REF} makes it possible to evaluate the pure performance of the PVREF regardless of the characteristics of V_{REF}. The proposed PVREF achieves 631 pA operation at 3.5 V supply voltage as described later in Fig. 21. Fig. 11 shows the programmed V_{REF2} when V_{IN} and the temperature are 3.5 V and 20 °C, respectively. The acquired 6-bit V_{REF2} is ranging from 83 to 409 mV, in steps of 5.17 mV. The measured programmed V_{REF2} is in good agreement with theoretical programmed V_{REF2} ranging from 83 to 411 mV in steps of 5.21 mV, within a V_{DETECT} offset of 2 mV and a step error of 0.04 mV. The measured current consumption is 631 pA at 3.5 V, and the TC of the programmed V_{REF2} is 21 μ V/°C as shown in Fig. 12. The measurement results show that the PVREF achieves both 631 pA low-power operation and a low TC of the programmed V_{REF2}, enabling the 6-bit programmability of V_{REF2} which contributes to the linear and monotonic programmability of V_{DETECT} with the fine voltage steps in the proposed PVD.

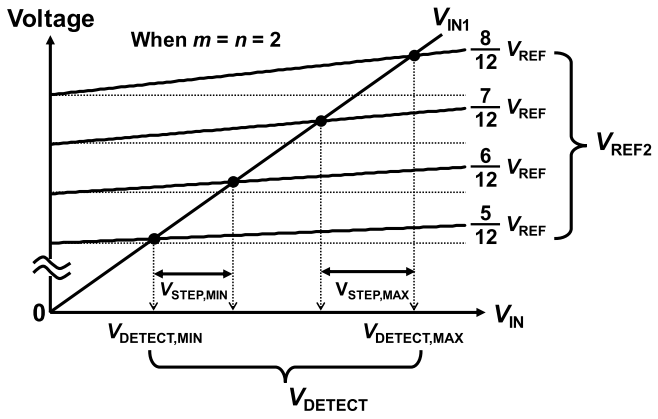


Fig. 13. Operation principle of the proposed PVD when V_{REF} includes V_{DD} dependence.

B. V_{DD}-Regulated Voltage Reference (VRVR)

The LS of V_{REF} in the PVD shown in Fig. 6 affects the linearity of the programmed V_{DETECT}. Fig. 13 shows the operation principle of the proposed PVD when the PVREF with $m = n = 2$ in Fig. 8 is applied. The points where

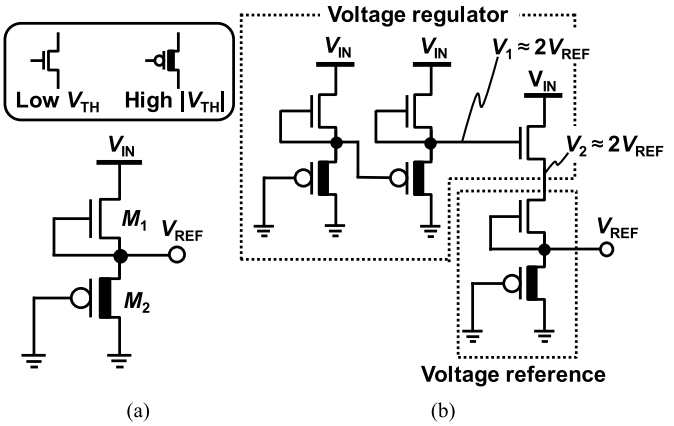


Fig. 14. (a) Conventional voltage reference based on [23]. (b) Proposed V_{DD}-regulated voltage reference (VRVR).

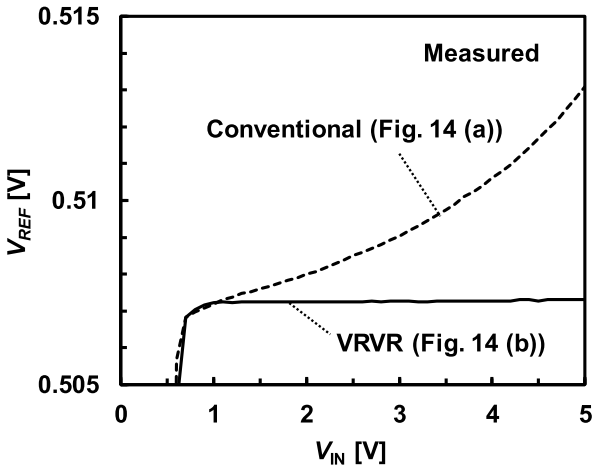


Fig. 15. Measured V_{IN} dependence of V_{REF}.

V_{IN1} and V_{REF2} intersect are the obtained programmed value of V_{DETECT}. Fig. 13 shows that the LS of V_{REF} causes an increase in the step size of the programmed V_{DETECT} (V_{STEP}). The step variation causes the nonlinearity of the programmed V_{DETECT}. Assuming that V_{REF} is expressed as $V_{REF,R}+\alpha(V_{IN}-V_{IN,R})$, where $V_{REF,R}$ is V_{REF} at a reference $V_{IN}(=V_{IN,R})$, α is the LS of the voltage reference ($=\Delta V_{REF}/\Delta V_{IN}$), and $V_{IN,R} = V_{DETECT,MIN}$ in Fig. 13, $V_{STEP,MIN}$ and $V_{STEP,MAX}$ are expressed as

$$V_{STEP,MIN} \approx k\frac{1}{(m+4)n}V_{REF,R} \tag{8}$$

$$V_{STEP,MAX} \approx k\frac{1}{(m+4)n}\left(V_{REF,R}+\alpha\Delta V_{IN}\right) \tag{9}$$

where $\Delta V_{IN} = V_{DETECT,MAX}-V_{DETECT,MIN}$. From (8) and (9), the largest step difference ($V_{STEP,MAX}$), defined as $V_{STEP,MAX}-V_{STEP,MIN}$, is expressed as

$$\Delta V_{STEP} \approx k\frac{1}{(m+4)n}\alpha\Delta V_{IN}. \tag{10}$$

As mentioned previously, $m = n = 8$ and $k = 12$ in our design. Assuming that $V_{DETECT,MAX} = 4.35$ V and $V_{DETECT,MIN} = 1$ V considering the target V_{DETECT}, $\Delta V_{IN} \approx 3.4$ V. As shown later in Fig. 15, our VRVR supplies V_{REF} of about 500 mV. Under the condition of $V_{REF,R} = 500$ mV, $V_{STEP,MIN}$ is calculated to 62.5 mV from (8). When ΔV_{STEP} is required to be less than 0.1 % of $V_{STEP,MIN}(=0.06$ mV) to prevent the step error from reducing the linearity of the programmed V_{DETECT}, α must be less than 140 μV/V. In this work, a VRVR with the LS of 37 μV/V and the current consumption of 300 pA is proposed. Figs. 14 (a) and (b) show circuit schematics of a conventional 2-transistor voltage reference circuit based on [23] and the proposed VRVR, respectively. In Fig. 14 (a), V_{REF} is determined by the threshold voltages of M_1 and M_2 as

$$V_{REF} = (|V_{THP}| - \frac{m_p}{m_n}V_{THN}) - m_p V_T \ln\left(\frac{\mu_p C_{OXP} W_2 L_1}{\mu_n C_{OXN} W_1 L_2}\right) \tag{11}$$

where m_n (m_p), V_{THN} (V_{THP}), and μ_n (μ_p) are the body-effect coefficient, the threshold voltage, and the mobility of the nMOSFET (pMOSFET), respectively. V_T is the thermal voltage ($= k_B T/q$), k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. W_1 (W_2) and L_1 (L_2) are the gate width and length of each transistor, respectively, and C_{OXN} (C_{OXP}) is the gate capacitance of each transistor. The first and second terms in (11) have the opposite temperature dependences. By taking a suitable ratio of M_1 to M_2, the temperature dependences of the first and second terms cancel each other. Ideally, V_{REF} shown in Fig. 14 (a) is temperature/V_{IN}-independent with the appropriate transistor size ratio of M_1 to M_2. On the other hand, M_1 suffers from the DIBL effect, that is, V_{TH1} decreases as V_{IN} ($=V_{IN}$ in Fig. 6) increases, which deteriorates the LS of the voltage reference shown in Fig. 14 (a). In the proposed VRVR shown in Fig. 14 (b), a V_{IN} regulator is added to the 2-transistor voltage reference to improve the LS of V_{REF}. The power overhead of the regulator is 10 % in the total power consumption of the VRVR. In the VRVR, $V_1 = V_2 \approx 2V_{REF}$, which shows that V_2 is regulated to be a constant voltage. Assuming that the LS of V_{REF} is α (< 0.01) in Fig. 14 (a), ΔV_2 / ΔV_{IN} is 2α in the VRVR, which reduces the LS of V_{REF} to $2\alpha^2$. Fig. 15 shows the measured V_{IN} dependence of the conventional voltage reference shown in Fig. 14 (a) and the proposed VRVR fabricated in a 250-nm CMOS process. The proposed VRVR achieves the LS of 37 μV/V ($=0.007$ %/V), whereas the LS of the voltage reference shown in Fig. 14 (a) is 1.5 mV/V ($=0.3$ %/V). The VRVR improves the LS of the voltage reference dramatically and achieves the target LS of 140 μV/V. The simulated PSRR of the VRVR is -83 dB at 100 Hz, which shows that the VRVR has a noise-tolerant performance against V_{IN} noise. The measured TC of the VRVR in the temperature range of -20 to 160 °C is 33.6 μV/°C ($=63$ ppm/°C) which is sufficiently low TC compared with the other Sub-1nA CMOS voltage references (e.g., 62 ppm/°C [23], 64 ppm/°C [24] and 252 ppm/°C [25]). The measured power consumption is sufficiently small value of 300 pA. The measurement results show that the VRVR achieves both low-power and V_{IN}-independent operation while maintaining the temperature-independent characteristics.

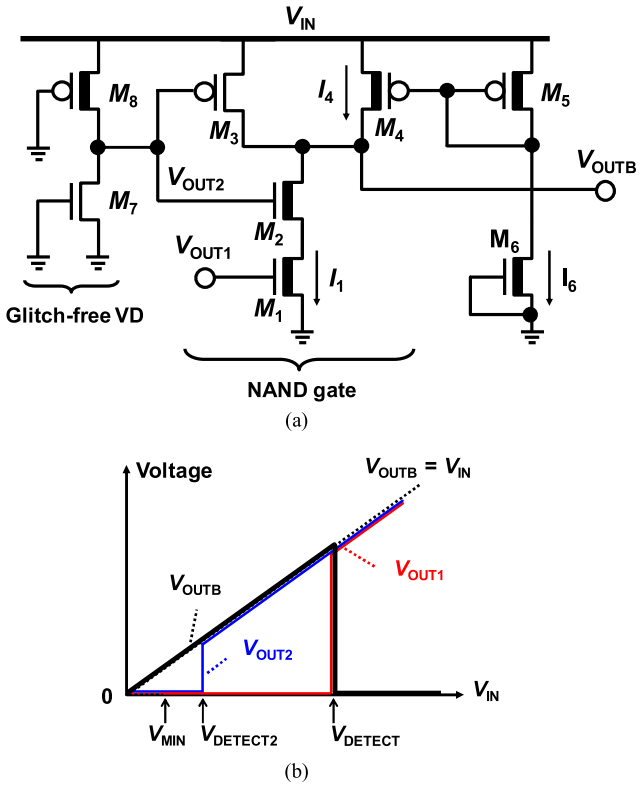


Fig. 16. (a) Circuit schematic of the output stage in the PVD including glitch-free VD and NAND gate and (b) their voltage characteristics.

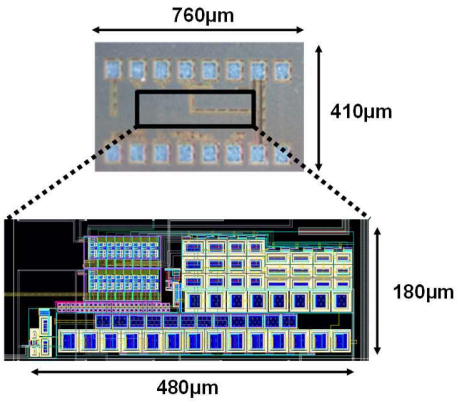


Fig. 17. Die photograph and a layout of the proposed PVD.

C. Glitch-Free and Short-Circuit-Current-Free Output Stage

Fig. 16 (a) and (b) show the circuit schematic of the output stage in the PVD shown in Fig. 6 and the characteristics of each node. The output stage realizes glitch-free and short-circuit-current-free operation. The glitch is due to the unknown states of the comparator, the voltage reference, and the output buffer in the PVD when V_{IN} is near 0 V. Typically, the minimum V_{IN} (e.g., 0.8 to 1 V) is specified in commercially available VDs [11]–[13] where the VDs operate properly. Glitch-free operation is indispensable for the PVD when it is applied to the battery management for energy harvesting since a glitch in the output of the PVD adversely affects the

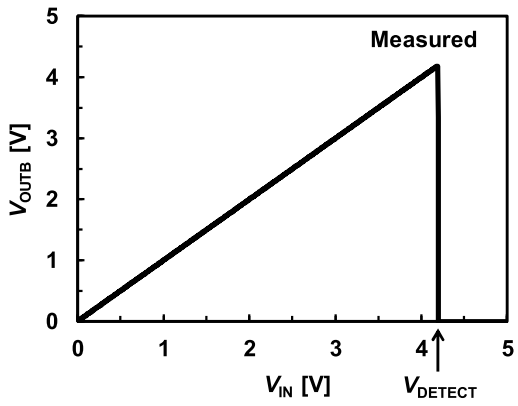


Fig. 18. Measured input and output characteristics of the PVD. V_{DETECT} is set to 4.2 V.

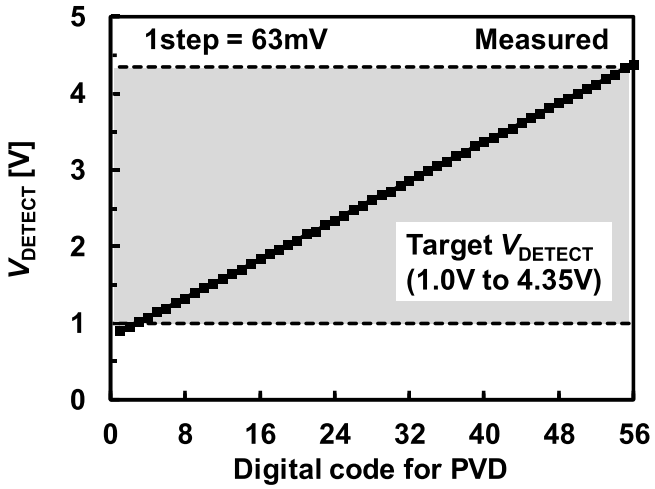


Fig. 19. Measured V_{DETECT} dependence on the digital code of the PVD.

energy harvesting [15]. In the proposed PVD, the glitch-free programmable operation is achieved by the combination of the PVD and a glitch-free VD based on the concept shown in [15]. In addition, short-circuit-current-free operation is achieved to reduce the energy loss of the battery. The short-circuit-current occurs when a typical CMOS NAND gate is applied to the PVD in Fig. 6. When V_{IN} is close to V_{DETECT}, neither the pull-up pMOSFETs nor the pull-down nMOSFETs are turned off completely in the NAND gate and a short-circuit current flows from V_{IN} to GND. Since the transition of the battery voltage is relatively slow, the short-circuit-current flows for a while, which causes additional energy loss. The proposed NAND stage with a glitch-free VD shown in Fig. 16 (a) achieves both the glitch-free and short-circuit-current-free operation. In Fig. 16 (a), M_7 and M_8 work as a glitch-free VD. $V_{DETECT2}$ is expressed as

$$V_{DETECT2} = |V_{THP}| - \frac{m_p}{m_n} V_{THN} - m_p V_T \ln\left(\frac{\mu_p C_{OXP} W_8 L_7}{\mu_n C_{OXN} W_7 L_8}\right). \quad (12)$$

where W_7 (W_8) and L_7 (L_8) are the gate width and length of each transistor, respectively. $V_{DETECT2}$ becomes temperature-independent with the proper size ratio of W_8/L_8 to W_7/L_7.

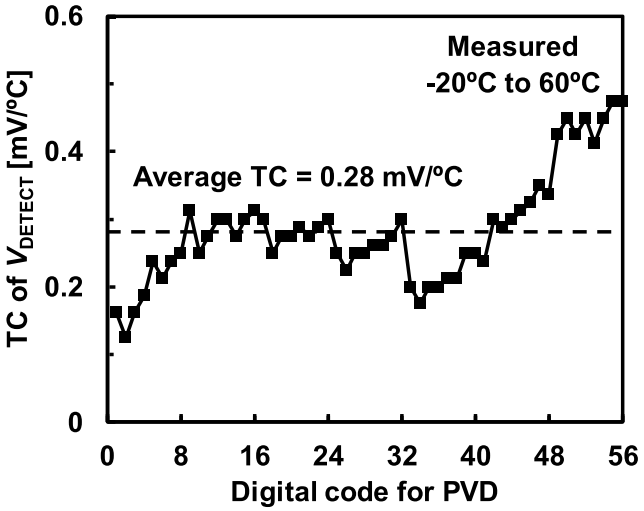


Fig. 20. Measured TC of V_{DETECT} for each digital code.

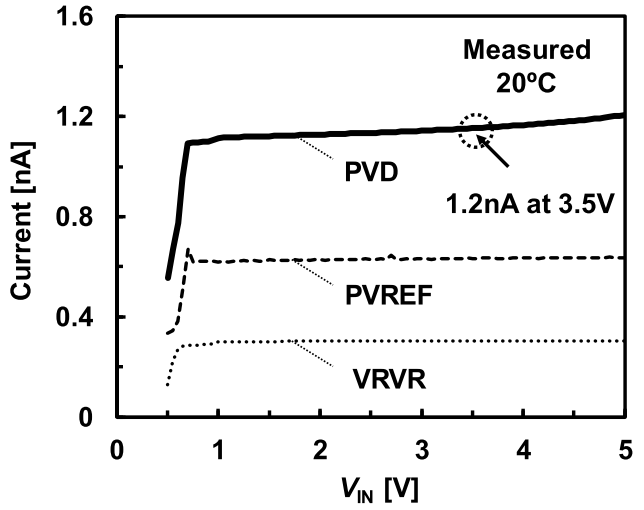
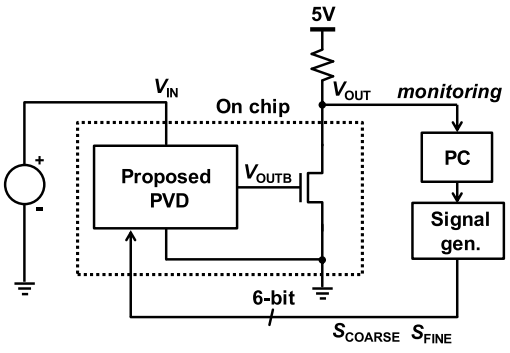
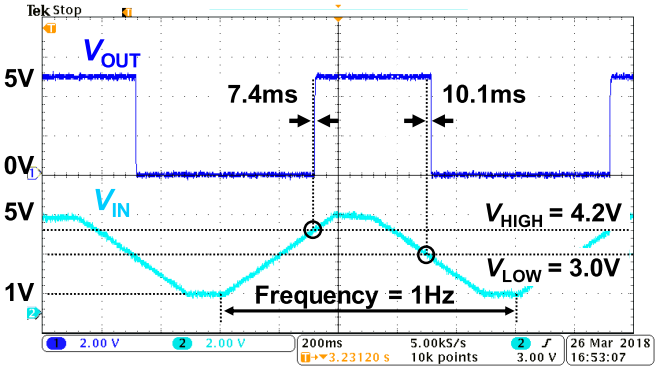


Fig. 21. Measured current of the entire PVD. Currents of the PVREF and the VRVR are also measured aside from the PVD.

In our design, $V_{DETECT2} \approx 500$ mV. When $V_{IN} < V_{DETECT2}$, V_{OUTB} is maintained at the voltage level of V_{IN} by the glitch-free voltage detector and the low V_{TH} pMOSFET M_3. When $V_{IN} > V_{DETECT2}$, M_3 and M_2 are turned off and turned on, respectively, and M_1 and M_4 comprise a common source amplifier working as an inverter. M_4 is a current source whose current (I_4) is similar to I_6. Thanks to the limited current of M_4, the short-circuit-current in the output stage is removed. In our design, $W_4/L_4 = W_5/L_5 = W_6/L_6$ and $W_6/L_6 : W_1/L_1 = 400 : 1$, which makes I_1 400 times lower than I_6 when $V_{OUT1} = 0$. I_4 maintains V_{OUTB} High when $V_{DETECT2} < V_{IN} < V_{DETECT}$. Assuming that the sub-threshold swing of the nMOSFET is 80 mV/dec, V_{OUT1} that invert V_{OUTB} from Low to High or High to Low is about 200 mV. Since the output stage always consumes I_6, I_6 is set to a sufficiently low current of 100 pA at room temperature to make the current consumption of the output stage negligibly low in the PVD.



(a)



(b)

Fig. 22. Response time of the PVD. (a) Block diagram of the test environment. (b) Measured waveform of the output node in the PVD.

IV. Measurement Results of Proposed Programmable Voltage Detector

In this section, measurement results of the proposed PVD fabricated in a 250-nm CMOS process are presented. Fig. 17 shows a chip photograph of the proposed PVD. The core area is 480 μm by 180 μm. Fig. 18 shows the measured input and output characteristics of the PVD when V_{DETECT} is set to 4.2V. The measurement result shows that the glitch is successfully removed from V_{OUTB}. Fig. 19 shows the programmed V_{DETECT} of the PVD. Although the PVD is designed to achieve the 6-bit programmability of V_{DETECT}, 56-level valid V_{DETECT} for covering the target V_{DETECT} range of 1.0 to 4.35 V are extracted. The programmed V_{DETECT} shown in Fig. 19 ranges from 902 to 4388 mV in steps of 63 mV, which covers the target V_{DETECT} range of 1.0 to 4.35V with steps of less than the target resolution of $\pm$42 mV. Fig. 20 shows the temperature coefficient of the programmed V_{DETECT}. The average TC of the 56-level programmed V_{DETECT} is competitive value of 0.28 mV/°C. To further increase the accuracy of battery charging, we can improve the resolution of the programmed V_{DETECT} or the TC of V_{DETECT} by increasing the power consumption of the PVD. Fig. 21 shows the power consumption of the entire PVD, the VRVR, and the PVREF at room temperature (20 °C). The power consumption of the entire PVD is 1.2 nA at 3.5 V including those of 0.3 nA and 0.63 nA for the VRVR and the PVREF, respectively. The PVD achieves the ultra-low power consumption with the reasonable TC of V_{DETECT} thanks to the proposed PVREF utilizing the FVS method and the

TABLE I
COMPARISON WITH PREVIOUS VOLTAGE DETECTORS

		TPS3839 [11]	AP4400A [13]	JSSC'16 [7]	ESSCIRC'15 [15]	A-SSCC'16 [16]	This work
CMOS process		N/A	N/A	180nm	250nm	250nm	250nm
Detection voltage	Programmability	No (factory trimming)	No (factory trimming)	No	Yes	Yes	Yes
	Max	4.38V	4.2V	3.58V (Fixed)	0.85V	4.67V	4.39V
	Min	0.9V	2.0V		0.52V	1.88V	0.90V
	Range	3.48V	2.2V		0.33V	2.79V	3.49V
	Number of Steps	9	23	1	21	56	56
	Uniform step	No	Yes (100mV step)		No	Yes (50mV step)	Yes (63mV step)
Power		150nA @1.2V (25°C)	20nA @3.4V (25°C)	79pA @3.6V (25°C)	248pA @1.0V (25°C)	3.7nA @3.5V (25°C)	1.2nA @3.5V (20°C)
TC of V_{DETECT}		0.055 mV/°C	0.75 mV/°C	1.5 mV/°C	0.11 mV/°C	0.17 mV/°C	0.28 mV/°C
Temperature range		-40°C to 85°C	-15°C to 85°C	0°C to 80°C	-20°C to 80°C	-20°C to 80°C	-20°C to 60°C

VRVR. The response time of the PVD is measured as shown in Figs. 22. Fig. 22 (a) shows the block diagram of the test equipment. In this measurement, the detection voltages for battery management, that is, V_{HIGH} and V_{LOW} shown in Fig. 1, are defined as 4.2 V and 3.0 V. A PC and a signal generator are used to define the V_{DETECT} of the PVD as a replacement of an MCU. A power source is used to reproduce a terminal voltage of the battery. We set the cycle time of the power source to 1 Hz with the V_{IN} slope (dV_{IN}/dt) of 10V/s. The slope is set to be faster than the charging speed of an RF energy harvesting system reported in [19] (= 2V/s). For the usage of the energy harvesting system, the PVD is required to respond sufficiently faster than those increase/decrease in V_{IN}. Fig. 22 (b) shows that the measured delays are 7.4 ms and 10.1 ms for the rise and fall edges of V_{OUT}, respectively. These time-lags causes the inaccuracy of 74mV/-101 mV in the supply voltage for the load system. If the higher accuracy of the input voltage for the system is required, the response time of the PVD must be reduced at the cost of the power consumption.

In Table I, this work is compared with the previously reported VDs. The proposed PVD enables the field programmability of the VD, allowing users to determine V_{DETECT} freely, making it suitable for the batteries and applications. The programmed V_{DETECT} covers the widest range from 902 to 4388 mV, covering the operating voltages of many types of battery. Compared with [16], the programming range of V_{DETECT} is improved to be more suitable for the operation voltages of various batteries. The step of the programmed V_{DETECT} is 63 mV, which is less than ±1 % of a typical charging voltage for a LiB (= ±42 mV). The measured TC of the programmed V_{DETECT} has a competitive value of 0.28 mV/°C.

V. Conclusions

In this work, a programmable voltage detector (PVD) fabricated in a 250-nm CMOS process that achieves the widest programmed detection voltage (V_{DETECT}) range of 0.90 to 4.39 V with a step voltage of 63 mV is newly presented. The programmability of the PVD enables users to program V_{DETECT} freely to set an appropriate V_{DETECT} for battery management considering the operating voltage of the battery. The proposed PVD achieves linear, monotonic voltage-step programmed V_{DETECT} and a low TC of 0.28 mV/°C at 1.2 nA current consumption when V_{IN} = 3.5 V thanks to the proposed programmable voltage reference using the fine voltage-step subtraction method.

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