# An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage

Teruki Someya, *Member, IEEE*, A. K. M. Mahfuzul Islam, *Member, IEEE*, Takayasu Sakurai, *Fellow, IEEE*, and Makoto Takamiya, *Senior Member, IEEE*

***Abstract*— A fully integrated CMOS temperature-to-digital converter utilizing MOSFETs in the sub-threshold region is proposed. The temperature-to-digital converter achieves the ultra-low power operation required for Internet of Things (IoT) nodes. The proposed principle takes the ratio of the sub-threshold currents of two nMOSFETs whose drain voltages are maintained well above and well below the thermal voltage, respectively. The proposed circuit implementation of the temperature-to-digital converter achieves ultra-low power consumption of 11 nW at room temperature of 25 °C. Measurement results of the proposed temperature sensor fabricated in a 180-nm CMOS process show −0.9/+1.2 °C peak-to-peak inaccuracy over a temperature range of −20 °C to 80 °C after a two-point calibration while achieving a resolution of 145 mK.**

***Index Terms*— Internet of Things (IoT), low power, sub-thermal drain voltage (STV), temperature sensor, temperature-to-digital converter.**

## I. Introduction

CMOS-COMPATIBLE smart temperature sensors that can be integrated into a system-on-chip (SoC) have become of great value because of their low cost and ease of use. Applications such as the thermal management of processors or SoCs [1]–[3], ambient temperature monitoring [4], and biomedical devices [5]–[7] are some examples. Recently, with the emergence of the Internet of Things (IoT), the need for sensors with as low-power consumption as possible to extend the battery life has become a focus of research. The low power operation is also required in an IoT node with a battery that has a large internal resistance $R_{BAT}$. The maximum instantaneous current from a battery ($I_{MAX}$) is limited owing to the voltage drop caused by the internal resistance $R_{BAT}$. In the case of a miniature size IoT node with a solid-state bare die battery [8], $I_{MAX}$ is limited to only 1.7 $\mu$A after 1000 cycles owing to the increased $R_{BAT}$ when the acceptable voltage drop is 100 mV. Therefore, reducing the average current of a temperature sensor to less than 1% of $I_{MAX}$ (= 17 nA) is desirable for an IoT node with the battery [8]. Another desirable feature of the temperature sensor for IoT nodes is proportional-to-absolute-temperature (PTAT) output with a digital interface. PTAT output is beneficial for realizing low-power, real-time thermal management because complicated off-chip processing is not required.

This paper describes a fully integrated CMOS temperature-to-digital converter with power consumption of only 11 nW. This paper is an extension of a previous conference paper [9]. The key extensions of this paper over [9] are: 1) a detailed description of the operating principle; 2) a detailed analysis of the error sources; and 3) new chip design and fabrication including digital interface circuits.

The key techniques in our proposed temperature-to-digital converter are as follows: 1) a new temperature-sensing principle that utilizes a sub-threshold current at a sub-thermal drain voltage (STV) and 2) a circuit implementation of the proposed principle in a 180-nm CMOS process which enables the temperature sensor to achieve ultra-low power consumption of 11 nW at 25 °C. The measured resolution is 145 mK, and the measured inaccuracy is −0.9/+1.2 °C for nine samples in a temperature range of −20 °C to 80 °C.

The remainder of this paper is organized as follows. Section II reviews the state-of-the-art of temperature sensors. Section III introduces the operation principle of the proposed temperature-sensing mechanism. Section IV proposes an ultra-low-power circuit implementation of the proposed temperature-to-digital converter. Section V demonstrates some measurement results of our temperature-to-digital converter. Section VI concludes this paper.

## II. State-of-the-Art Temperature Sensors

An on-chip temperature-to-digital converter that consists of a temperature sensor, its bias circuitry, and an ADC, all integrated into the same die, is often called a smart temperature sensor. For temperature sensing in a CMOS process, the device of choice is a parasitic bipolar junction transistor (BJT), which can be realized using the same diffusions as those used

Manuscript received June 30, 2018; revised September 26, 2018, December 12, 2018, and December 20, 2018; accepted December 20, 2018. Date of publication January 29, 2019; date of current version February 21, 2019. This paper was approved by Guest Editor Nan Sun. *(Corresponding author: Teruki Someya.)*

T. Someya was with the University of Tokyo, Tokyo 153-8505, Japan. He is now with Tokyo Institute of Technology, Tokyo 152-8550, Japan (e-mail: someya@ssc.pe.titech.ac.jp).

A. K. M. M. Islam was with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan. He is now with the Department of Electrical Engineering, Graduate School of Engineering, Kyoto University, Kyoto 615-8510, Japan.

T. Sakurai and M. Takamiya are with the University of Tokyo, Tokyo 153-8505, Japan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2891718

for MOSFETs. A BJT-based temperature sensor is generally self-referenced because a self-generated bandgap voltage is used to digitize the base-to-emitter voltage ($V_{\mathrm{BE}}$) difference between two BJTs biased by different collector currents. The voltage difference, $\Delta V_{\mathrm{BE}}$, is PTAT thus providing an on-chip digital representation of temperature with the use of an ADC. These sensors are also called bandgap temperature sensors and provide accuracy of less than ±0.1 °C under the temperature range of −55 °C to 125 °C with one-point calibration [10], [11]. One disadvantage of bandgap temperature sensors is that they require high-accuracy ADC circuits to achieve an accurate temperature sensing, which increases their power consumption [12].

To realize a sub-1-V temperature sensor, the replacement of BJTs with diode-connected MOSFETs was proposed in [13]. With the help of a zoom ADC, temperature inaccuracy of ±0.4 °C was achieved after one-point calibration with a power consumption of approximately 600 nW (excluding the digital backend). Temperature-sensing mechanisms using the logic gate delay of CMOS have also been proposed, facilitating ease-of-design [14]. Such sensors require calibration with two or three points and also require a nonlinear master curve. Thus, the generation of an on-chip digital output requires further processing that consumes power.

MOSFET sub-threshold current can also be used as a replacement of BJTs to achieve temperature sensing. Sub-threshold MOSFET-based temperature sensors enable a low voltage and low power consumption. Although they suffer from lower accuracy and typically require a two-point calibration, they are expected to be beneficial for many practical applications where the need for high accuracy and resolution can be relaxed. Recently, a new class of temperature sensors utilizing MOSFET sub-threshold current has been proposed. A current-to-frequency converter (CFC)-based temperature sensor, where the frequency of an oscillator becomes exponential to the absolute temperature, was proposed in [12]. To obtain a PTAT digital value, the logarithm operation is required. Furthermore, nonlinear fitting is used to achieve an accuracy of −0.76/+0.76 °C. In [15], a 113-pW temperature-to-digital converter with a temperature range of only −20 °C to 40 °C, which is too limited for many applications, was proposed. Although a 120-nW temperature sensor was also proposed in [16], the covered temperature range was only −10 °C–30 °C, and the topology requires an external reference clock, which increases the additional power consumed by its generation. To realize an inherent on-chip PTAT quantity, in [17], a linear approximation of the exponential function, $\exp(x)$, was utilized by choosing the $x$ carefully. The required $x$ was realized by taking the ratio of the sub-threshold currents of two MOSFETs biased at different $V_{\mathrm{GS}}$ values. The linearity of the sensor was dependent on the optimum value, which may vary because of mismatch.

In this paper, we take a similar approach to that used in [17] but use a different physical phenomenon to obtain the PTAT quantity. We keep the $V_{\mathrm{GS}}$ value the same but apply different $V_{\mathrm{DS}}$ values to the two MOSFETs. By setting the $V_{\mathrm{DS}}$ for one MOSFET much larger than the thermal voltage $V_T$ and setting $V_{\mathrm{DS}}$ for the other MOSFET below $V_T$, the corresponding current ratio provides better linearity and sensitivity than those obtained by the mechanism proposed in [17].

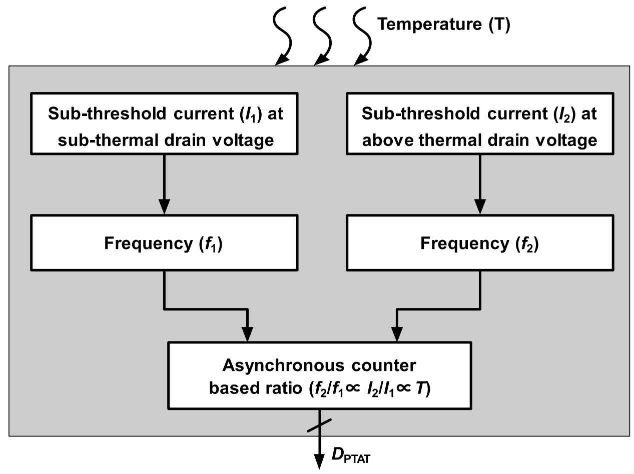



Fig. 1. Flowchart of the proposed temperature-to-digital converter.

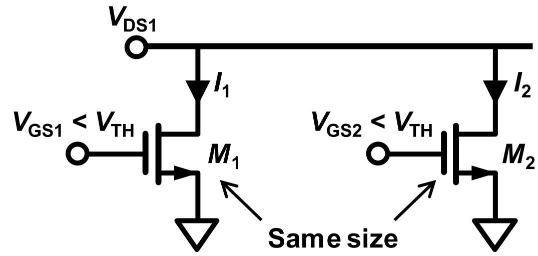



Fig. 2. Mechanism of the conventional temperature sensing [17].

## III. Proposed Temperature-Sensing Mechanism

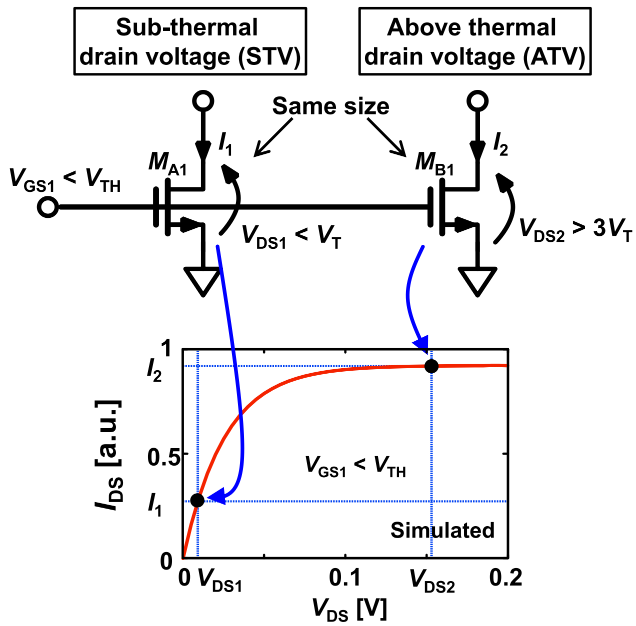
Fig. 1 shows a flowchart of the proposed temperature-to-digital converter. The process of conversion from the temperature to a PTAT digital output has three steps: 1) generation of two sub-threshold currents obtained from a pair of nMOSFETs with different drain voltages ($I_1$, $I_2$); 2) current-to-frequency conversion ($f_1$, $f_2$); and 3) frequency ratio ($f_2/f_1$) calculation for the PTAT digital output ($D_{\mathrm{PTAT}}$). The key point here is that the current ratio $I_2/I_1$ shows a PTAT characteristic in the target temperature range of −20 °C to 80 °C. The details of the principle of achieving a PTAT $I_2/I_1$ are described in the next.

### A. Temperature Sensing Mechanism

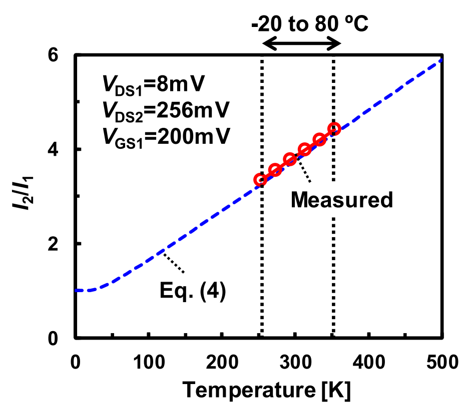
A PTAT $I_2/I_1$ is required to realize the proposed temperature-to-digital converter shown in Fig. 1. Fig. 2 shows the temperature-sensing principle of a conventional work [17] that achieves a PTAT $I_2/I_1$ by approximating an exponential function by a linear function. In [17], two identical nMOSFETs in the sub-threshold region with different gate voltages of $V_{\mathrm{GS1}}$ and $V_{\mathrm{GS2}}$ were implemented to achieve a PTAT $I_2/I_1$. The current ratio of $I_2$ to $I_1$ is expressed as

$$\frac{I_2}{I_1} = \exp\left(\frac{\Delta V_{\mathrm{GS}}}{n V_{\mathrm{T}}}\right) \tag{1}$$

where $\Delta V_{\mathrm{GS}} = V_{\mathrm{GS2}} - V_{\mathrm{GS1}}$, $V_{\mathrm{T}}$ $(= kT/q)$ is the thermal voltage, $k$ is Boltzmann's constant, $q$ is the electron charge, $T$ is the absolute temperature, and $n$ is the sub-threshold swing




(a)




(b)

Fig. 3. Proposed temperature-sensing mechanism. (a) $V_{DS}$ biasing of MOSFETs. (b) Theoretical and measured $I_2/I_1$ for a single transistor.

parameter. In (1), $I_2/I_1$ has an optimum $\Delta V_{GS}$ that maximizes the linearity of $I_2/I_1$ in a temperature range. For a typical $n$ of 1.4, the optimum $\Delta V_{GS}$ is $-72$ mV in the temperature range of $-20$ °C to 80 °C. The sensitivity of $I_2/I_1$ is calculated to be 0.0009/°C when $\Delta V_{GS}$ is $-72$ mV.

Fig. 3(a) shows the operating principle of our proposed temperature-sensing mechanism. Two identical nMOSFETs $M_{A1}$ and $M_{B1}$ operating in the sub-threshold region are biased with different $V_{DS}$ values. An STV less than the thermal voltage $V_T$(= 26 mV at 27 °C) is applied to $V_{DS1}$, while above thermal drain voltage (ATV) more than 3 $V_T$ is applied to $V_{DS2}$. As a result, drain currents of $M_{A1}$ and $M_{B1}$ are expressed as follows [18]:

$$I_1 = K \cdot \exp\left(\frac{V_{GS1} - V_{TH}}{nV_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)\right) \quad (2)$$

$$I_2 = K \cdot \exp\left(\frac{V_{GS1} - V_{TH}}{nV_T}\right) \quad (3)$$

where $K$ is a technology-related parameter and $V_{TH}$ is the threshold voltage of the transistors. The current ratio $I_2/I_1$

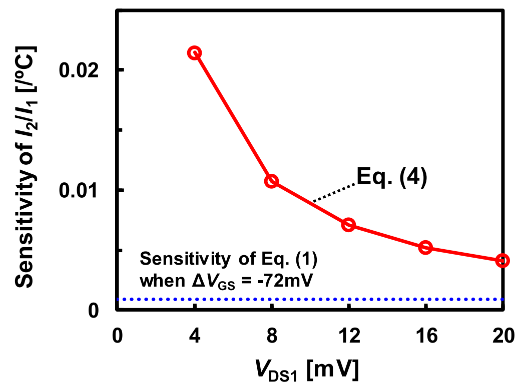



Fig. 4. Sensitivity of $I_2/I_1$.

becomes a function of $V_{DS1}$ and $T$ as follows:

$$\frac{I_2}{I_1} = \frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)}. \quad (4)$$

Assuming that $V_{DS1}$ is sufficiently smaller than $V_T$, $I_2/I_1$ is approximated as

$$\frac{I_2}{I_1} = \frac{V_T}{V_{DS1}} + C \quad (5)$$

where $C$ is a temperature-independent constant. Equation (5) shows that the sensitivity of $I_2/I_1$ to $T$ can be improved by reducing $V_{DS1}$. $I_2/I_1$ in (4) with $V_{DS1}$ of 8 mV is plotted in Fig. 3(b) along with the measured $I_2/I_1$ in the temperature range of $-20$ °C to 80 °C using a single nMOSFET implemented in a 180-nm CMOS process. The theoretical slope (= sensitivity) of $I_2/I_1$ obtained from (5) is 0.0107/°C, whereas the measured slope of $I_2/I_1$ is 0.0108/°C. The measured and theoretical slopes agree within an error of 1%. Fig. 4 shows the theoretical sensitivity of $I_2/I_1$ obtained from (5). The proposed principle has over ten times higher sensitivity than that in [17] when $\Delta V_{GS}$ in (1) is set to $-72$ mV and $V_{DS1}$ in (5) is set to 8 mV. Fig. 5(a) shows the adjusted $R^2$ for (4) versus $V_{DS1}$ in the temperature range of $-20$ °C to 80 °C with the adjusted $R^2$ in (1) obtained when $\Delta V_{GS} = -72$ mV. Theoretically, the proposed temperature sensing mechanism shows higher linearity when $V_{DS1} < 12$ mV. Fig. 5(b) shows the peak-to-peak inaccuracy of $I_2/I_1$ in the temperature range of $-20$ °C to 80 °C. Two-point calibration is performed by reading $I_2/I_1$ at 0 °C and 60 °C. The proposed temperature sensing mechanism enables both higher sensitivity and better linearity than those in [17].

### B. Mismatch Effect

The matching of $M_{A1}$ and $M_{B1}$ is important in the proposed temperature sensing principle. A mismatch between $M_{A1}$ and $M_{B1}$ may affect the linearity of $I_2/I_1$. Considering the mismatch between $M_{A1}$ and $M_{B1}$, (4) is modified to

$$\begin{aligned}\frac{I_2}{I_1} &= \exp\left(\frac{-\Delta V_{TH}}{nV_T}\right)\frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)}\\ &= K_0(T)\frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)}\end{aligned} \quad (6)$$

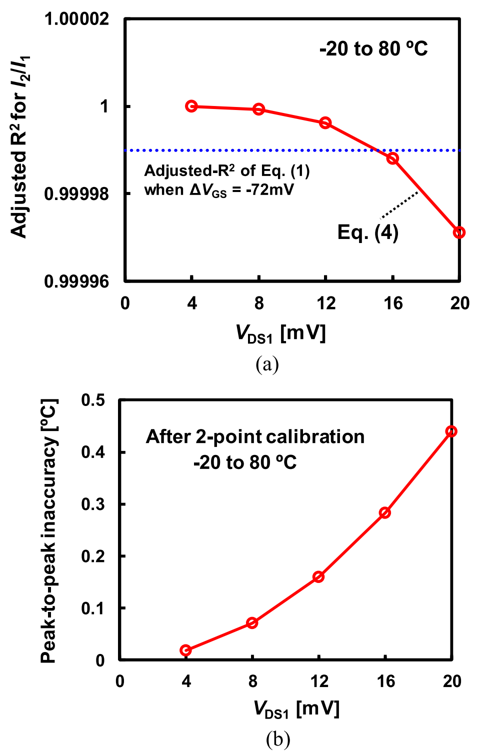



Fig. 5. (a) Adjusted $R^2$ of $I_2/I_1$. (b) Inaccuracy of the temperature-sensing calculated from $I_2/I_1$.

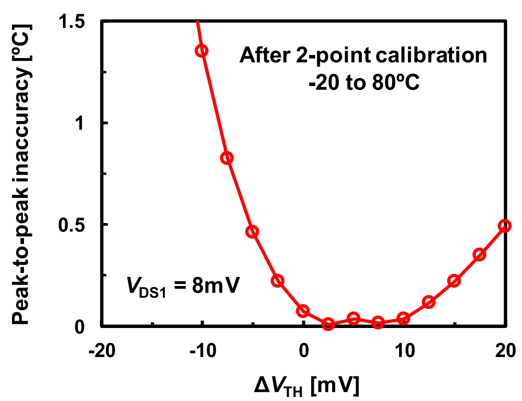



Fig. 6. Effect of the transistor mismatch on the accuracy of the temperature sensing.

where $\Delta V_{\mathrm{TH}} = V_{\mathrm{TH2}} - V_{\mathrm{TH1}}$. When $\Delta V_{\mathrm{TH}} \ll nV_{\mathrm{T}}$, $K_0(T)$ is approximated as 1 and $I_2/I_1$ shows the PTAT characteristics in (5). Conversely, when $\Delta V_{\mathrm{TH}}$ is not sufficiently smaller than $nV_{\mathrm{T}}$, the accuracy of $I_2/I_1$ is affected by the mismatch. Fig. 6 shows the $\Delta V_{\mathrm{TH}}$ dependence of the inaccuracy of $I_2/I_1$ after a two-point calibration obtained from (6) in the temperature range of −20 °C to 80 °C. $n$ of 1.4 obtained from a SPICE simulation was used for the analysis. The error of 0.07 °C at $\Delta V_{\mathrm{TH}} = 0$ is the inherent inaccuracy of $I_2/I_1$ when $V_{\mathrm{DS1}}$ is set to 8 mV as shown in Fig. 5(b). These results show that the mismatch of the transistor pair may reduce the accuracy of $I_2/I_1$.

$\Delta V_{\mathrm{TH}}$ for a pair of MOSFETs is described by the standard deviation

$$\sigma_{\Delta\mathrm{VTH}} = \frac{A_{\mathrm{VT}}}{\sqrt{WL}} \tag{7}$$

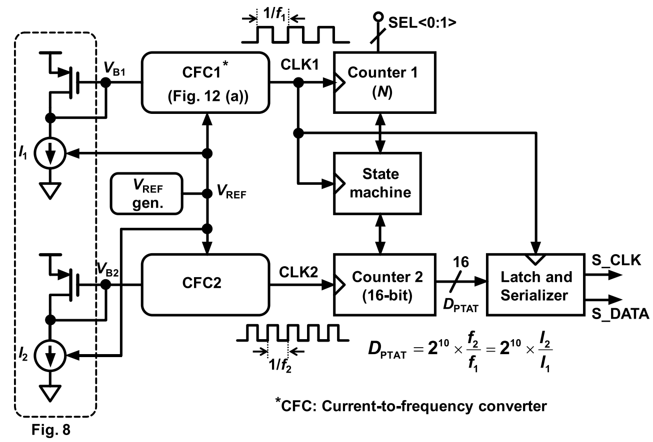



Fig. 7. Overall block diagram of the proposed temperature-to-digital converter.

where $A_{\mathrm{VT}}$ is the slope in Pelgrom plot [19]. Using a typical $A_{\mathrm{VT}}$ of 3.3 mV·$\mu$m for a 180-nm CMOS process [20], we set $W$ and $L$ for the transistors as 8.0 and 1.5 $\mu$m, respectively, which give $\sigma_{\Delta\mathrm{VTH}}$ of 0.95 mV. Thus, according to Fig. 6, an additional peak-to-peak error of 0.3 °C may occur considering the $3\sigma_{\Delta\mathrm{VTH}}$ value of the $\Delta V_{\mathrm{TH}}$ mismatch.

## IV. Design of Temperature-to-Digital Converter

Fig. 7 shows a block diagram of the proposed temperature-to-digital converter. The current generators generate currents $I_1$ and $I_2$ obtained from nMOSFETs with different drain voltages. Two clock signals, CLK1 and CLK2, are generated using CFCs based on relaxation oscillators. The corresponding frequencies $f_1$ and $f_2$ are linear to the currents $I_1$ and $I_2$, respectively. As a result, $f_2/f_1$ shows the same PTAT characteristic as $I_2/I_1$. The counter-based scheme in [21] is used to readout the PTAT digital output. CLK1 and CLK2 are fed to two asynchronous binary counters that enable the on-chip digital conversion of $f_2/f_1$ $(= I_2/I_1)$ without any external clock references. CLK2 edge is counted until CLK1 edge has been counted up to a predefined number $N$. When CLK1 has been counted to $N$, the value of Counter 2 $(= D_{\mathrm{PTAT}})$ is latched and converted to a 16-bit serial output (S_DATA). In our design, $N$ can be programed in the range of 10–13 bits. The programmability of $N$ enables the programing of the resolution of the temperature-to-digital converter. The resolution has a tradeoff relationship with the conversion time, i.e., $m$ times finer resolution requires $m$ times larger conversion time. Designers or users should select the highest resolution while meeting the required conversion time in the usage. In our temperature-to-digital converter, a voltage reference is implemented to supply a constant voltage $V_{\mathrm{REF}}$ for the analog components. The voltage reference makes the temperature-to-digital converter free from external references. In our design, a two-transistor-based on-chip voltage reference presented in [22] is used.

### *A. Current Generators*

In the proposed principle shown in Fig. 3(a), a circuit implementation that regulates $V_{\mathrm{DS1}}$ to an STV and $V_{\mathrm{DS2}}$ to an ATV is required. In particular, a temperature-independent

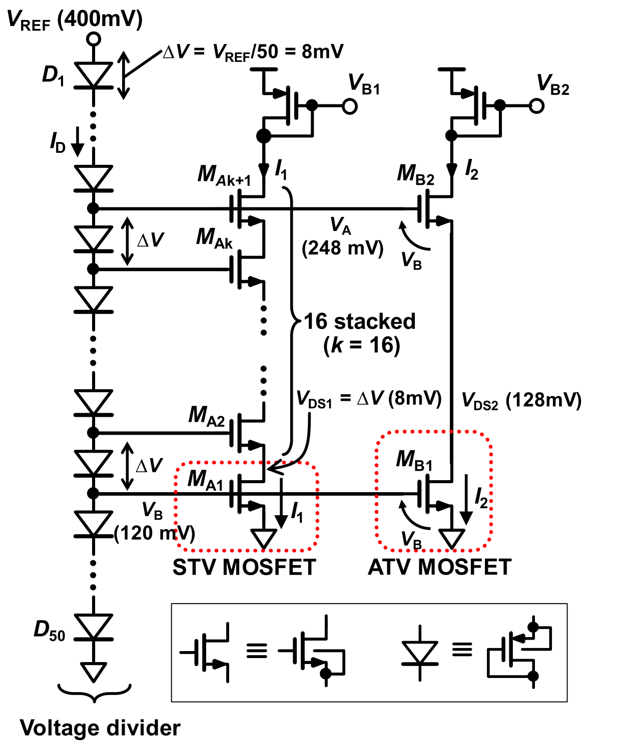
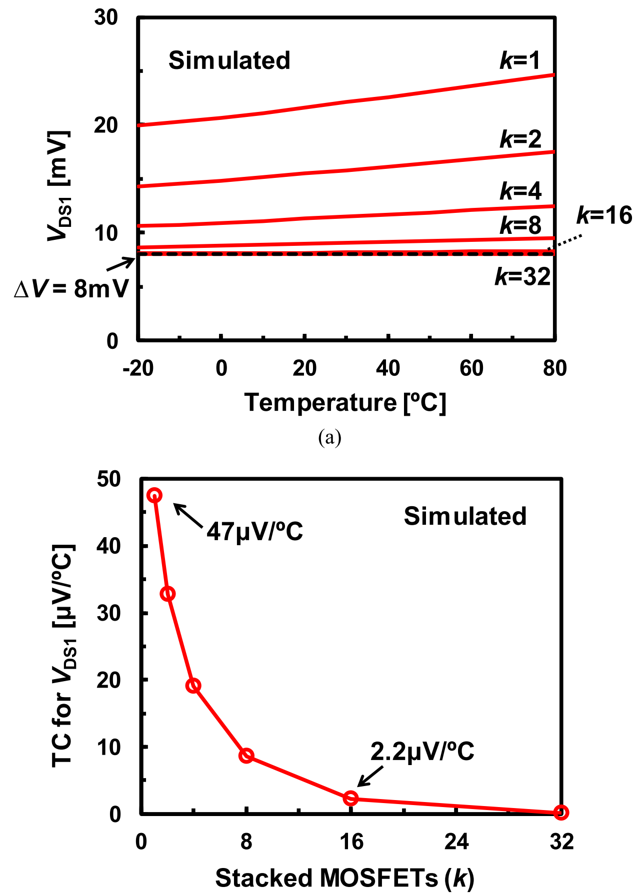



Fig. 8. Circuit schematic of the current generators using STV and ATV MOSFETs.

$V_{DS1}$ is indispensable for $M_{A1}$. The temperature dependence of $V_{DS1}$ decreases the linearity of $I_2/I_1$. Moreover, the offset voltage in $V_{DS1}$ may decrease the sensitivity of $I_2/I_1$. We can calculate the effect of the offset voltage on the sensitivity of $I_2/I_1$ from (5). For example, when the target $V_{DS1}$ is 8 mV, offsetting $V_{DS1}$ by $\pm 5\%$ (= 0.4 mV) increases/decreases the sensitivity of $I_2/I_1$ by $\pm 5\%$. Therefore, we propose a circuit implementation to realize the accurate $V_{DS1}$ while maintaining the low power operation.

Fig. 8 shows a circuit schematic of the proposed current generators including the $V_{DS1}$ bias circuitry. A reference voltage ($V_{REF}$) supplied by the $V_{REF}$ generator shown in Fig. 7 is equally divided by a 50-stage diode chain, where the voltage drop across each diode is $\Delta V (= V_{REF}/50 \approx 8$ mV). The operation principle of the current generator for $I_2$ is based on the voltage subtraction mechanism proposed in [22]. We assume that $M_{B1}$ and $M_{B2}$ are identical nMOSFETs with drain voltages of over 3 $V_T$. The gate-to-source voltages of these transistors must be the same since the currents of $M_{B1}$ and $M_{B2}$ are identical, which forces $V_{DS2}$ to be $V_A - V_B$. In Fig. 8, $V_{DS2}$ is 128 mV because $V_A$ and $V_B$ are 248 and 120 mV, respectively. Thus, $M_{B1}$ acts as the ATV MOSFET shown in Fig. 3(a). Realizing a drain–source bias voltage to be below the thermal voltage is challenging as the STV MOSFET $M_{A1}$ must operate in the deep triode region. When the stack number $k$ is 1, $V_{DS1}$ does not converge to $\Delta V$ and has a temperature-dependent offset voltage ($V_{OS}$). However, with increasing $k$, $V_{DS1}$ gradually converges to $\Delta V$. Fig. 9(a) and (b) shows the simulated temperature characteristics and temperature coefficient (TC) for $V_{DS1}$ against $k$, respectively. $V_{OS}$ for $V_{DS1}$ is over 10 mV with a TC of 47 $\mu$V/°C when $k = 1$. The offset and TC decrease the




(a)

(b)

Fig. 9. (a) Temperature characteristics of $V_{DS1}$. (b) TC of $V_{DS1}$ with various $k$.

sensitivity and accuracy of $I_2/I_1$. We solve the problem by increasing the stack number $k$ to obtain a $V_{DS1}$ value of $\Delta V$ and reduce the temperature dependence of $V_{DS1}$. Although $V_{OS}$ occurs in the source node of $M_{AK+1}$ owing to the difference in the operating regions between $M_{AK+1}$ and $M_{AK}$, the effect of $V_{OS}$ on $V_{DS1}$ is mitigated by the stacked nMOSFETs ($M_2$ to $M_{Ak}$) and $V_{DS1}$ converges to $\Delta V$. The simulation results as shown in Fig. 9(a) and (b) confirm that $V_{DS1}$ approaches $\Delta V$ with increasing $k$, and the TC is also reduced consequently. However, increasing $k$ results in a larger area. Thus, the $V_{DS1}$ accuracy and the circuit area are in a tradeoff relationship. The current of the voltage divider $I_D$ must be sufficiently lower than the output current limit of the voltage reference. In our design, $I_D$ is set to less than 10 pA in room temperature. The simulated currents of $I_1$ and $I_2$ at room temperature are 80 pA and 260 pA, respectively. The total current of the current generators is 350 pA.

To estimate an appropriate value of $k$, the effect of the temperature dependence of $V_{DS1}$ on the inaccuracy of $I_2/I_1$ is considered. As shown in Fig. 9(a), the temperature characteristic of $V_{DS1}$ in the proposed current generator shows a monotonic increase for each value of $k$. Assuming that $V_{DS1}$ has a temperature coefficient of $\alpha$ ppm/°C and expressed as

$$V_{DS1} = \frac{V_{REF}}{M}(1 + \alpha(T - T_R) \times 10^{-6}) \tag{8}$$

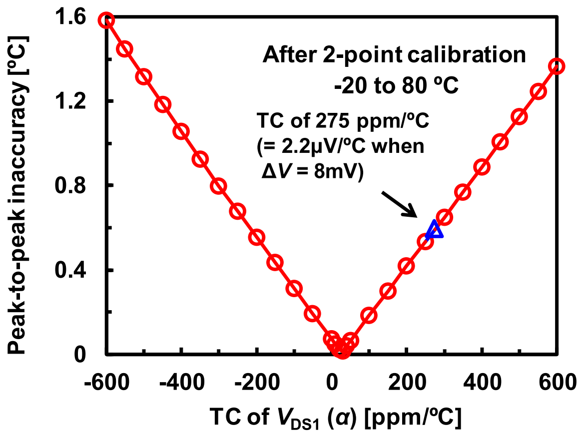



Fig. 10. Dependence of the inaccuracy of the temperature sensing on the temperature coefficient of $V_{\mathrm{DS1}}$ when the target $V_{\mathrm{DS1}} = 8$ mV.

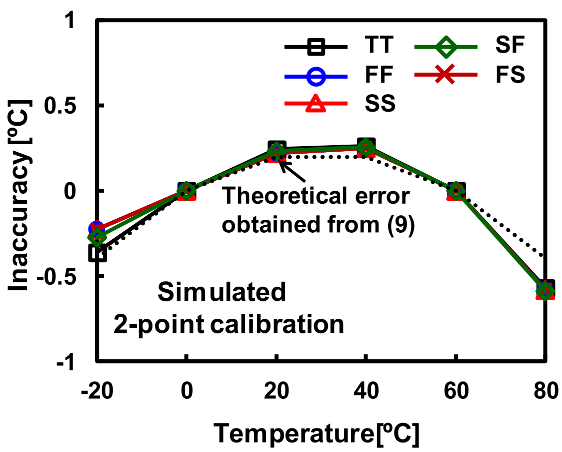



Fig. 11. Process corner analysis of the inaccuracy of the temperature sensing.

where $M$ is the number of diodes in the voltage divider, $V_{\mathrm{REF}}/M$ $(= \Delta V)$ is the target $V_{\mathrm{DS1}}$, and $T_R$ is a reference temperature, $I_2/I_1$ is given as

$$\frac{I_2}{I_1} = \frac{1}{1 - \exp\left(-\Delta V \frac{1+\alpha(T-T_R)\times 10^{-6}}{V_{\mathrm{T}}}\right)}. \tag{9}$$

Fig. 10 shows the peak-to-peak temperature errors using $I_2/I_1$ in (9) after two-point calibration when $T_R = -20$ °C, and the target temperature range is $-20$ °C to 80 °C. As shown in Fig. 10, an increase in the temperature dependence of $V_{\mathrm{DS1}}$ increases the error. In our design, $k = 16$ is selected, resulting in $\alpha = 2.2$ $\mu$V/°C and, in theory, to a 0.6 °C inaccuracy in $I_2/I_1$ when $\Delta V = 8$ mV. Fig. 11 shows the simulated inaccuracy of $I_2/I_1$ for our designed current generators for different process corners. The worst simulated peak-to-peak inaccuracy is 0.84 °C in the process corners. The obtained simulated results relatively differ from the theoretical error obtained from (9) at high temperatures. One possible reason is that the theoretical error shown in (9) is introduced under the condition that the TC of $V_{\mathrm{DS1}}$ is first order. If we can include higher order factors, the model will be improved to match the actual characteristics. The accuracy of $I_2/I_1$ can be further improved by increasing $k$ at the cost of the increased area. Thus, the proposed technique achieves a constant $V_{\mathrm{DS1}}$ and $V_{\mathrm{DS2}}$ with a small current overhead of 350 pA.

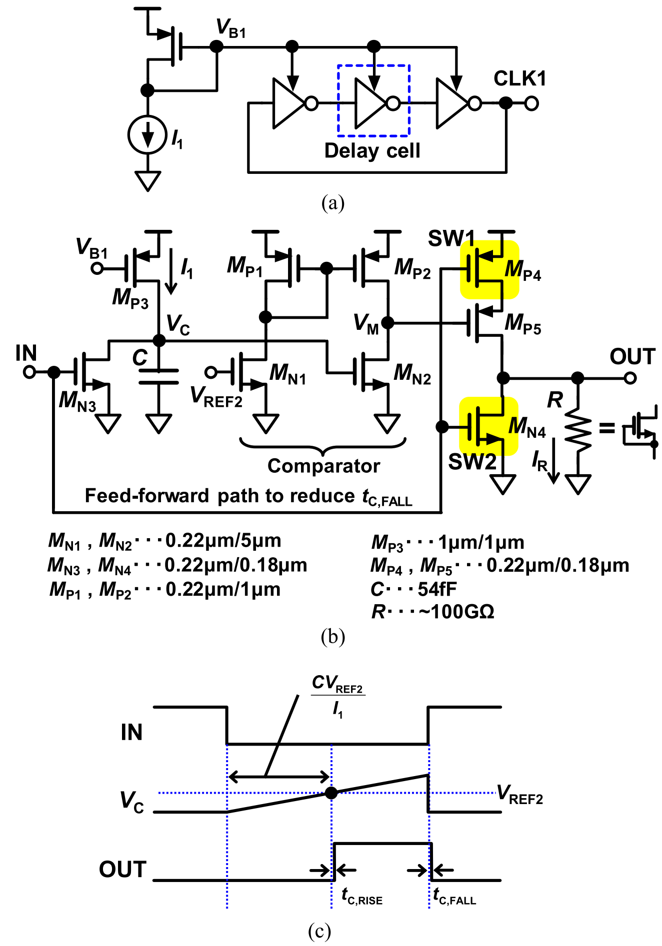



Fig. 12. (a) Concept of the CFC. (b) Schematic of the delay cell. (c) Timing diagram of the delay cell.

## *B. Current-to-Frequency Converter*

In Fig. 7, the oscillation frequency of CLK1 (CLK2) must be highly linear to $I_1$ ($I_2$). The proposed CFCs are based on a relaxation oscillator as shown in Fig. 12(a). The oscillation period of CFC1 is expressed as

$$T_{\mathrm{OSC},1} = N_{\mathrm{CELL}}\left(\frac{C\,V_{\mathrm{REF2}}}{I_1} + t_{\mathrm{C,FALL}} + t_{\mathrm{C,RISE}}\right) \tag{10}$$

where $N_{\mathrm{CELL}}$ $(= 3$ in our design) is the number of delay cells in CFC1, and $t_{\mathrm{C,FALL}}$ and $t_{\mathrm{C,RISE}}$ are the propagation delays of the proposed delay cell in the CFCs. $V_{\mathrm{REF2}}$ is a fixed voltage for the comparators in the delay cells obtained from the diode chain in Fig. 8. The oscillation period of CFC2 $(= T_{\mathrm{OSC},2})$ is also obtained from (10) by exchanging $I_1$ with $I_2$. $t_{\mathrm{C,FALL}}$ and $t_{\mathrm{C,RISE}}$ should be sufficiently small compared with $CV_{\mathrm{REF2}}/I_1$ so that $T_{\mathrm{OSC},1}$ becomes proportional to $CV_{\mathrm{REF2}}/I_1$. In this case, $f_2/f_1$ $(= T_{\mathrm{OSC},1}/T_{\mathrm{OSC},2})$ gives the same PTAT characteristics as $I_2/I_1$. In the delay cell shown in Fig. 12(b), the first stage is a differential amplifier with a pMOSFET current mirror load acting as a comparator. The negative input is biased at $V_{\mathrm{REF2}}$ $(< V_{\mathrm{TH}})$. In the second stage, a common-source amplifier with a large load resistor is implemented to reduce $t_{\mathrm{C,RISE}}$.

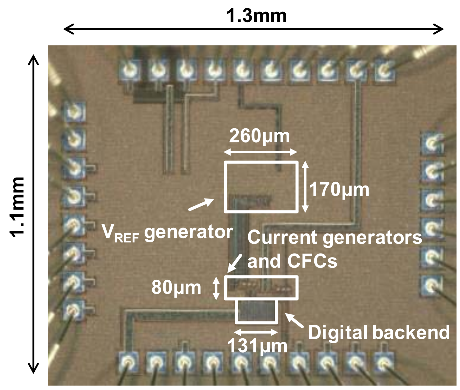



Fig. 13. Chip photograph of the proposed temperature-to-digital converter.

The load resistor is implemented with an OFF transistor. To achieve sub-1-nW static power consumption in the delay cell, the resistor ($R$) should be large (e.g., 5 GΩ). However, the large $R$ increases $t_{C,FALL}$ owing to the limited current $I_R$. To reduce $t_{C,FALL}$, we utilize a split-output scheme [23] that decouples the comparator stage from the pull-down path. A feed-forward path composed of SW1 and SW2 is added in the second stage in Fig. 12(b). When IN changes from low to high, the propagation through the first stage and the second stage in the comparator is bypassed and OUT is pulled down by SW2, which leads to the reduction of $t_{C,FALL}$. In the simulation, $t_{C,RISE}$ and $t_{C,FALL}$ are reduced to less than 2% and 0.1% of $CV_{REF}/I_1$, respectively, in the temperature range of −20 °C to 80 °C at $V_{DD} = 0.8$ V.

The frequencies of the CFCs are set to over 1 kHz to make the conversion within 1 s at room temperature when $N = 10$ bits in Fig. 6. The frequencies of CFCs are temperature dependent that makes the conversion time of the temperature sensor temperature-dependent. In our measurement, $f_1$ ranged from 100 Hz to 10 kHz in the temperature range of −20 °C to 80 °C. If the temperature sensor is used in the wide temperature range especially in lower than 0 °C, designers must consider that the temperature sensor meets the demand for conversion time. The conversion time can be improved at the cost of the power consumption or resolution by reducing $N$ in Fig. 7.

### *C. Voltage Reference*

In the temperature sensor, a voltage reference is required to achieve the current generators shown in Fig. 8. In this paper, two-transistor-based voltage reference presented in [22] is applied to the current generators which operate with nW power consumption. On the other hand, a standard voltage $V_{REF}$ supplied by two-transistor voltage reference has temperature dependence due to the mismatch [24]. We assume that $V_{REF}$ with a temperature coefficient $\beta$ ppm/°C is given by

$$V_{REF} = V_{REF,R} + \beta V_{REF,R}(T - T_R) \times 10^{-6} \tag{11}$$

where $V_{REF,R}$ is $V_{REF}$ when $T$ is a reference temperature $T_R$. By substituting (11) into (8), $V_{DS1}$ is expressed as

$$V_{DS1} \approx \frac{V_{REF,R}}{M}(1 + (\alpha + \beta)(T - T_R) \times 10^{-6}). \tag{12}$$

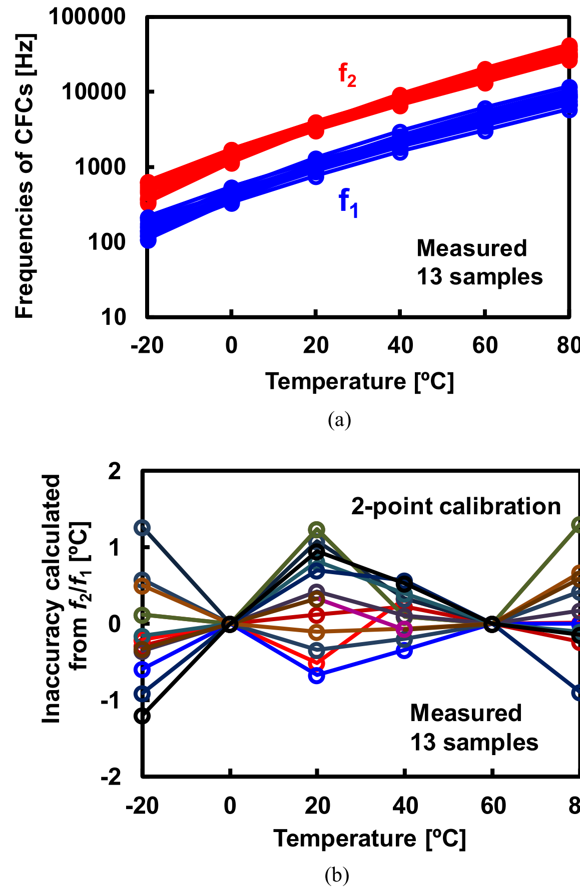



Fig. 14. (a) Frequencies of the CFCs. (b) Inaccuracy of the temperature sensors calculated from $f_2/f_1$ [9].

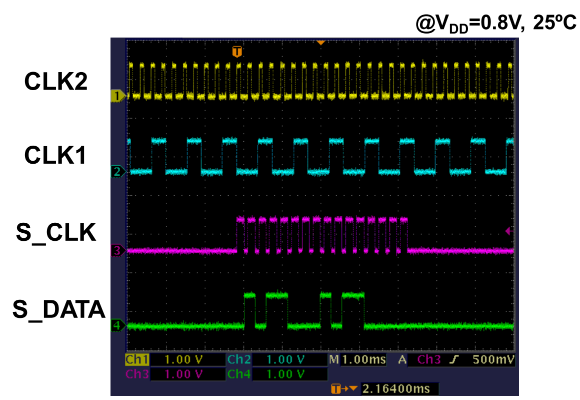
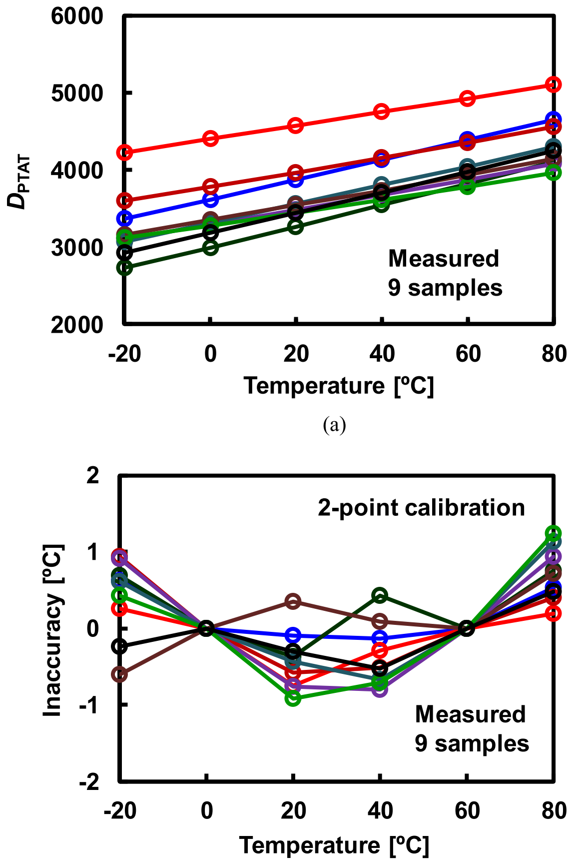



Fig. 15. Measured waveforms of the proposed temperature-to-digital converter.

The peak-to-peak temperature inaccuracy obtained from $I_2/I_1$, under the condition that $V_{REF}$ has a TC of $\beta$, $T_R = -20$ °C, and $V_{REF,R}/M = 8$ mV, can then be estimated from Fig. 10 by replacing $\alpha$ with $\alpha + \beta$. Overall, temperature affects $V_{DS1}$ in two ways. The first effect comes from the $V_{REF}$ itself. The second effect comes from the current generators as shown in Fig. 9. Thus, the TC variability of $V_{DS1}$ is a statistical sum of TCs of $\Delta V$ and the current generator as shown in (12). The reported absolute TC of a two-transistor voltage reference [24] without trimming is ranged from 17 to 231 ppm/°C. In the worst case, i.e., when $V_{REF}$ has a TC of 231 ppm/°C, the peak-to-peak inaccuracy of $I_2/I_1$ is 1.2 °C in our simulation.



(b)

Fig. 16. Measured (a) $D_{PTAT}$ and (b) temperature inaccuracy among nine dies.

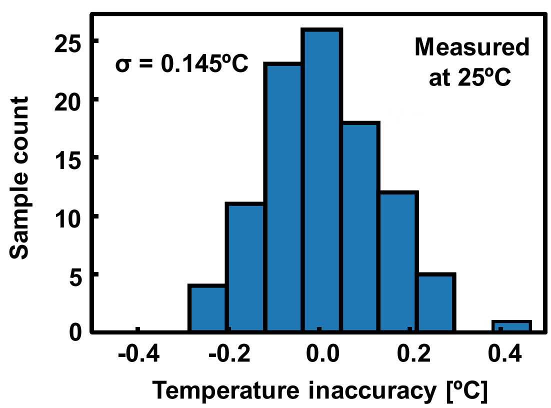



Fig. 17. Measured temperature inaccuracy of 100 reading.

Post-fabrication one-temperature point trimming is an effective method of reducing the TC of $V_{REF}$ [24]. In [24], the 2T voltage reference utilizing the trimming method reduces the worst TC of $V_{REF}$ to less than 47 ppm/°C, which reduces the simulated peak-to-peak inaccuracy of the proposed temperature sensing to less than 0.9 °C. By implementing trimming for the voltage reference, the accuracy of the temperature sensor can be improved.

## V. Measurement Results

The proposed temperature-to-digital converter including a voltage reference [22] and digital backend is fabricated in a 180-nm CMOS process.

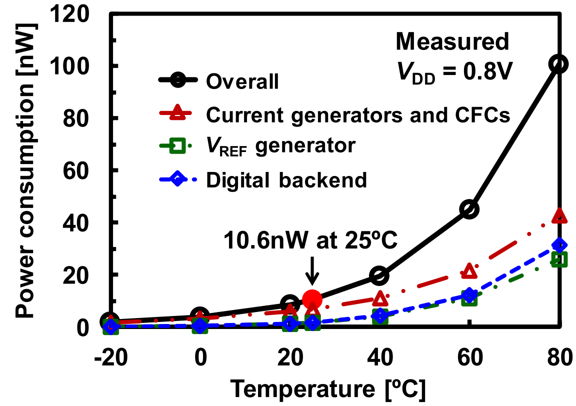



Fig. 18. Power consumption of the temperature-to-digital converter.

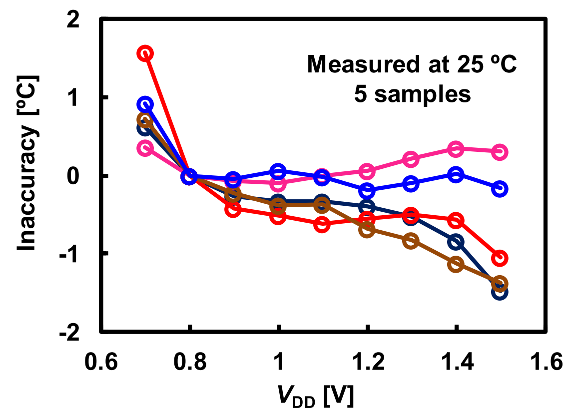



Fig. 19. $V_{DD}$ dependence of the temperature inaccuracy.

Fig. 13 shows a chip photograph of our temperature-to-digital converter. The total area of the temperature-to-digital converter including the digital backend is 0.074 mm$^2$. In [9], to measure the inaccuracy of the temperature sensor, $f_1$ and $f_2$ were measured with an oscilloscope as shown in Fig. 14(a), and the inaccuracy was estimated by taking $f_2/f_1$ as shown in Fig. 14(b). In this paper, the digital serialized $D_{PTAT}$ (= S_DATA in Fig. 7) is read for the samples to measure the accuracy and resolution of the temperature sensor. Fig. 15 shows the waveforms of CLK1, CLK2, S_CLK, and S_DATA shown in Fig. 7 at 0.8 V and 25 °C. Fig. 16(a) shows the obtained $D_{PTAT}$ of nine samples in the temperature range of −20 °C to 80 °C, while Fig. 16(b) shows the inaccuracy of the temperature-to-digital converters. After a two-point calibration, the peak-to-peak inaccuracy of the nine samples in this paper is −0.9/+1.2 °C. The counter-resolution, which is the LSB associated with the 10-bit conversion of the temperature-to-digital converter, among the measured samples is 94 mK. Owing to the thermal noise, the sampled counter value $D_{PTAT}$ varies in each measurement. To evaluate the sensory resolution, $D_{PTAT}$ is measured 100 times at a fixed temperature (25 °C in this paper) [25]. Fig. 17 shows the 100 samples of the temperature inaccuracy. The standard deviation of the samples is 1.54 LSB, which corresponds to a noise-limited resolution of 145 mK. Fig. 18 shows the power consumption of the entire circuit and each component in the temperature-to-digital converter. The power consumption of the entire circuit is 10.6 nW at room temperature (25 °C).

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED MOSFET-BASED LOW-POWER TEMPERATURE SENSORS

| | This work (w/ digital backend) | CICC'[9] (w/o digital backend) | JSSC'14 [21] | A-SSCC'14 [17] | ISSCC'17 [12] | ISSCC'14 [13] |
|---|---|---|---|---|---|---|
| CMOS process [nm] | 180 | 180 | 180 | 65 | 180 | 160 |
| PTAT digital output | Yes | Yes | Yes | Yes | No | Yes |
| Type | MOSFET | MOSFET | MOSFET | MOSFET | MOSFET | DTMOS |
| Area [mm$^2$] | 0.074 | 0.065 | 0.09 | 0.022 | 0.22 | 0.085 |
| Supply voltage | 0.8 | 0.8 | 1.2 | 0.4 | 1.2 | 0.85 |
| Power [nW] | 11 | 13*1 | 71 | 280 | 570 | 600 |
| Conversion time [ms] | 839 (at 25ºC) | 861 (at 25ºC) | 30 | 25 | 8 | 6 |
| Energy/conversion [nJ] | 8.9 | 11 | 2.2 | 7 | 4.6 | 3.6 |
| Temperature range [ºC] | -20 ~ 80 | -20 ~ 80 | 0 ~ 100 | 0 ~ 100 | -20 ~ 80 | -40 ~ 125 |
| Inaccuracy [ºC] | -0.9/1.2*2 (9 samples) | -1.2/1.3*2 (13 samples) | -1.4/1.5*2 (18 samples) | -1.6/1.0*2 (8 samples) | -0.76/0.76*3 (5 samples) | -0.4/0.4*3 (16 samples) |
| Calibration point | 2-point | 2-point | 2-point | 2-point | 2-point | 1-point |
| Resolution [mK] | 94*4<br>145*5 | 105*4 | 300*5 | 250*6 | 90*5 | 63*5 |
| Resolution FoM *7 [nJ·K$^2$] | 0.19 | 0.14*8 | 0.19 | 0.44 | 0.037 | 0.0141 |
| $V_{DD}$ sensitivity [ºC/V] | 3.8 at 25ºC, 0.7 ~ 1.5 V (5 samples) | 4.6 at 20ºC, 0.8 ~ 1.4 V (3 samples) | 14 at 25ºC, 1.0 ~ 1.4 V (1 sample) | N/A | 0.36, 0.8 ~ 1.8 V | 0.45, 0.85 ~ 1.2 V |

*1) Power consumption of digital backend is estimated by simulation
*2) Peak-to-peak inaccuracy
*3) 3σ inaccuracy
*4) Counter resolution
*5) Noise-limited resolution
*6) Definition of resolution is not clearly mentioned
*7) Resolution FoM = (Energy/Conversion) × (Resolution)$^2$ [26]
*8) Calculated from counter resolution

The current generators and CFCs consume 6.9 nW, $V_{\mathrm{REF}}$ generator and digital backend consume 1.9 and 1.8 nW, respectively. The power consumption of the voltage reference is increased from that of [9] so that it is less affected by the switching noise from the digital circuits. Even when the temperature increases to 80 °C, the power consumption of the entire circuit is 100 nW. Fig. 19 shows the measured $V_{\mathrm{DD}}$ dependence of temperature inaccuracy for five samples at 25 °C. The inaccuracy over a $V_{\mathrm{DD}}$ range from 0.7–1.5 V is $-1.5/+1.6$ °C which results in a $V_{\mathrm{DD}}$ sensitivity of 3.8 °C/V.

In Table I, the performance of the proposed temperature-to-digital converter and the previous MOSFET-based low-power temperature sensors are summarized and compared. The proposed temperature-to-digital converter has the lowest power consumption of 11 nW at 25 °C in Table I, while achieving a competitive inaccuracy of $-0.9/+1.2$ °C among nine samples and a resolution of 145 mK.

## VI. CONCLUSION

In this paper, an 11-nW ultra-low power temperature-to-digital converter is proposed. A new principle of the temperature sensing based on the sub-threshold operation at STV contributes to realizing a linear PTAT digital output while achieving a competitive resolution. A circuit implementation of the current generators and CFCs realizes the proposed sensing principle under the ultra-low power operation. The circuit implementation of the temperature-to-digital converter achieves the lowest power consumption of 11 nW among the temperature sensors that covers the temperature range of $-20$ °C to 80 °C. Measurement results of the test chips fabricated in a 180-nm CMOS process show that the temperature-to-digital converter realizes $-0.9/+1.2$ °C inaccuracy over a temperature range of $-20$ °C to 80 °C with a resolution of 145 mK.

## REFERENCES

[1] T. Yang, S. Kim, P. R. Kinget, and M. Seok, "Compact and supply-voltage-scalable temperature sensors for dense on-chip thermal monitoring," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2773–2785, Nov. 2015.
[2] U. Sönmez, F. Sebastiano, and K. A. A. Makinwa, "Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 834–843, Mar. 2017.
[3] Y.-J. An, D.-H. Jung, K. Ryu, S.-H. Woo, and S.-O. Jung, "An energy-efficient all-digital time-domain-based CMOS temperature sensor for SoC thermal management," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 8, pp. 1508–1517, Aug. 2015.
[4] J. Li, T. Yang, M. Yang, P. R. Kinget, and M. Seok, "An area-efficient microprocessor-based SoC with an instruction-cache transformable to an ambient temperature sensor and a physically unclonable function," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 728–737, Mar. 2018.
[5] P. Schönle, F. Glaser, T. Burger, G. Rovere, L. Benini, and Q. Huang, "A multi-sensor and parallel processing SoC for miniaturized medical instrumentation," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2076–2087, Jul. 2018.
[6] N. Van Helleputte *et al.*, "A multi-parameter signal-acquisition SoC for connected personal health applications," in *IEEE ISSCC Dig. Tech. Papers*, pp. 314–315, Feb. 2014.
[7] Y. Luo, K. H. Teng, Y. Li, W. Mao, C. H. Heng, and Y. Lian, "A 93 $\mu$W 11Mbps wireless vital signs monitoring SoC with 3-lead ECG, bio-impedance, and body temperature," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 29–32.
[8] *Datasheet of CBC005*, Cymbet Corp., Elk River, MN, USA.
[9] T. Someya, A. K. M. M. Islam, T. Sakurai, and M. Takamiya, "A 13 nW temperature-to-digital converter utilizing sub-threshold MOSFET operation at sub-thermal drain voltage," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[10] A. L. Aita, M. A. P. Pertijs, K. A. A. Makinwa, J. H. Huijsing, and G. C. M. Meijer, "Low-power CMOS smart temperature sensor with a batch-calibrated inaccuracy of ±0.25 °C (±3$\sigma$) from −70 °C to 130 °C," *IEEE Sensors J.*, vol. 13, no. 5, pp. 1840–1848, May 2013.
[11] B. Yousefzadeh, S. Heidary Shalmany, and K. A. A. Makinwa, "A BJT-based temperature-to-digital converter with ±60 mK (3$\sigma$) inaccuracy from −55 °C to +125 °C in 0.16-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, Apr. 2017.
[12] K. Yang *et al.*, "A 0.6 nJ −0.22/+0.19 °C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 160–161.
[13] K. Souri, Y. Chae, F. Thus, and K. Makinwa, "A 0.85 V 600 nW all-CMOS temperature sensor with an inaccuracy of ±0.4 °C (3$\sigma$) from −40 to 125 °C," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 222–223.
[14] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642–1648, Aug. 2005.
[15] H. Wang and P. P. Mercier, "Near-zero-power temperature sensing via tunneling currents through complementary metal-oxide-semiconductor transistors," *Sci. Rep.*, vol. 7, no. 1, Jun. 2017, Art. no. 4427.
[16] M. K. Law, A. Bermak, and H. C. Luong, "A sub-$\mu$W embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.
[17] W. Zhao, R. Pan, Y. Ha, and Z. Yang, "A 0.4 V 280-nW frequency reference-less nearly all-digital hybrid domain temperature sensor," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 301–304.
[18] Y. Taur and T. Ning, "MOSFET devices," *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[19] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.
[20] M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, "Transistor matching in analog CMOS applications," in *IEDM Tech. Dig.*, Dec. 1998, pp. 915–918.
[21] S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, Aug. 2014.
[22] T. Someya, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "56-level programmable voltage detector in steps of 50 mV for battery management," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 49–52.
[23] S. K. Hsu *et al.*, "A 280 mV-to-1.1 V 256b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 118–127, Jan. 2013.
[24] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.
[25] T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A VCO based highly digital temperature sensor with 0.034 °C/mV supply sensitivity," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2651–2663, Nov. 2016.
[26] K. A. A. Makinwa, *Smart Temperature Sensor Survey*. Accessed: Jun. 20, 2018. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

**Teruki Someya** (S'16–M'18) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from the University of Tokyo, Tokyo, Japan, in 2013, 2015, and 2018, respectively.

He is currently a Researcher with Tokyo Institute of Technology, Tokyo. His research interests include energy efficient ultra-low power circuits for Internet of Things (IoT) applications.

**A. K. M. Mahfuzul Islam** (S'11–M'14) received the B.E. degree in electrical and electronics engineering, the M.E. degree in communications and computer engineering, and the Ph.D. degree in informatics from Kyoto University, Kyoto, Japan, in 2009, 2011, and 2014, respectively.

From 2013 to 2015, he was a Research Fellow of Japan Society for the Promotion of Science. In 2015, he joined the Institute of Industrial Science, University of Tokyo, Tokyo, Japan, as a Research Associate. Since 2018, he has been a Junior Associate Professor with the Department of Electrical Engineering, Kyoto University. His research interests include characterization and modeling of transistor noise, low-power CMOS sensor circuits, and low-power design methodology.

Dr. Islam was a recipient of the Best Paper Award at ICMTS'2017 and the Student Design Award at A-SSCC'2013.

**Takayasu Sakurai** (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and system-on-chip (SoC) solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher with the University of California at Berkeley, Berkeley, CA, USA, where he conducted research in VLSI CAD. Since 1996, he has been a Professor with the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's, and large-area electronics. He has authored or co-authored over 600 technical publications including 100 invited presentations and several books and filed over 200 patents.

Dr. Sakurai is an IEICE Fellow. He was a recipient of the 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, the 2009 and 2010 IEEE Paul Rappaport Award, the 2010 IEICE Electronics Society Award, the 2009 IEICE Achievement Award, the 2005 IEEE ICICDT Award, the 2004 IEEE Takuo Sugano Award, and the 2005 P&I patent of the year award and four product awards. He is the Executive Committee Chair of VLSI Symposia and a Steering Committee Chair of the IEEE A-SSCC. He served as the Conference Chair of the Symp. on VLSI Circuits and ICICDT, the Vice Chair of ASPDAC, the TPC Chair of the A-SSCC and VLSI Symp., an Executive Committee Member of ISLPED, and a Program Committee Member of ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He delivered keynote speech at more than 50 conferences including ISSCC, ESSCIRC, and ISLPED. He was an Elected AdCom Member of the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS Distinguished Lecturer. He is also a domain research Supervisor for nano-electronics area in Japan Science and Technology Agency.

**Makoto Takamiya** (S'98–M'00–SM'14) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high-speed digital LSI's. In 2005, he joined the University of Tokyo, where he is currently an Associate Professor of VLSI Design and Education Center. From 2013 to 2014, he was a Visiting Scholar with the University of California at Berkeley, Berkeley, CA, USA. His research interests include the integrated power management circuits for wireless powering and energy harvesting for Internet of Things (IoT) applications, and the digital gate driver IC for power electronics.

Dr. Takamiya is a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference. He was a recipient of the 2009 and 2010 IEEE Paul Rappaport Awards and the Best Paper Award in 2013 IEEE Wireless Power Transfer Conference. He formerly served on the Technical Program Committees of IEEE Symposium on VLSI Circuits from 2009 to 2017 and IEEE Custom Integrated Circuits Conference from 2006 to 2011.