Automatic Generation of Gate Driving Vectors for Digital Gate Drivers to Satisfy EMI Regulations

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***Abstract*— To reduce the development period of power electronics equipment to satisfy EMI regulations, an automatic generation method of gate driving vectors (AGGV) for the digital gate drivers is proposed. In the proposed AGGV, the frequency spectrum of the V_{CE} waveform of IGBT is compared with the EMI limit and the gate driving vectors are automatically searched using a simulated annealing algorithm to meet the EMI limit and to minimize the switching loss. In the switching measurement of IGBT at 20 A and 300 V and a given EMI limit, compared with the conventional single step gate driving, the proposed digital gate driving reduces the switching loss by 22 %. An EMI reduction using the proposed digital gate driving, which cannot be achieved by the conventional single step gate driving, is also demonstrated.**

Keywords—Gate driver, IGBT, EMI, Optimization

I. Introduction

In the development process of power electronics equipment, the electromagnetic interference (EMI) is a troublesome problem, because the EMI measurement to check pass or fail the EMI regulations is done after the final product of the power electronics equipment is completed. When the product fails the EMI regulations, two types of measures, hardware-based approach and software-based approach, are considered. In the hardware-based approach, several components including EMI filters and shield plates are added to reduce EMI, which will increase the cost and delay the product development schedule. Therefore, the software-based approach, where the EMI spectrum is tuned using a programmable hardware, is preferred, because it is cheaper and faster than the hardware-based approach.

A programmable gate driver, which controls a gate driving waveform of power transistors during turn-on / off transients, is a promising candidate for the programmable hardware for the software-based approach. In order to check pass or fail of the EMI regulations, the frequency-domain evaluation instead of the time-domain evaluation is required, because the EMI regulations are defined in the frequency-domain. All previously reported programmable gate drivers [1-7], however, use the time-domain evaluation such as dV_{CE}/dt and d^2V_{CE}/dt^2, where V_{CE} is collector-to-emitter voltage of IGBT, to control the gate driving waveforms. In the reduction of EMI, the switching loss (E_{LOSS}) is also should be considered, because EMI and E_{LOSS} are in a trade-off relationship [3].

To solve the problems, in this paper, an automatic generation method of gate driving vectors (AGGV) for the digital gate driver (DGD) IC [8] based on the frequency-domain evaluation of V_{CE} is proposed for the first time. In AGGV, the gate driving vectors are automatically searched using a simulated annealing algorithm to meet the given EMI regulation and to minimize the switching loss, thereby achieving a highly efficient power electronics equipment complying with EMI regulations.

II. Proposed Automatic Generation Method of Gate Driving Vectors (AGGV)

The measurement setup and the gate waveform optimization method for DGD are the same as [9] except for the length of the gate driving vector for DGD, time step of DGD, and the object function for the optimization. Fig. 1 shows a circuit schematic of the measurement setup for the double pulse test of IGBT (2MBI100TA-060-50, 600 V, 100 A) at 300 V. In order to realize a programmable 63-level drivability in DGD, 63 parallel transistors are connected to the gate of IGBT and a 6-bit control signal is applied to specify

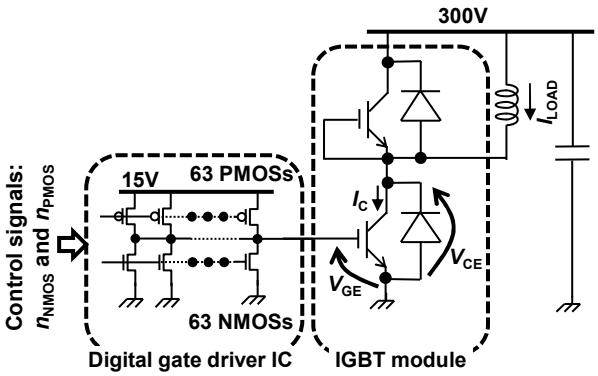


Fig. 1. Circuit schematic of measurement setup.

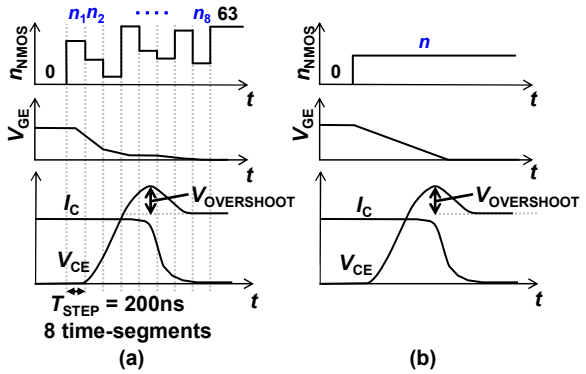
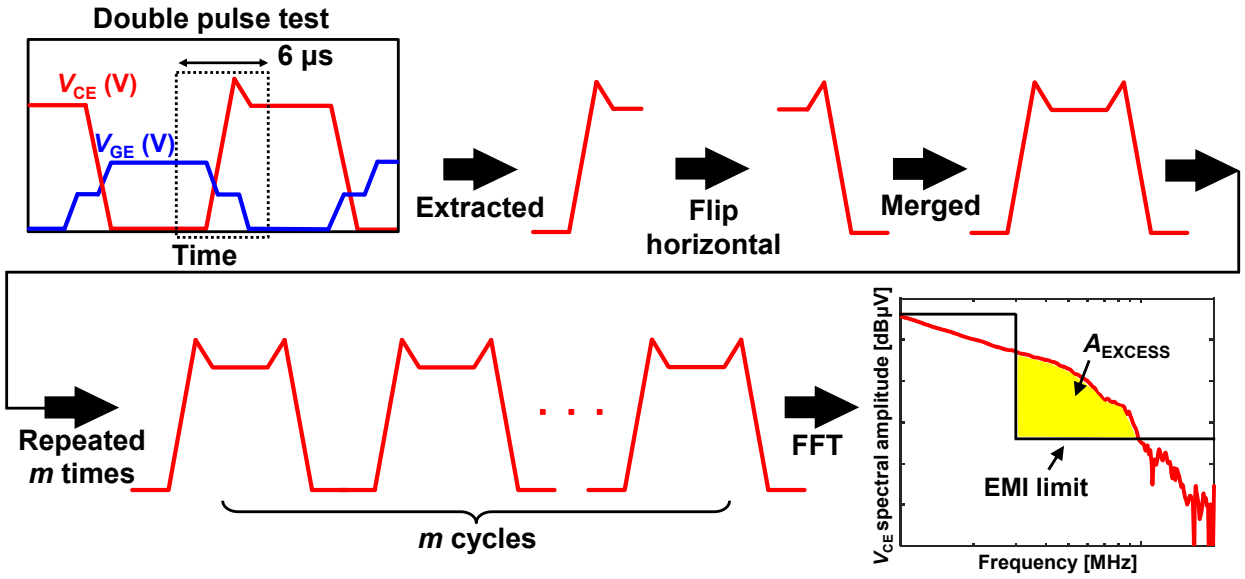
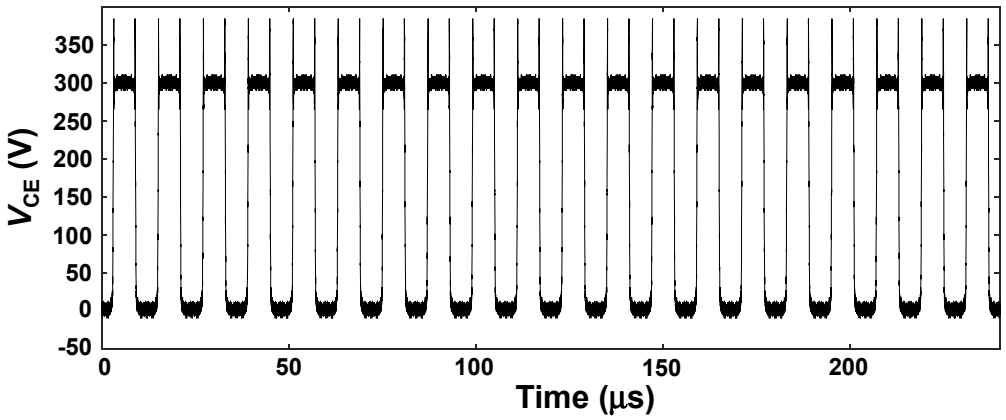


Fig. 2. Gate driving vectors and waveforms. (a) Proposed 6-bit digital gate driver. (b) conventional single-step gate drive for comparison.



(a)



(b)

Fig. 3. (a) Method to obtain spectrum from V_{CE} waveform for the frequency-domain evaluation of V_{CE}. A_{EXCESS} is area shown yellow. (b) Example of repetitive waveform made from measured V_{CE} waveform in Fig. 8 (b).

the number of activated PMOS (NMOS) transistors, n_{PMOS} (n_{NMOS}) [8]. In this paper, only turn-off is shown for simplicity. Fig. 2 (a) shows the gate driving vectors and waveforms in the 6-bit DGD for the turn-off of IGBT. In this paper, the gate driving vectors are defined as (n_1, n_2, n_3,…, n_8) , where n_1, n_2, and n_8 are integers from 0 to 63. In this paper, eight 200-ns time steps for turn-off are used, because four 400-ns time steps in [9] were not enough. Fig. 2 (b) shows the gate driving vectors and waveforms of the conventional single-step gate drive for comparison.

Fig. 3 (a) shows a method to obtain a spectrum from V_{CE} waveform obtained in the double pulse test for the frequency-domain evaluation of V_{CE}. First, a V_{CE} rise edge waveform during turn-off is extracted from the double pulse test, and it is flipped horizontally to make the fall edge waveform. Then, the rise and fall edge waveforms are merged and repeated m times (e.g. m = 20) to make a repetitive waveform. Fig. 3 (b) shows an example of the repetitive waveform made from the measured V_{CE} waveform in Fig. 8 (b). Finally, a spectrum is obtained by FFT of the repetitive waveform. In order to check pass or fail of the EMI regulations, a spectrum area (A_{EXCESS}), where the V_{CE} spectrum exceeds an EMI limit, is defined as shown in Fig. 3 (a) and Eqs. (1) to (4). A_{EXCESS} is the area shown yellow in Fig. 3 (a) and setting A_{EXCESS} to zero means that V_{CE} spectrum satisfies the EMI regulation.

$$A_{EXCESS} = \int_{F_{START}}^{F_{END}} \left\{ \frac{\max(VA_{CE}, VA_{EMI}) - VA_{EMI}}{VA_{EMI}} \right\} dF \quad (1)$$

$$F = \log_{10}\left(\frac{f}{1[MHz]}\right) \quad (2)$$

$$F_{START} = \log_{10}\left(\frac{f_{START}}{1[MHz]}\right) \quad (3)$$

$$F_{END} = \log_{10}\left(\frac{f_{END}}{1[MHz]}\right) \quad (4)$$

where VA_{CE} is the spectrum amplitude of V_{CE} in units of dBμV, VA_{EMI} is the spectrum amplitude of the EMI regulation in units of dBμV, and f is the frequency. f_{START} and f_{END} are the lower and upper limit frequency of the EMI regulation, respectively. In this paper, f_{START} is 1 MHz and f_{END} is 20 MHz. Object function (f_{OBJ}) to be minimized in the optimization using the simulated annealing algorithm [8-9] is defined as

$$f_{OBJ} = \sqrt{C_1 \cdot A_{EXCESS} + \left(\frac{E_{LOSS}}{E_{LOSS,MAX}}\right)^2} \quad (5)$$

where C_1 is a constant (C_1 = 10000) and $E_{LOSS,MAX}$ is the maximum E_{LOSS}. In the optimization, the large C_1 means that the first priority is to meet the given EMI regulation and the second priority is to minimize the switching loss. Compared with [9], only the definition of f_{OBJ} is changed and the optimization algorithm is the same. In the proposed AGGV, the gate driving vectors (n_1, n_2, n_3,…, n_8) are globally and automatically optimized by repeating the double pulse test around 4000 times using LabVIEW and MATLAB, which takes 20 to 40 minutes.

Fig. 4 shows the photo of the measurement setup. The load current is 20 A. The double pulse test measurements were made at room temperature.

III. Measured Results

In this paper, two types of virtual EMI regulations named "EMI limit A" and "EMI limit B" defined in Fig. 5 are used to demonstrate the generality of the proposed AGGV. In "EMI limit A", the spectrum amplitude of V_{CE} is 150 dBμV between 1 MHz and 5 MHz, while the spectrum amplitude of V_{CE} is 110 dBμV between 5 MHz and 20 MHz. In "EMI limit B", the spectrum amplitude of V_{CE} is 150 dBμV between 1 MHz and 8 MHz, while the spectrum amplitude of V_{CE} is 80 dBμV between 8 MHz and 20 MHz. In this paper, the relationship between EMI and E_{LOSS} is analyzed in details, because EMI and E_{LOSS} are in a trade-off relationship [3].

Figs. 6 (a) and (b) show the measured E_{LOSS} vs. A_{EXCESS} of the conventional single-step gate drive in Fig. 2 (b) with varied n from 5 (minimum in this paper) to 63 (maximum) and the proposed gate drive in Fig. 2 (a) optimized for "EMI limit A" and "EMI limit B", respectively. A_{EXCESS} of zero means that the V_{CE} waveform meets the given EMI regulation, while non-zero A_{EXCESS} means that the V_{CE} waveform violates the given EMI regulation. In the conventional single-step gate drive in Fig. 6 (a), when n is

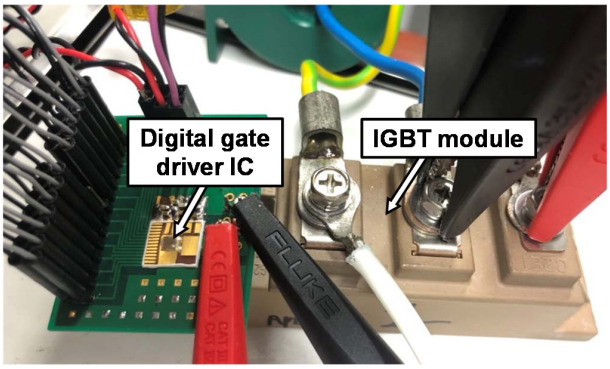


Fig. 4. Photo of measurement setup.

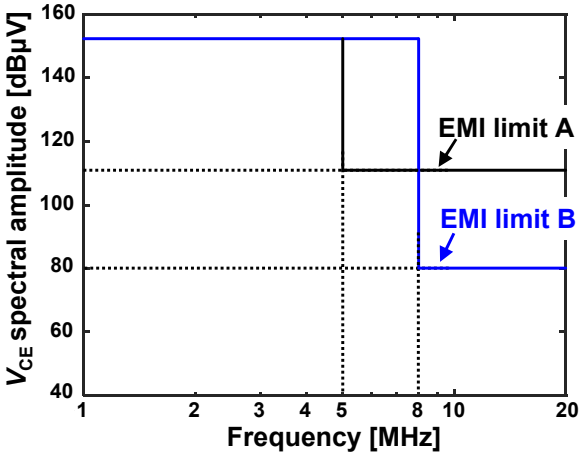
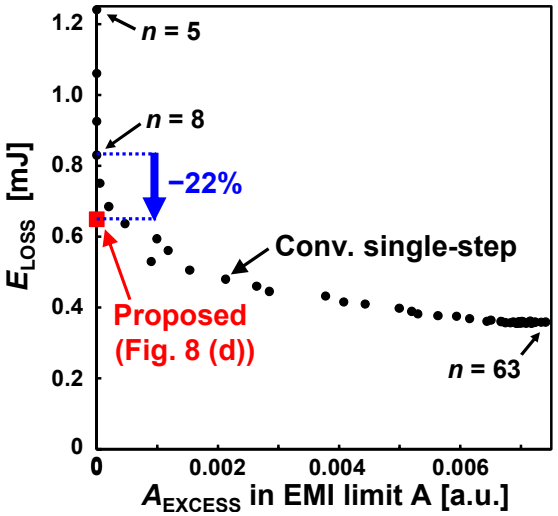
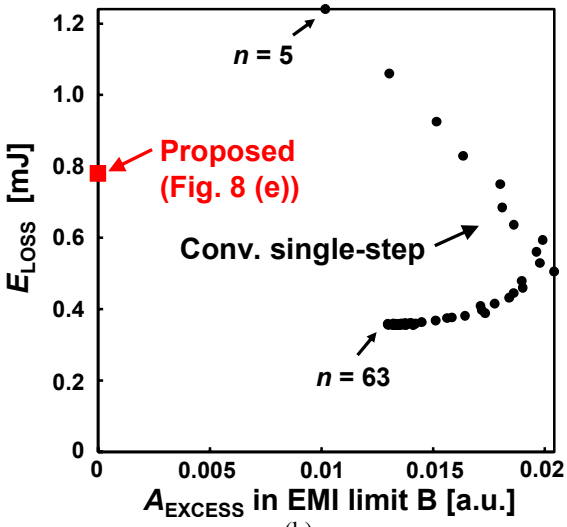


Fig. 5. Two types of virtual EMI regulations named "EMI limit A" and "EMI limit B".

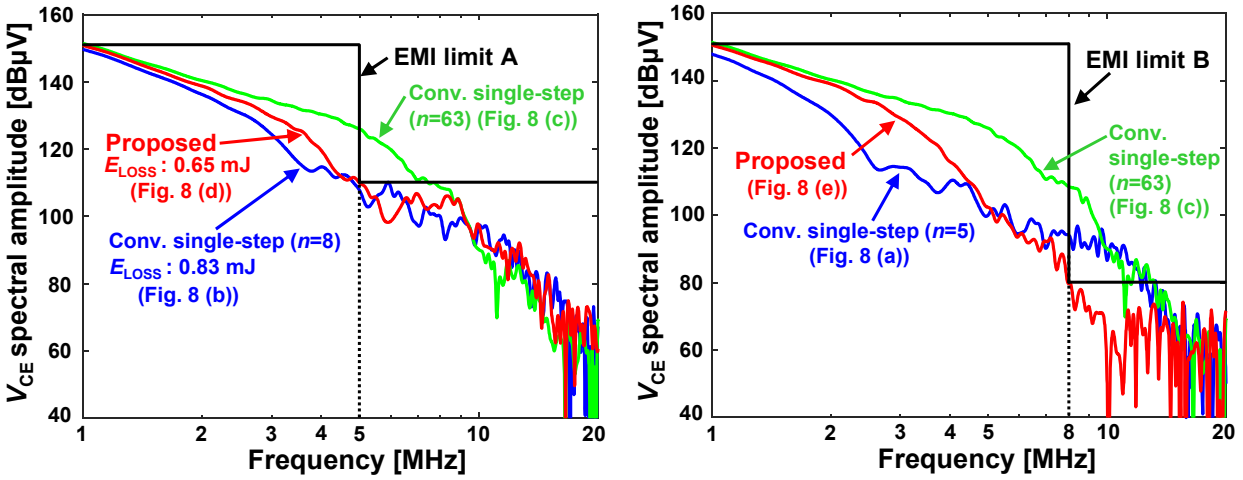


(a)

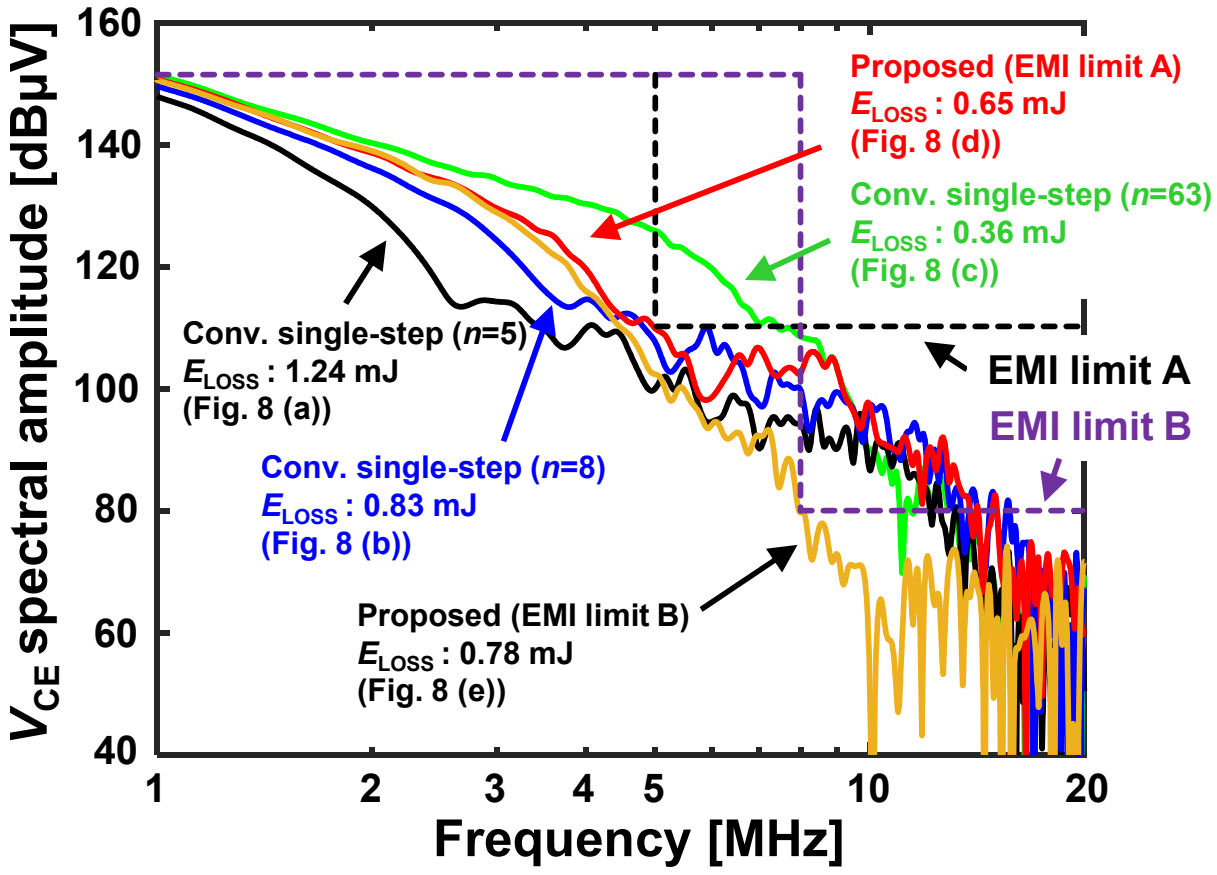


(b)

Fig. 6. Measured E_{LOSS} vs. A_{EXCESS} of conventional single-step gate drive in Fig. 2 (b) with varied n from 5 (minimum in this paper) to 63 (maximum) and the proposed gate drive in Fig. 2 (a) optimized for (a) "EMI limit A" and (b) "EMI limit B".



(a) (b)



(c)

Fig. 7. (a) Measured spectrums of V_{CE} in conventional single-step gate drive with n = 8 and 63 and proposed gate drive optimized for "EMI limit A". (b) Measured spectrums of V_{CE} in conventional single-step gate drive with n = 5 and 63 and proposed gate drive optimized for "EMI limit B". (c) Superimposed graph of (a) and (b).

increased from 5 to 63, A_{EXCESS} is increased and E_{LOSS} is reduced, which clearly shows the trade-off relationship between EMI and E_{LOSS}. In Fig. 6 (a), both the conventional single-step gate drive with varied n from 5 to 8 and the proposed gate drive meets "EMI limit A". In Fig. 6 (b), however, only the proposed gate drive meets "EMI limit B".

Fig. 7 (a) shows the measured spectrums of V_{CE} in the conventional single-step gate drive with n = 8 and 63 and the

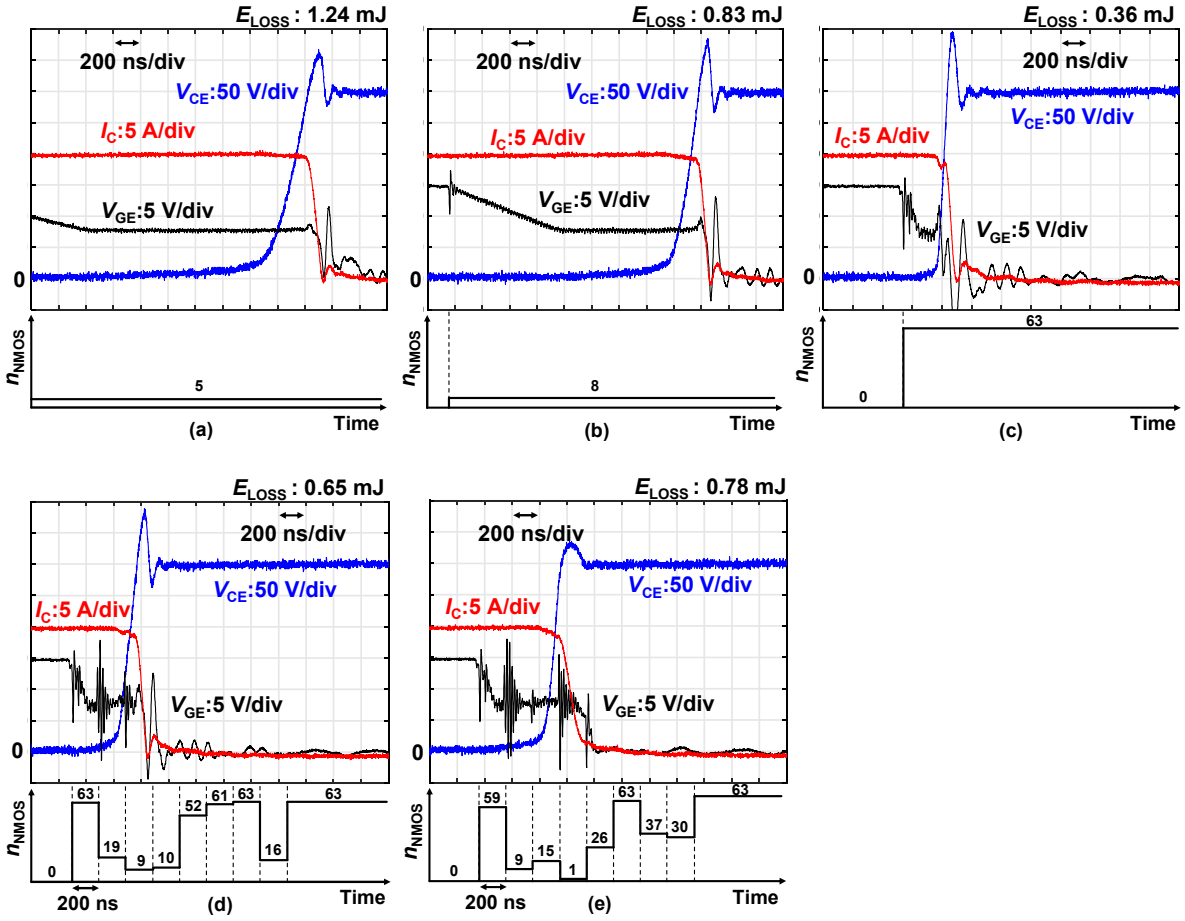


Fig. 8. Gate driving vectors and measured waveforms of V_{GE}, V_{CE}, and I_C. (a) - (c) show conventional single-step gate drives with n = 5, 8, 63, respectively. (d) and (e) show proposed gate drives optimized for "EMI limit A" and "EMI limit B", respectively.

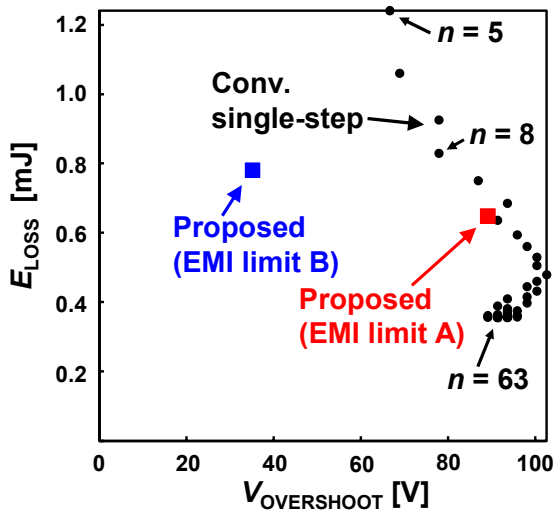


Fig. 9. Measured E_{LOSS} vs. $V_{OVERSHOOT}$ of conventional single-step gate drive with varied n from 5 to 63 and proposed gate drive optimized for "EMI limit A" and "EMI limit B".

proposed gate drive optimized for "EMI limit A". Please note that both the conventional single-step gate drive with n = 8 and the proposed gate drive just barely satisfy "EMI limit A". Fig. 7 (b) shows the measured spectrums of V_{CE} in the conventional single-step gate drive with n = 5 and 63 and the proposed gate drive optimized for "EMI limit B". Fig. 7 (c) is the superimposed graph of Figs. 7 (a) and (b). In the conventional single-step gate drive, the high-frequency components of V_{CE} increases with increasing n.

Figs. 8 (a) - (c) show the gate driving vectors and the measured waveforms of V_{GE}, V_{CE}, and I_C in the conventional single-step gate drive with n = 5, 8, 63, respectively. Figs. 8 (d) and (e) show the gate driving vectors and the measured waveforms of V_{GE}, V_{CE}, and I_C in the proposed gate drive optimized for "EMI limit A" and "EMI limit B", respectively.

As shown in Fig. 6 (a), in the conventional single-step gate drive, when n is increased from 5 to 8, E_{LOSS} is reduced with satisfying "EMI limit A". In contrast, when n is increased above 9, the conventional single-step gate drive violates "EMI limit A", while E_{LOSS} is reduced. As shown in Fig. 6 (a) and Fig. 7 (a), compared with the conventional single-step gate drive with n = 8 shown in Fig. 8 (b), the proposed digital gate driving shown in Fig. 8 (d) reduces the switching loss by 22 % with satisfying "EMI limit A".

As shown in Fig. 6 (b) and Fig. 7 (b), all conventional single-step gate drives with varied n from 5 to 63 cannot

meet “EMI limit B”, while the proposed driving shown in Fig. 8 (e) satisfies “EMI limit B”, which clearly shows the advantage of DGD.

The relationship between E_{LOSS} and $V_{OVERSHOOT}$ is also analyzed in details, because E_{LOSS} and $V_{OVERSHOOT}$ are in a trade-off relationship [9]. $V_{OVERSHOOT}$ is defined in Fig. 2. Fig. 9 shows the measured E_{LOSS} vs. $V_{OVERSHOOT}$ of the conventional single-step gate drive with varied n from 5 to 63 and the proposed gate drive optimized for “EMI limit A” and “EMI limit B”. As shown in Fig. 9, compared with the proposed gate drive optimized for “EMI limit A” shown in Fig. 8 (d), the proposed gate drive optimized for “EMI limit B” shown in Fig. 8 (e) reduces $V_{OVERSHOOT}$ from 89 V to 35 V, while E_{LOSS} is increased by 20 % from 0.65 mJ to 0.78 mJ. The reason for the reduction of $V_{OVERSHOOT}$ in Fig. 8 (e) is estimated to be $n_4 = 1$, which suggests that the transient small gate driving current during the overshoot of V_{CE} reduces $V_{OVERSHOOT}$.

IV. Conclusions

AGGV is proposed to reduce the development period of power electronic equipment to satisfy EMI regulations. In AGGV, the gate driving vectors are automatically searched to meet the given EMI regulation and to minimize the switching loss. In the switching measurement of IGBT at 20 A and 300 V and the given EMI limit, compared with the conventional single step gate driving, the proposed digital gate driving reduces the switching loss by 22 %. An EMI reduction using AGGV, which cannot be achieved by the conventional single step gate driving, is also demonstrated.

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