Power Device Degradation Estimation by Machine Learning of Gate Waveforms

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***Abstract*— The emitter resistance (R_E), the junction temperature (T_J), the collector current (I_C), and the threshold voltage (V_{TH}) of power devices are key parameters that determine the reliability of power devices. Adding dedicated sensors to measure the key parameters, however, will increase the cost of the power converters. To solve the problem, power device degradation estimation methods by the machine learning of gate waveforms are proposed. Two methods are shown in this paper. First, in order to detect the bond wire lift-off of power devices, the estimation of the number of the connected bond wires using the linear regression of two feature points extracted from the gate waveforms of a SiC MOSFET is shown using SPICE simulations. Then, in order to detect the power device degradation, the estimation of R_E, T_J, I_C, and V_{TH} using the convolutional neural network (CNN) with the gate waveforms of an IGBT for input is shown using both simulations and measurements.**

Keywords- CNN, Neural Network, IGBT, power device, degradation, reliability, gate

I. INTRODUCTION

Highly reliable power devices are required, because the power devices are important components of power electronics systems that support society. As examples of the power devices, an insulated gate bipolar transistor (IGBT) and a SiC MOSFET are discussed in this paper. The most frequent cause of the long-term degradation of the IGBTs is the bond wire lift-off due to the thermal cycles [1,2], where emitter bond wires are peeled-off from the pad. Fig. 1 (a) shows five important parameters related to the bond wire lift-off in IGBTs, the number of the connected bond wires (n), the emitter resistance (R_E), the junction temperature (T_J), the collector current (I_C), and the threshold voltage (V_{TH}). In order to measure the values of n, R_E, T_J, I_C, and V_{TH}, however, adding dedicated sensors for current, voltage and temperature will increase the cost of the power converters. Several previous papers tried to reduce the number of sensors. The estimation of I_C for an IGBT using the collector-emitter voltage (V_{CE}), gate-emitter voltage (V_{GE}), T_J, and V_{TH} as input has been investigated based on a neural network [3]. It is, however, very costly to know these voltages and T_J beforehand using sensors and only I_C can be estimated. The estimation of T_J by measuring the peak voltage of the gate drive voltage has been proposed [4]. The estimation, however, is only for T_J and since it does not use an AI-based approach, the estimation needs very high precision of the peak voltage measurement without noise, which is practically very difficult.

To solve the problems, two power device degradation estimation methods by the machine learning of the gate voltage (V_G) waveforms are proposed in this paper. Fig. 1 (b) shows a schematic of the V_G waveforms and two feature points ($V_{G,BENT}$ and $V_{G,MIN}$), where the definitions will be shown later. In Section II, as shown in Fig. 1 (c), in order to detect the bond wire lift-off of power devices, the estimation of n using the linear regression of two feature points extracted from V_G waveforms of a SiC MOSFET is shown using simulations. In Section III, as shown in Fig. 1 (d), in order to detect the power device degradation, the estimation of R_E, T_J, I_C, and V_{TH} using the convolutional neural network (CNN) with V_G waveforms of an IGBT for input is shown using both simulations and measurements.

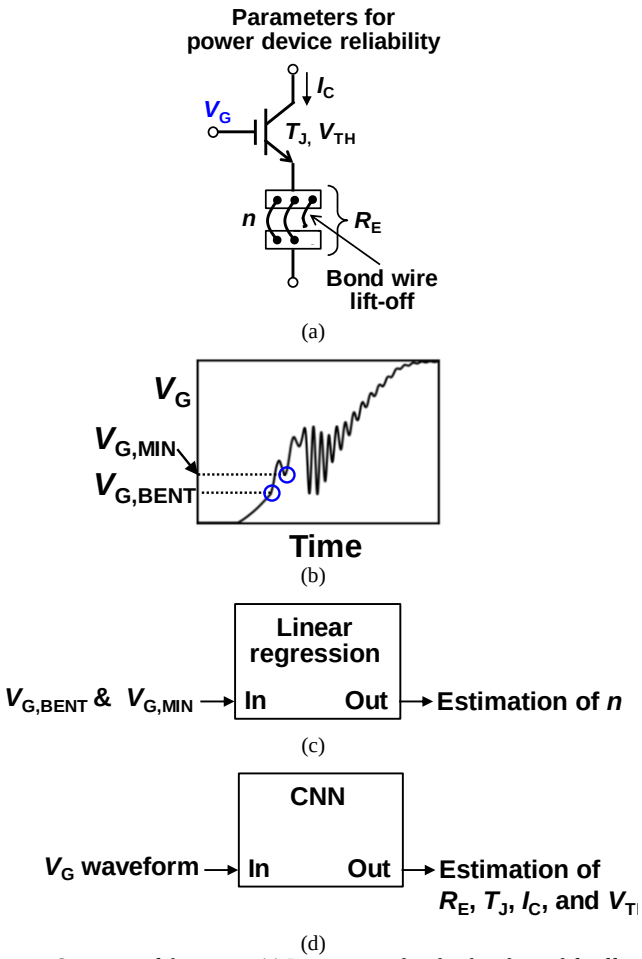


Fig. 1. Overview of this paper. (a) Parameters related to bond wire lift-off in IGBTs. (b) Schematic of V_G waveforms and two feature points ($V_{G,BENT}$ and $V_{G,MIN}$). (c) Estimation of n using linear regression of two feature points. (d) Estimation of R_E, T_J, I_C, and V_{TH} using CNN with V_G waveforms.

II. DETECTION OF BOND WIRE LIFT-OFF USING LINEAR REGRESSION OF TWO FEATURE POINTS

In order to detect the bond wire lift-off of power devices, in this chapter, the estimation of n using the linear regression of two feature points ($V_{G,BENT}$ and $V_{G,MIN}$) extracted from V_G waveforms of a SiC MOSFET is shown. As shown in Fig. 1 (b), $V_{G,BENT}$ is defined the inflection point of V_G around V_{TH}, and $V_{G,MIN}$ is defined the first minima of V_G.

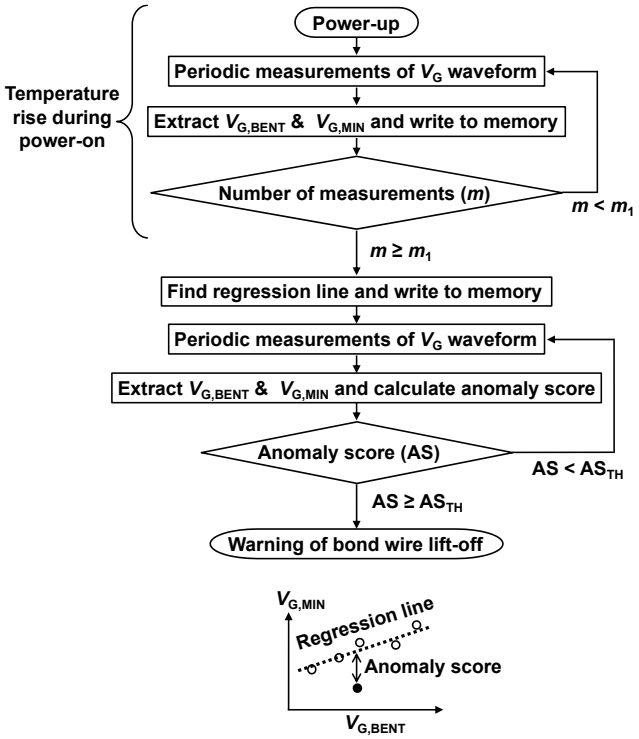


Fig. 2. Flowchart of proposed detection method of bond wire lift-off.

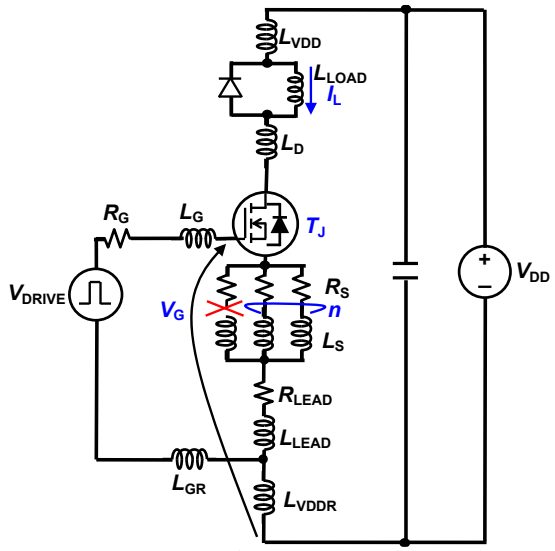


Fig. 3. Circuit schematic of double pulse test for SiC MOSFET.

Fig. 2 shows a flowchart of the proposed detection method of the bond wire lift-off. During the initial power-on of a power converter, in order to collect two feature points with different temperatures, V_G waveforms are periodically measured m_1 times, $V_{G,BENT}$ and $V_{G,MIN}$ are extracted, and they are written to memory. Then, a regression line is found using the data of $V_{G,BENT}$ and $V_{G,MIN}$, and the regression line is written to memory. After that, during the normal operation of the power converter, V_G waveforms are periodically measured, $V_{G,BENT}$ and $V_{G,MIN}$ are extracted, and an anomaly score is calculated. The anomaly score is the distance between the two feature points and the regression line. When the anomaly score is larger than the predetermined value (AS_{TH}), the bond wire lift-off is detected.

Fig. 3 shows a circuit schematic of the double pulse test for the SiC MOSFET (C3M0060065D, 650V, 37A) to demonstrate the estimation of n using the linear regression of $V_{G,BENT}$ and $V_{G,MIN}$. Table I shows the parameters for the

Table I Parameters for SPICE simulation.

	Name	Value
V_{DD}	Supply voltage	300 V
L_{VDD}	Parasitic inductance between diode and capacitor	6 nH
L_{LOAD}	Load inductance	1.5 mH
L_D	Parasitic inductance between diode and drain	3 nH
R_G	External gate resistance	2.5 Ω
L_G	Parasitic inductance between gate driver and gate	6 nH
n	Number of connected bond wires	3, 2, 1
R_S	Parasitic resistance of bond wires (n = 3, 2, 1)	0.270 mΩ, 0.405 mΩ, 0.810 mΩ
L_S	Parasitic inductance of bond wires (n = 3, 2, 1)	1.15 nH, 1.72 nH, 3.44 nH
R_{LEAD}	Parasitic resistance of lead of source	7.41 mΩ
L_{LEAD}	Parasitic inductance of lead of source	3.55 nH
L_{GR}	Parasitic inductance between ground of gate driver and lead of source	3 nH
L_{VDDR}	Parasitic inductance between lead and capacitor	6 nH
V_{DRIVE}	Gate driver voltage source	0 V / 15 V

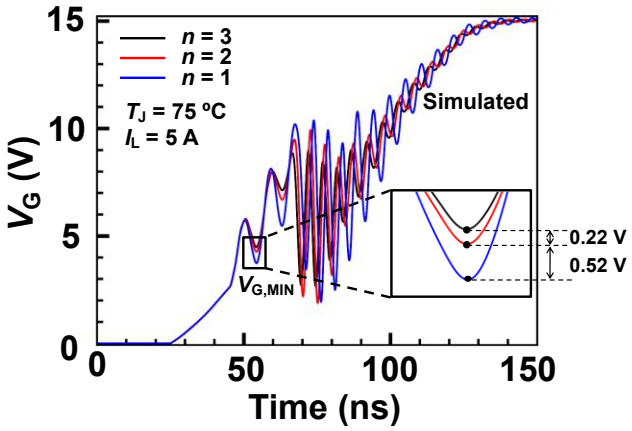


Fig. 4. Simulated V_G waveforms with varied n at T_J = 75 ºC and I_L = 5 A.

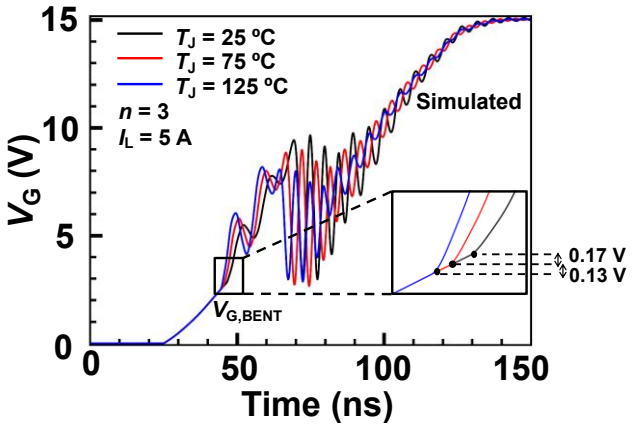


Fig. 5. Simulated V_G waveforms with varied T_J at n = 3 and I_L = 5 A.

SPICE simulation of the circuit. In the circuit simulations, n is varied to emulate the bond wire lift-off, and T_J and the load current (I_L) are varied, because T_J and I_L are key parameters to determine V_G during the operation of the power converters.

Fig. 4 shows the simulated V_G waveforms with varied n at T_J = 75 ºC and I_L = 5 A. $V_{G,MIN}$ clearly changes with n, while $V_{G,BENT}$ does not depend on n, because the R_S and L_S change with n as shown in Table I and $V_{G,BENT}$ is determined by V_{TH}.

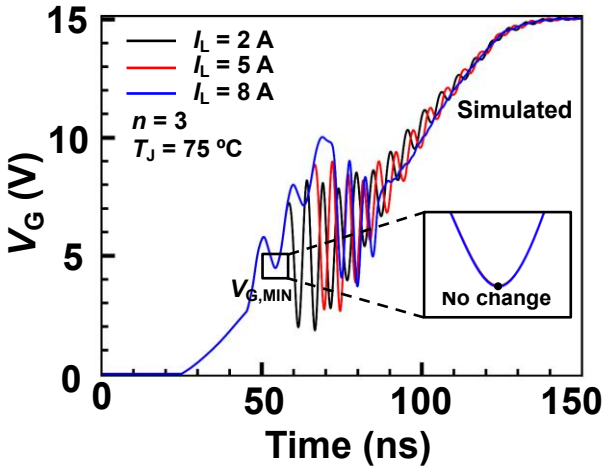


Fig. 6. Simulated V_G waveforms with varied I_L at n = 3 and T_J = 75 ºC.

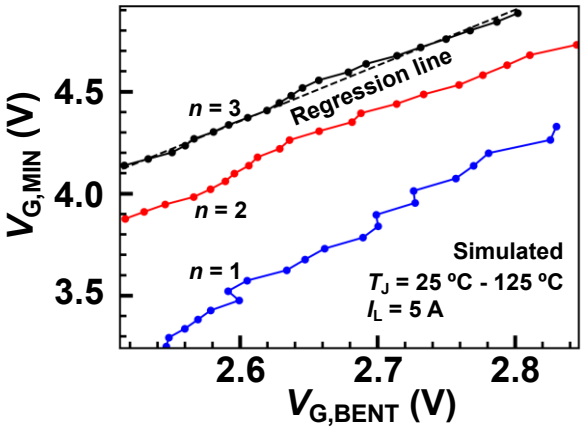


Fig. 7. Simulated relationship between $V_{G,MIN}$ and $V_{G,BENT}$ with varied T_J and n at I_L = 5 A.

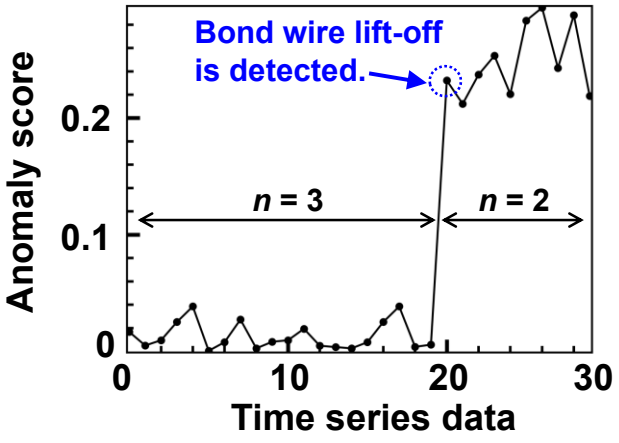


Fig. 8. Simulated time series data of anomaly score at I_L = 5 A.

Fig. 5 shows the simulated V_G waveforms with varied T_J at n = 3 and I_L = 5 A. Both $V_{G,BENT}$ and $V_{G,MIN}$ change with T_J, because T_J changes V_{TH}. Fig. 6 shows the simulated V_G waveforms with varied I_L at n = 3 and T_J = 75 ºC. Both $V_{G,BENT}$ and $V_{G,MIN}$ do not depend on I_L. The above results show that n can be estimated by a regression analysis of $V_{G,BENT}$ and $V_{G,MIN}$, because $V_{G,BENT}$ depends on T_J, and $V_{G,MIN}$ depends on both n and T_J.

Fig. 7 shows the simulated relationship between $V_{G,MIN}$ and $V_{G,BENT}$ with varied T_J and n at I_L = 5 A. When T_J increases, both $V_{G,BENT}$ and $V_{G,MIN}$ decrease, because V_{TH} is reduced.

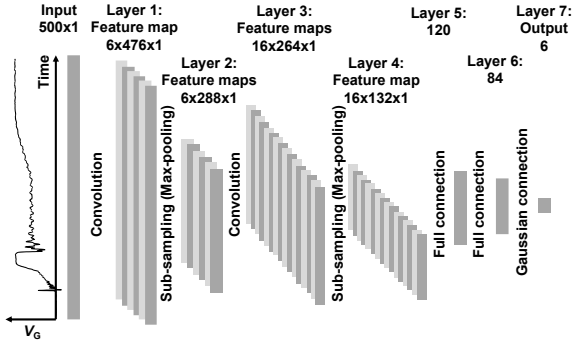
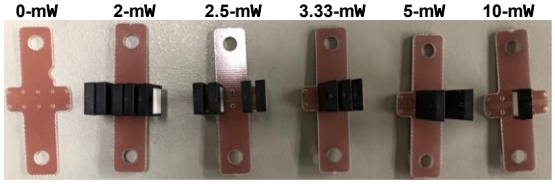


Fig. 9. CNN network adopted for measurement.

(a)



(b)

Fig. 10. (a) Measurement setup of IGBT. (b) Varied R_E to emulate the bond wire lift-off.

When n increases, only $V_{G,MIN}$ decreases as shown in Fig. 4. The regression line for n = 3 to calculate the anomaly score is also shown. When the bond wire lift-off occurs, n changes from 3 to 2, the distance between the data and the regression line increases, and the anomaly score increases, thereby detecting the bond wire lift-off. Fig. 8 shows the simulated time series data of the anomaly score at I_L = 5 A. In each data point, T_J is randomly changed between 25 ºC and 125 ºC. n is 3 in the first 20 data points, while n is 2 in the last 10 data points. When n changes from 3 to 2, the anomaly score suddenly increases from sub-0.04 to above-0.2, thereby detecting the bond wire lift-off.

III. Estimation of R_E, T_J, I_C, and V_{TH} Using Convolutional Neural Network

In order to detect the power device degradation, in this chapter, the estimation of R_E, T_J, I_C, and V_{TH} using CNN with V_G waveforms of an IGBT for input is shown using both simulations and measurements [5]. In [5], the estimation of R_E, T_J, I_C, and V_{TH} using simulations and the estimation of R_E and I_C using measurements are shown. In this paper, the measurements are shown.

Fig. 9 shows the CNN network architecture adopted for a measurement. The input is a voltage waveform of the gate driver output during the turn-on of IGBT. The input vector length is chosen to be 500, which corresponds to 6-ns cycle sampling for the entire turn-on process of 3-µs. The output is the categorized in 6 classes.

Fig. 10 shows the measurement setup with an IGBT (2MBI100TA-060-50, 600 V, 100 A) and varied R_E to emulate the bond wire lift-off. R_E is varied by changing the number of resistors in parallel. The measured waveforms are shown in Fig. 11. It is seen from the measured waveforms that it is

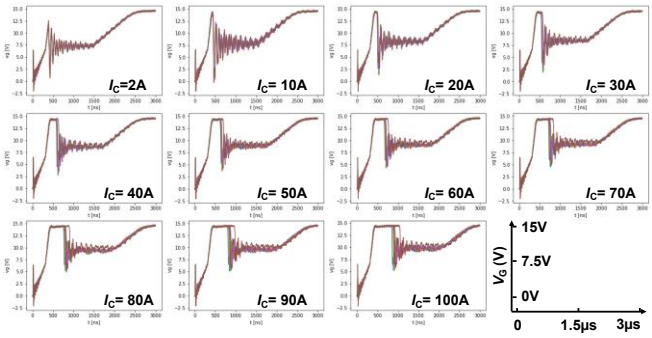


Fig. 11. Measured V_G waveforms with varied I_C.

Table II Six classes of R_E and I_C.

(a) R_E: Emitter resistance

Class #	0	1	2	3	4	5	Total
Label: R_E=	0mW	2mW	2.5mW	3.33mW	5mW	10mW	
# of waveforms	1100	1100	1100	1100	1100	1100	6600

(b) I_C: Collector current

Class #	0	1	2	3	4	5	Total
Label: I_C range	0A	15A	30A	45A	60A	75A	100A
# of waveforms	1200	600	1200	600	1200	1800	6600

Table III Estimation results using CNN.

(a) R_E: Emitter resistance

Success rate: 0.995

		Correct class						
		0	1	2	3	4	5	Ratio
Guessed class	0	275	3	0	0	0	0	0.989
	1	0	265	0	0	0	0	1
	2	0	0	264	0	0	0	1
	3	0	0	0	262	4	0	0.985
	4	0	0	0	1	279	0	0.996
	5	0	0	0	0	0	297	1
	Ratio	1	0.989	1	0.996	0.986	1	

# of epochs: 74

(b) I_C: Collector current

Success rate: 1.000

		Correct class						
		0	1	2	3	4	5	Ratio
Guessed class	0	315	0	0	0	0	0	1
	1	0	144	0	0	0	0	1
	2	0	0	272	0	0	0	1
	3	0	0	0	155	0	0	1
	4	0	0	0	0	298	0	1
	5	0	0	0	0	0	466	1
	Ratio	1	1	1	1	1	1	

# of epochs: 213

difficult to estimate R_E and I_C using human eyes. The machine recognition is needed for estimating the parameters. R_E and I_C are categorized into 6 classes this time as shown in Table II. The results of estimation using the CNN approach are tabulated in Table III. The success rate is very high amounting up to 99.5%. The number of epochs in the table shows the number of deep learning optimization loops needed for the entire learning process. Using i7 Intel processor with the clock rate of 2.5-GHz, one epoch needs approximately 1-s, which is sufficiently fast to be practical.

IV. Conclutions

Two power device degradation estimation methods by the machine learning of gate waveforms are proposed and demonstrated with simulations and measurements. Introducing the machine learning into the power electronics will be a key to increase the reliability of the power devices and to reduce the cost for various sensors.

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