

Theoretical and Experimental Analyses of Dynamic Performance of Three-Level Buck Converters in Discontinuous Conduction Mode for Standby Mode Power Supply

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A three-level buck converter in the discontinuous conduction mode (DCM), where the output power is typically less than 1 W and the output current is less than several hundreds of mA, is a key circuit for integrated voltage regulators to achieve high efficiency at a light load in the standby mode operation of microprocessors. In this study, the fundamental circuit characteristics including the conversion ratio and transfer function are analytically derived for the first time. The derived transfer function is verified via time-domain small-signal-injection simulation as well as experimental measurements using a prototype of the three-level buck converter in the DCM with off-the-shelf ICs. Similar to conventional two-level buck converters in the DCM, three-level buck converters have a first-order lag transfer function, while those in the continuous conduction mode (CCM) have a second-order lag transfer function. A compensator design for the three-level buck converters in DCM and CCM in low-power application is discussed.

Keywords: three-level buck converter, discontinuous conduction mode, dynamic performance analysis

1. Introduction

To make the energy-efficient operation of many-core microprocessors possible, fine-grained per-core dynamic voltage scaling is required. As the number of cores increases, the required number of power supply voltages also increases. Integrated voltage regulators (IVRs) are a means of generating multiple power supply voltages on a chip, because increasing the number of off-chip voltage regulators is not practical⁽¹⁾⁽²⁾. The key requirements of IVRs are a high-power conversion efficiency (η) and a small form factor.

Since the first proposal⁽³⁾, three-level DC–DC converters have attracted increasing attention in a wide range of output powers with such advantages as reduced voltage rating for switches, smaller inductor requirement for a given current ripple, and larger duty ratio for a given step-down ratio^{(4)–(14)}. In particular, for the low-power integrated circuit (IC) applications of interest in this research (typically, the output power is less than 1 W, and the output current is less than several hundred milliamperes), one of the largest advantages of the three-level DC–DC converters is that they can handle a higher input voltage, even with an advanced scaled complementary metal-oxide-semiconductor (CMOS) process with reduced voltage ratings. As shown in Fig. 1, a three-level buck converter^{(7)–(14)} combining a cascode two-level buck converter⁽¹⁾⁽²⁾ and a 1/2 switched capacitor DC–DC converter is a key circuit for IVRs, because the 3-level buck converter has

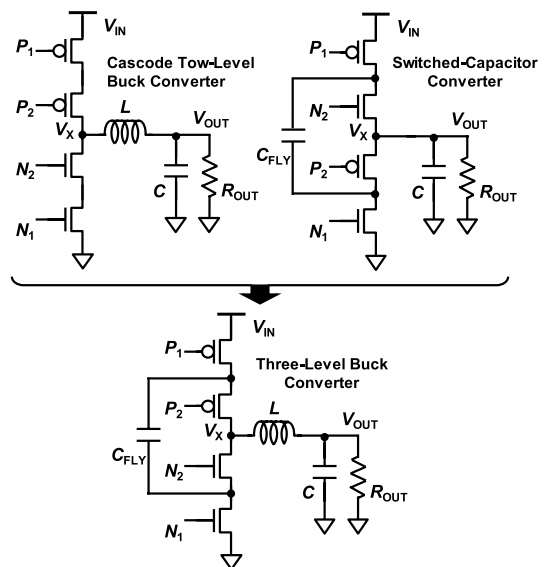


Fig. 1. Power stage and output filters of cascade two-level buck converter, 1/2 switched capacitor DC–DC converter, and three-level buck converter

a smaller inductance and faster transient response than the conventional two-level buck converter at fixed ripples^{(7)–(12)}. A fully integrated three-level buck converter in the continuous conduction mode (CCM) delivering a current of 150 mA with η of 72% for the active mode operation of microprocessors has been reported⁽⁸⁾. The converter, however, cannot be applied to the stand-by mode operation of microprocessors, because η is low at a light load (e.g., < 10 mA) owing

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to the CCM. In IVRs for energy-efficient microprocessors, a high η in the standby mode, as well as the active mode, is required. To achieve a high η at a light load, discontinuous conduction mode (DCM) operation is necessary. However, there have been very few publications about three-level buck converters in the DCM⁽¹²⁾, although a detailed analysis of a three-level buck converter in the CCM was reported⁽¹³⁾⁽¹⁴⁾. A previous study⁽¹²⁾ does not include an analysis on the fundamental circuit characteristics of a three-level buck converter in the DCM, meaning that it is not yet clarified how to design controllers.

To solve this problem, fundamental circuit characteristics, including the conversion ratio and the transfer function, of three-level buck converters in the DCM are analytically derived for the first time⁽¹⁵⁾. In this work, more-detailed explanations on the analysis, as well as experimental validations for the analysis, are shown. In addition, a design of a controller targeting low-power IC applications (typically, the output is a few watts, and the output current is several hundred milliamperes) is shown. In Section 2, the circuit operation of three-level buck converters in the DCM is shown. A detailed derivation of circuit characteristics, including the transfer function, in the DCM is given in Section 3, and, in Section 4, a time-domain small-signal-injection simulation is described that validates the derived results. Also, the experimental validation of the derived transfer function is shown in Section 5. In Section 6, a practical design of a controller considering the transition between the CCM and the DCM for low-power IC applications is discussed. Finally, Section 7 concludes this work.

2. Circuit Operation of Three-level Buck Converters in Discontinuous Conduction Mode

The three-level buck converter in Fig.1 includes four switches (P_1 , P_2 , N_1 , and N_2). As shown in Fig. 2, the three-level buck converter in the DCM has five states (S_A – S_E), instead of the four states (S_A – S_D) in the three-level buck converter in the CCM⁽¹³⁾⁽¹⁴⁾. S_E only exists in the DCM, and the inductor current (I_L) is zero in the S_E state. Figure 3 shows operation waveforms of the voltage in the V_X node and I_L in the three-level buck converter in the DCM. T_S is the duration of one period, and D_1 – D_6 are duty ratios. D_1 , D_2 , and D_3 are assumed to be equal to D_4 , D_5 , and D_6 , respectively. The voltage across the flying capacitor (V_{CFLY}) is assumed to be half of V_{IN} in the case of a sufficiently large C_{FLY} . When the conversion ratio M ($= V_{OUT}/V_{IN}$) is less than 1/2, the state transition order is (S_A , S_B , S_E , S_C , S_B , S_E) as shown in Fig. 3(a). In contrast, when M is more than 1/2, the order is (S_D , S_A , S_E , S_D , S_C , S_E) as shown in Fig. 3(b).

3. Analysis of Circuit Characteristics in Three-level Buck Converters in Discontinuous Conduction Mode

3.1 Analysis of Conversion Ratio The conversion ratio (M) of a three-level buck converter in the DCM is derived by combining the volt-second balance in the inductor voltage (V_L), and the balance of the load current and the averaged I_L .

$$\langle V_L \rangle = 0 \dots\dots\dots (1)$$

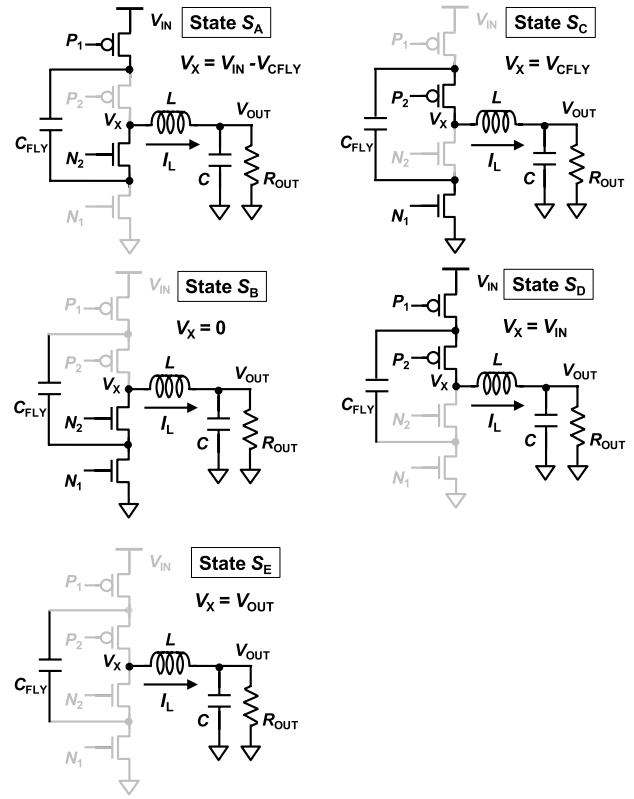


Fig. 2. Five circuit states of three-level buck converters (S_A – S_E)

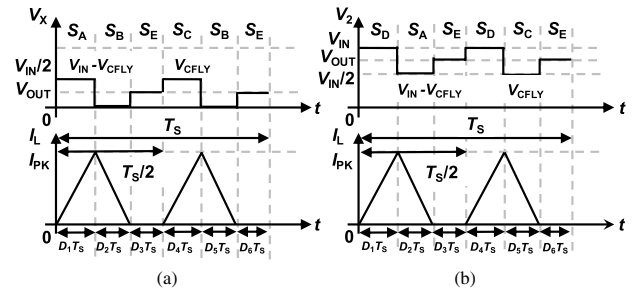


Fig. 3. Switching patterns of three-level buck converter: (a) $M \leq 0.5$ and (b) $M \geq 0.5$

$$\frac{V_{OUT}}{R_{OUT}} = \langle I_L \rangle \dots\dots\dots (2)$$

When $M \leq 0.5$, Eq. (1) is expressed as

$$0 = (V_{IN} - V_{CFLY} - V_{OUT})D_1T_S + (0 - V_{OUT})D_2T_S + 0 \cdot D_3T_S + (V_{CFLY} - V_{OUT})D_4T_S + (0 - V_{OUT})D_5T_S + 0 \cdot D_6T_S \Leftrightarrow \frac{V_{OUT}}{V_{IN}} = \frac{1}{2} \times \frac{D_1}{D_1 + D_2}, \dots\dots\dots (3)$$

and Eq. (2) becomes

$$\frac{V_{OUT}}{R_{OUT}} = \frac{1}{2} I_{PK} (D_1 + D_2) \times 2 = \frac{1}{2} \frac{V_{IN} - V_{OUT}}{L} D_1 (D_1 + D_2) T_S \dots\dots\dots (4)$$

By pairing Eqs. (3) and (4), a quadratic equation for M is acquired,

$$0 = M^2 + \frac{D_1^2}{K} M - \frac{D_1^2}{2K}, \dots\dots\dots (5)$$

where K is defined as

$$K = \frac{2L}{R_{OUT}T_S} \dots \dots \dots (6)$$

By solving Eq. (6), taking the positive sign, M is derived as

$$M = \frac{1}{1 + \sqrt{1 + 2\left(\frac{K}{D_1^2}\right)}} \dots \dots \dots (7)$$

When $M \geq 0.5$, Eqs. (3)–(5), and (7) correspond to (8)–(11), respectively.

$$\frac{V_{OUT}}{V_{IN}} = \frac{D_1 + (D_1 + D_2)}{2(D_1 + D_2)} \dots \dots \dots (8)$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \frac{R_{OUT}T_S}{L} D_1 (D_1 + D_2) \dots \dots \dots (9)$$

$$0 = M^2 - \frac{1}{2} \left(1 - \frac{2D_1^2}{K}\right) M - \frac{D_1^2}{K} \dots \dots \dots (10)$$

$$M = \frac{2}{1 - \frac{K}{2D_1^2} + \sqrt{\left(1 - \frac{K}{2D_1^2}\right)^2 + \frac{4K}{D_1^2}}} \dots \dots \dots (11)$$

Eqs. (7) and (11) are expressed in terms of only the control parameter D_1 and circuit parameters, such as L , T_S , and R_{OUT} .

3.2 Analysis of Transfer Function with Averaged Switch Model

The transfer functions of a three-level buck converter in the DCM are derived by using an averaged switch model of switch networks⁽¹⁶⁾. Figure 4 shows the switch network in a three-level buck converter in the DCM. The voltage and current waveforms corresponding to Fig. 4 are illustrated in Fig. 5. The averaged switch network quantities, $\langle V_1 \rangle$, $\langle V_2 \rangle$, $\langle I_1 \rangle$, and $\langle I_2 \rangle$, are calculated as follows. When $M \leq 0.5$,

$$\begin{cases} \langle V_1 \rangle = V_{IN} \\ \langle V_2 \rangle = V_{OUT} \\ \langle I_1 \rangle = \frac{D_1^2 T_S}{2L} \left(\frac{V_{IN}}{2} - V_{OUT} \right) \\ \langle I_2 \rangle = \frac{D_1^2 T_S}{2L} \cdot \frac{V_{IN}}{V_{OUT}} \left(\frac{V_{IN}}{2} - V_{OUT} \right), \end{cases} \dots \dots \dots (12)$$

and when $M \geq 0.5$,

$$\begin{cases} \langle V_1 \rangle = V_{IN} \\ \langle V_2 \rangle = V_{OUT} \\ \langle I_1 \rangle = \frac{D_1^2 T_S}{L} \frac{V_{OUT} (V_{IN} - V_{OUT})}{2 V_{OUT} - V_{IN}} \\ \langle I_2 \rangle = \frac{D_1^2 T_S}{L} \frac{V_{IN} (V_{IN} - V_{OUT})}{2 V_{OUT} - V_{IN}}. \end{cases} \dots \dots \dots (13)$$

Figure 6 shows the small-signal equivalent circuit of Fig. 4. For small signals, the equivalent circuit is obtained by linearization of the expressions for the averaged switch models. Note that v_1 , v_2 , i_1 , i_2 , and d are small perturbations from $\langle V_1 \rangle$, $\langle V_2 \rangle$, $\langle I_1 \rangle$, $\langle I_2 \rangle$, and D_1 , respectively. The parameters (j_1 , g_1 , r_1 , j_2 , g_2 , and r_2) in Fig. 6 are summarized in Table 1.

From the small-signal equivalent model, a control-to-output transfer function $G_{vd}(s)$ can be found as follows:

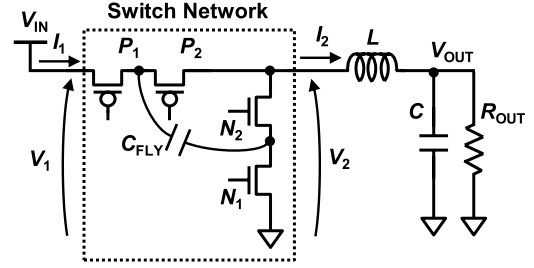


Fig. 4. Three-level buck converter with definition of switch network terminal quantities, V_1 , V_2 , I_1 , and I_2

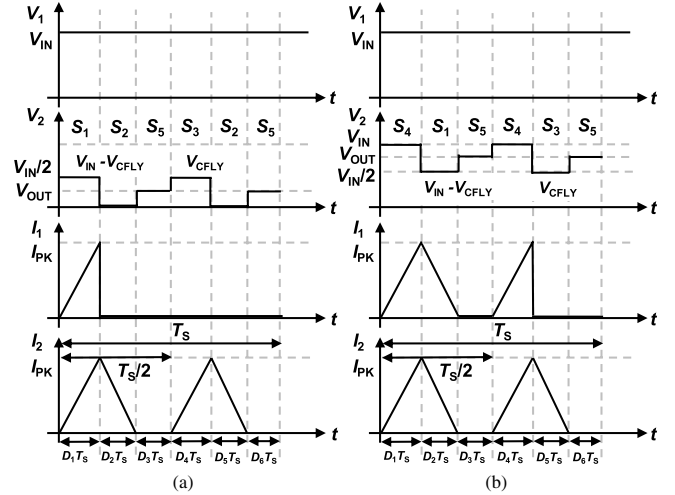


Fig. 5. Voltage and current waveforms of switch network: (a) $M \leq 0.5$ and (b) $M \geq 0.5$

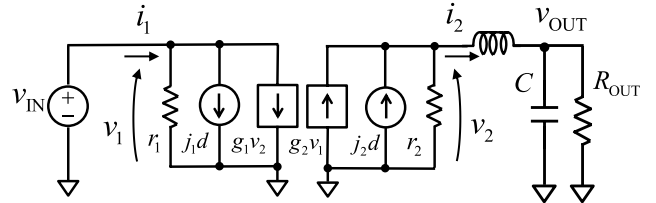


Fig. 6. Small-signal AC models of three-level buck converter in DCM obtained by averaged switch model

$$G_{vd}(s) = \frac{v_{OUT}}{d} \Big|_{v_{IN}=0} = \frac{G_{d0}}{1 + s/\omega_p} \dots \dots \dots (14)$$

$$G_{d0} = j_2(R_{OUT} \parallel r_2) \dots \dots \dots (15)$$

$$\omega_p = \frac{1}{(R_{OUT} \parallel r_2) C} \dots \dots \dots (16)$$

In the equivalent circuit, the inductor is in series with the input current source; thus, the inductor dynamics (particularly at low frequencies) are assumed to be insignificant⁽¹⁶⁾. In Table 2, values of M and the control-to-output transfer function of the two-level⁽¹⁷⁾ and three-level buck converters in the DCM are summarized. For comparison, Table 3 shows values of M and the transfer functions of the two-level⁽¹⁷⁾ and three-level⁽¹³⁾⁽¹⁴⁾ buck converters in the CCM. Similar to conventional two-level buck converters, three-level buck converters in the DCM have a first-order lag transfer function, whereas three-level buck converters in the CCM have a second-order lag transfer function, suggesting that different controllers are required for the DCM and CCM. In the design of a conventional two-level buck converter operating both in the CCM

Table 1. Summary of parameters in Fig. 6

Three-Level Buck Converter	$j_1 \equiv \frac{\partial \langle i_1 \rangle}{\partial D_1}$	$r_1 \equiv 1 / \frac{\partial \langle i_1 \rangle}{\partial V_{IN}}$	$g_1 \equiv -\frac{\partial \langle i_1 \rangle}{\partial V_{OUT}}$	$j_2 \equiv \frac{\partial \langle i_2 \rangle}{\partial D_1}$	$r_2 \equiv -1 / \frac{\partial \langle i_2 \rangle}{\partial V_{OUT}}$	$g_2 \equiv \frac{\partial \langle i_2 \rangle}{\partial V_{IN}}$
$0 \leq M \leq 0.5$	$j_1 = \frac{2D_1 V_{IN}}{KR_{OUT}} \left(\frac{1}{2} - M \right)$	$r_1 = \frac{2KR_{OUT}}{D_1^2}$	$g_1 = \frac{D_1^2}{KR_{OUT}}$	$j_2 = \frac{D_1 V_{IN}}{KR_{OUT}} \cdot \frac{1-2M}{M}$	$r_2 = \frac{2KR_{OUT}}{D_1^2} M^2$	$g_2 = \frac{D_1^2}{KR_{OUT}} \cdot \frac{1-M}{M}$
$0.5 \leq M \leq 1.0$	$j_1 = \frac{2D_1 V_{IN}}{KR_{OUT}} \cdot \frac{2M(1-M)}{2M-1}$	$r_1 = \frac{KR_{OUT}}{2D_1^2} \cdot \frac{(2M-1)^2}{M^2}$	$g_1 = \frac{D_1^2}{KR_{OUT}} \cdot \frac{(2M-1)^2+1}{(2M-1)^2}$	$j_2 = \frac{2D_1 V_{IN}}{KR_{OUT}} \cdot \frac{2(1-M)}{2M-1}$	$r_2 = \frac{KR_{OUT}}{2D_1^2} (2M-1)^2$	$g_2 = \frac{2D_1^2}{KR_{OUT}} \cdot \frac{1-2(M-1)^2}{(2M-1)^2}$

 Table 2. Values of M and control-to-output transfer function $G_{vd}(s)$ of two-level and three-level buck converters in the DCM

	Two-Level DCM Buck Converter ⁽¹⁶⁾	Three-Level DCM Buck Converter (This Work)	
		$M < 0.5$	$M > 0.5$
$M = V_{OUT}/V_{IN}$	$\frac{2}{1 + \sqrt{1 + 4\left(\frac{K}{D_1^2}\right)}}$	$\frac{1}{1 + \sqrt{1 + 2\left(\frac{K}{D_1^2}\right)}}$	$\frac{2}{1 - \frac{K}{2D_1^2} + \sqrt{\left(1 - \frac{K}{2D_1^2}\right)^2 + \frac{4K}{D_1^2}}}$
$G_{vd}(s)$	$G_{d0} \left(1 + \frac{s}{\omega_p} \right)$		
G_{d0}	$\frac{MV_{IN}}{D_1} \cdot \frac{2(1-M)}{2-M}$	$\frac{MV_{IN}}{D_1} \cdot \frac{1-2M}{1-M}$	$\frac{MV_{IN}}{D_1} \cdot \frac{2(1-M)(2M-1)}{1-2(M-1)^2}$
ω_p	$\frac{1}{R_{OUT}C} \cdot \frac{2-M}{(1-M)}$	$\frac{1}{R_{OUT}C} \cdot \frac{2(1-M)}{(1-2M)}$	$\frac{1}{R_{OUT}C} \cdot \frac{1-2(M-1)^2}{(2M-1)(1-M)}$

 Table 3. Values of M and control-to-output transfer function $G_{vd}(s)$ of two-level and three-level buck converters in the CCM

	Two-Level CCM Buck Converter ⁽¹⁷⁾	Three-Level CCM Buck Converter ^(13,14)	
		$M < 0.5$	$M > 0.5$
$M = \frac{V_{OUT}}{V_{IN}}$	D	D_1	$D_1 + \frac{1}{2}$
$G_{vd}(s)$	$G_{d0} \left(1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2} \right)$		
G_{d0}	V_{IN}		
ω_0	$\frac{1}{\sqrt{LC}}$		
Q	$R_{OUT} \sqrt{\frac{C}{L}}$		

for heavy loads (e.g., 100 mA) in the active mode and in the DCM for light loads (e.g., 0.1 mA) in the stand-by mode, the controller must be carefully designed for combined operation in the CCM and the DCM. The proposed model makes possible the design of controllers for three-level buck converters in the DCM.

4. Validation of Derived Transfer Function by Time-Domain Small-signal-injection Simulation

The purpose of the research described in this section was to validate the theoretical analysis presented in Section 3 with the time-domain small signal-injection simulation method ⁽¹⁸⁾.

4.1 Time-domain Small-signal-injection Method

The time-domain small signal-injection simulation method ⁽¹⁸⁾ can be used to find the transfer function in the case of non-resonant switching mode power supply circuits such as

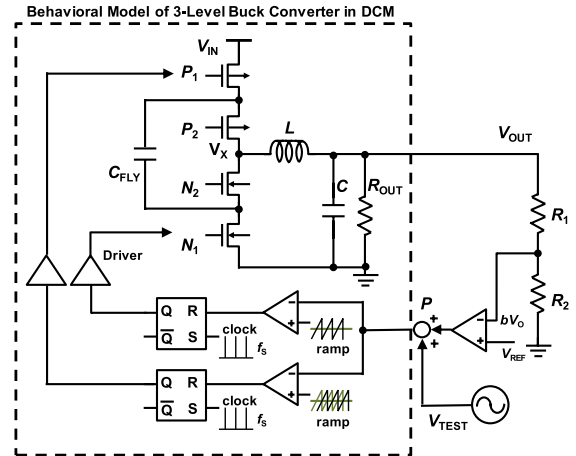
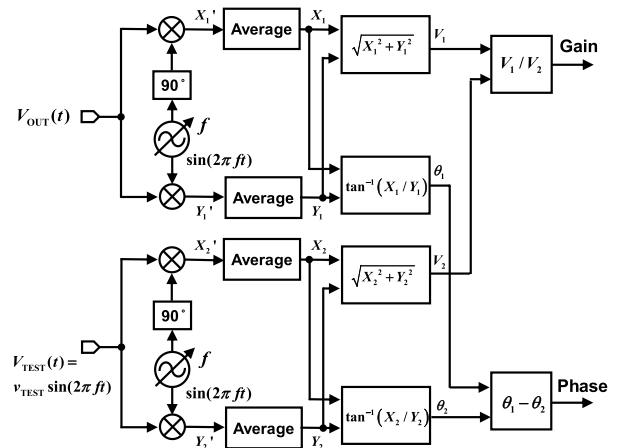


Fig. 7. Time-domain small-signal injection simulation for validation


 Fig. 8. Calculation of the loop gain and phase at a frequency of f

a three-level buck converter. A non-resonant switching mode power supply including a three-level buck converter means that the switching frequency is much faster than the natural frequency of the system.

In this method, the whole loop of the three-level buck converter is broken at the output of the error amplifier, as shown in Fig. 7. Then, a small signal voltage source V_{TEST} whose waveform is sinusoidal with a small magnitude at a given frequency is injected at point P , where the whole loop is broken, as in Fig. 7. The injected small signal V_{TEST} passes through the controller and the power stage and finally reaches the

output voltage V_{OUT} . Reflecting the control-to-output small-signal behavior at a certain frequency point, the final small signal appearing at the output voltage contains a gain in magnitude and a shift in phase with respect to the input small signal. Here, the magnitude of the input small signal should be small enough that the average DC operation point at the periodic steady state does not change, and the output voltage does not saturate with non-linear behavior.

To obtain the transfer function, first, Fourier analysis is performed on the output voltage as illustrated in Fig. 8. Then, a gain of the transfer function at an injected frequency point is

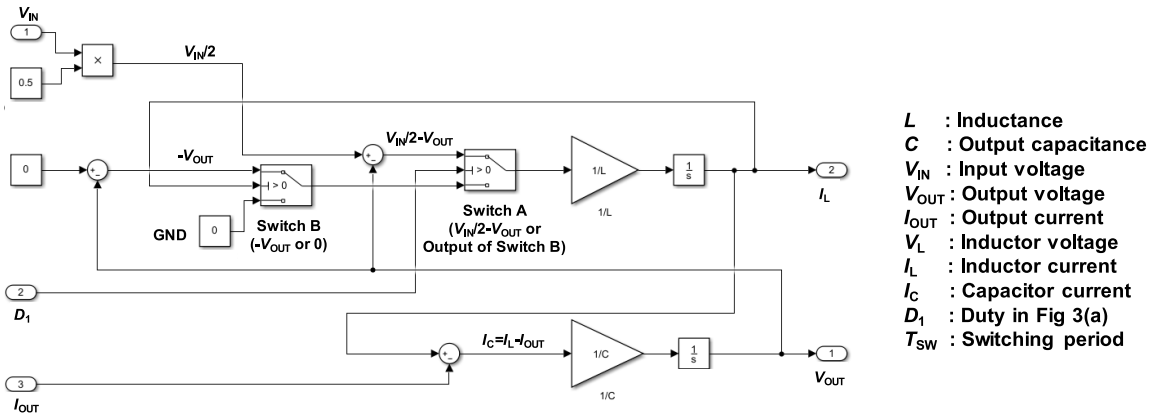
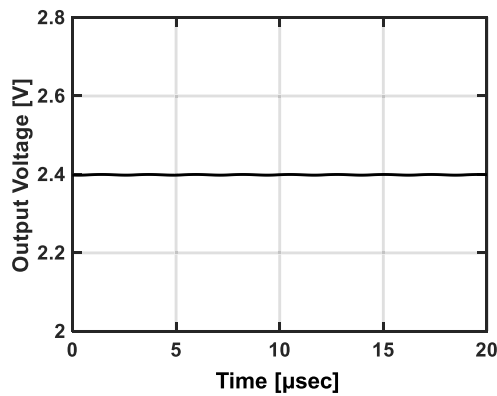
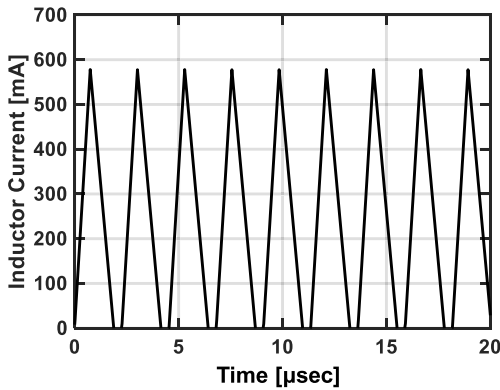


Fig. 9. Idealized behavioral models of three-level buck converter ($M < 0.5$) in Fig. 7 created on MATLAB/Simulink

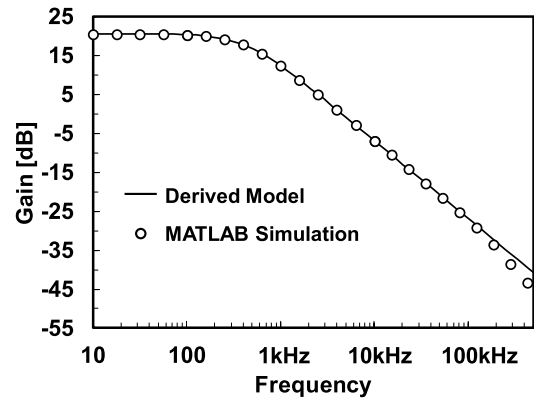


(a)

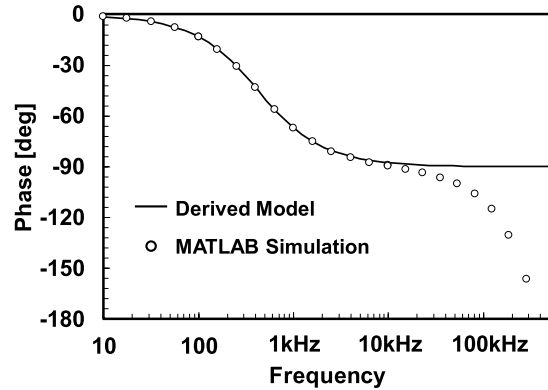


(b)

Fig. 10. Three-level buck converter in DCM steady-state waveform of (a) output voltage and (b) inductor current under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, $D_1 = 0.1661$, $M = 0.20$



(a)



(b)

Fig. 11. Bode plots of derived theoretical model and time-domain simulation results of (a) gain and (b) phase under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, $D_1 = 0.1661$, $M = 0.20$

obtained by dividing the output signal V_1 by the magnitude of the injected input small V_2 . Also, a phase of the transfer function at an injected frequency point is obtained by measuring the output phase θ_1 with respect to the input phase θ_2 . Finally, by sweeping the frequency of the injection small signal f and repeating the Fourier analysis and gain/phase calculation at each frequency point, the entire frequency response of the transfer function is collected⁽¹⁹⁾.

4.2 Simulation Results The derived transfer function was verified by time-domain small-signal-injection simulation, as explained above. Figure 9 shows a behavioral model of a three-level buck converter in DCM constructed on the MATLAB/Simulink platform. The behavioral model simulates the inductor current I_L and the output voltage V_{OUT} based on the operation of a three-level buck converter when $V_{OUT} > V_{IN}/2$, as shown in Fig. 3(a). The detail of the model is as follows. The ideal switch A and switch B in the model play a condition branch role. Switch A controls the voltage applied across the inductor based on the duty ratio D_1 . During the period given by $D_1 T_{SW}$, switch A determines one state in which a voltage $V_{IN}/2 - V_{OUT}$ is applied across the inductor and increases the inductor current. After the period of $D_1 T_{SW}$, switch A changes to the other state controlled by switch B. In the other state, initially, a voltage $-V_{OUT}$ is applied to decrease the current. Once the inductor current reaches zero when $t = (D_1 + D_2) T_{SW}$, the voltage across the inductor becomes zero. Depending on whether the inductor current is zero, switch B controls the voltage across the inductor, $-V_{OUT}$ or 0. This process is repeated with a given switching period T_{SW} . D_1 , D_2 , and D_3 are assumed to be equal to D_4 , D_5 , and D_6 , respectively in Fig. 3(a).

Figure 10 shows waveforms of the output voltage and inductor current in the behavioral simulation under the conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, and $V_{OUT} = 2.4$ V. D_1 is 0.1661 to achieve a voltage conversion ratio $M = V_{IN}/V_{OUT} = 0.20$ according to Eq. (7).

Figure 11 shows Bode plots of the derived transfer function in Table 2 and simulation results under the same conditions. The Bode plot of the derived transfer function is consistent with that of the simulated results at least approximately one-third of the switching frequency, which indicates the validity of the derived transfer function of the three-level buck converter in the DCM. The discrepancy in the high-frequency region near the switching frequency is caused by the dynamics of the inductor in DCM, which is not considered by the averaged switch model of switch networks⁽¹⁶⁾ discussed in Section 4. The high-frequency behavior can be accurately captured by more-complicated analysis⁽²⁰⁾, even for the three-level buck converter in the DCM. However, the analysis is sufficient in terms of compensator designs, because a loop bandwidth with a compensator becomes much lower than the high-frequency pole because of the inductor dynamics, as is discussed in Section 6.

5. Experimental Validation of Derived Transfer Function

5.1 Prototype of Three-level Buck Converter in DCM

A three-level buck converter in DCM was designed combining with off-the-shelf discrete ICs for experimental

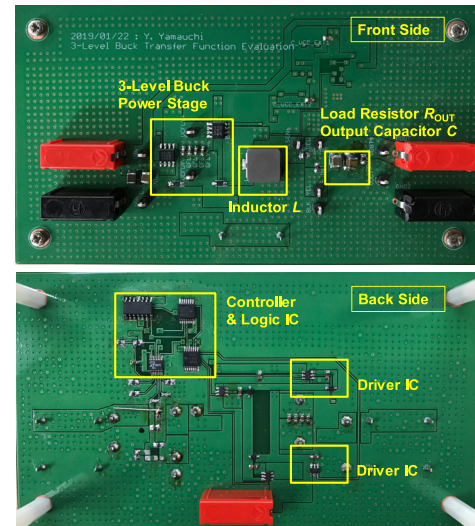


Fig. 12. Prototype of three-level buck converter in the DCM using off-the-shelf ICs

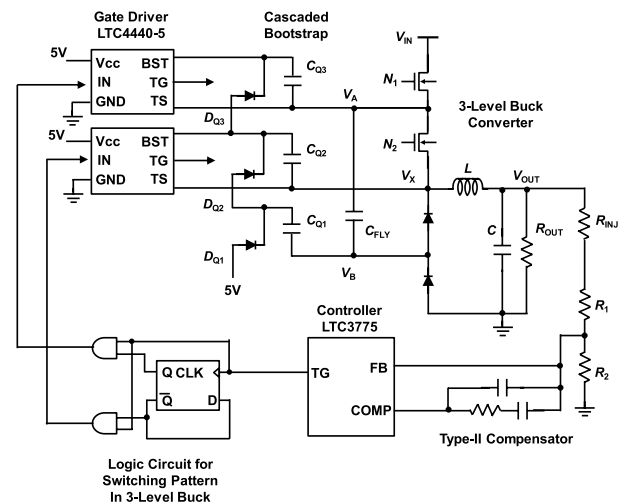


Fig. 13. Detailed implementation of gate driver, switching pattern generation, and controller in the prototype of three-level buck converter in the DCM using off-the-shelf ICs

validation, as shown in Fig. 12. Asynchronous rectification was employed using two diodes in the low side for simplicity while a control method maintaining the DCM operation with all metal-oxide-semiconductor field-effect transistors (MOSFETs) was utilized⁽²¹⁾. Also, in this prototype, a voltage-mode controller with a type-II compensator was employed for stable voltage control. Logic circuits⁽²²⁾, illustrated in Fig. 13, were used to generate gate signal patterns for the three-level buck converter with conventional buck converter controller IC. The circuit in Fig. 13 also employed a cascaded bootstrap scheme⁽²³⁾ in the three-level buck converter. Because the top-two MOSFETs were floating switches, the bootstrap capacitors were needed for their gate drivers. Bootstrap diode D_{Q1} , D_{Q2} , and bootstrap capacitor C_{Q1} were used for charging a voltage across C_{Q2} . Also, bootstrap diode D_{Q3} and bootstrap capacitor C_{Q2} charged the voltage across C_{Q3} so that the bootstrap circuit worked as a whole.

Figure 14 shows the measured waveforms of the output voltage and inductor current in the prototype three-level buck

converter under the conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, and $V_{OUT} = 2.4$ V. The inductor current I_L was in DCM, and the V_B node voltage swung between $V_{IN}/2$ ($= 6$ V) and 0. These waveforms suggest that the prototype circuit operates properly as a three-level buck converter in DCM for experimental validation of the transfer function. In this measurement, a 500 m Ω shunt resistor was used to sense the inductor current.

5.2 Measurement Setup The measurement setup for the experimental validation of the transfer function is shown in Fig. 15. A frequency response analyzer, FRA5097, was employed to measure the transfer function experimentally. The oscillator of the FRA5097 was inserted through the injected resistance R_{INJ} (50 Ω), which was connected between the output node and the output voltage divider⁽²⁴⁾. The injected resistance was much smaller than the voltage dividing resistances, so it can be assumed that the injected resistor did not affect the transfer function. Also, in this measurement setup, the open-loop gain as a whole was measured, meaning

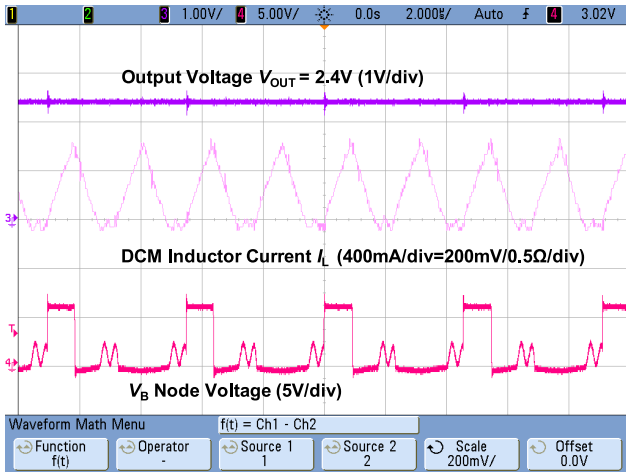


Fig. 14. Steady state waveforms of the prototype three-level buck converter in the DCM under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C_{OUT} = 100$ μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, $V_{OUT} = 2.4$ V

not only the control-to-output characteristic, but also characteristics of the compensator, ramp generator, and voltage divider were included. Hence, they had to be subtracted later from the open-loop transfer function after characterizing individually the transfer function of the parts, except for the control-to-output.

5.3 Measurement Results Figures 16 and 17 show the Bode plots of the open-loop transfer function, the compensator transfer function, and the control-to-output transfer function for the condition described in Section 5.1. Because the open loop transfer function is a product of the compensator plant transfer function and compensator transfer function in the s -domain, the gain of the control-to-output transfer function—Figs. 16(c) and 17(c)—was obtained by subtracting the gain of the compensator transfer function—Figs. 16(b) and 17(b)—from the gain of the open-loop transfer function—Figs. 16(a) and 17(a). In Figs. 16(c) and 17(c), the experimental results for the gain of the control-to-output transfer function were -20 dB/dec after the cutoff frequency, 595 Hz for $C = 100$ μ F, $V_{IN} = 12$ V and 295 Hz for $C = 200$ μ F, $V_{IN} = 14$ V. They agree with the analytically derived transfer function in Eq. (14) and experimentally verify the derived model for the transfer function of the three-level buck converter in DCM.

6. Discussion on Compensator Design for Three-level Buck Converter Covering both DCM and CCM

Because the control-to-output transfer function of the three-level buck converter in the DCM was analyzed and validated, here, the compensator design for the three-level buck converter across DCM and CCM was investigated, particularly for low-power IC application, with simulations. A typical output power was assumed to be less than 1 W, and a typical output current was assumed to be less than several hundred milliamperes. As was shown, the transfer function of the three-level buck converters in the DCM has the same form as the conventional buck converter in the DCM, which is a first-order lag function. However, the three-level and

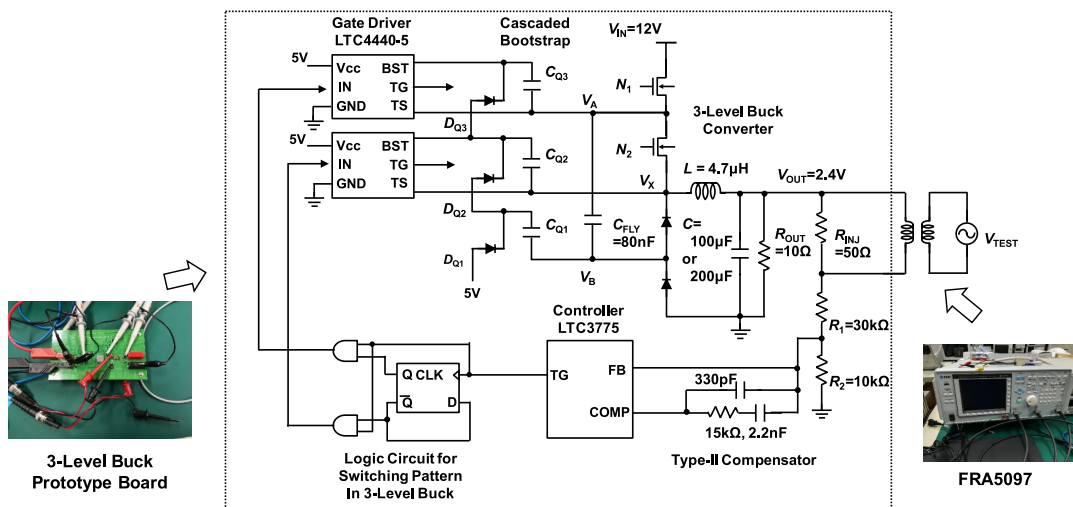


Fig. 15. Measurement setup for the experimental validation of the transfer function with use of frequency response analyzer FRA5097 at $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F or 200 μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, $V_{OUT} = 2.4$ V

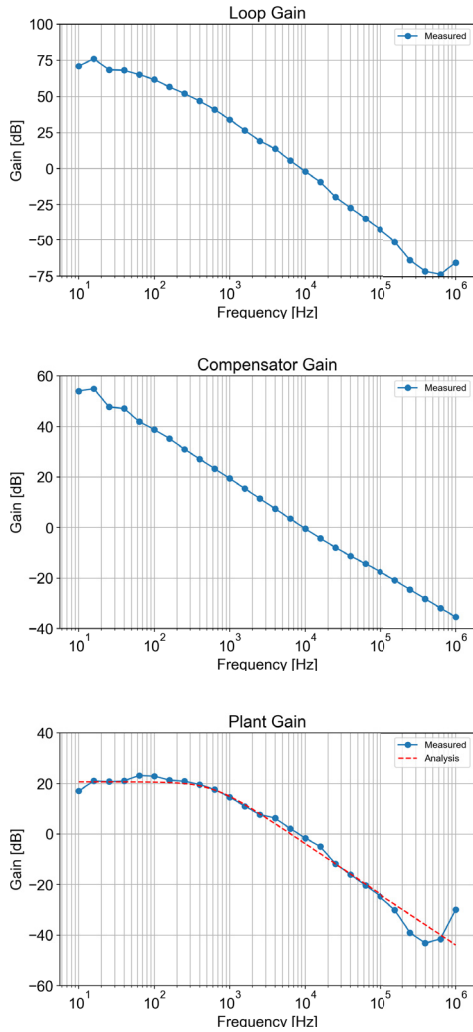


Fig. 16. Measurement results of transfer function in the prototype of three-level buck converter in DCM (a) loop gain (b) compensator gain, and (c) control-to-output gain under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 12$ V, $V_{OUT} = 2.4$ V

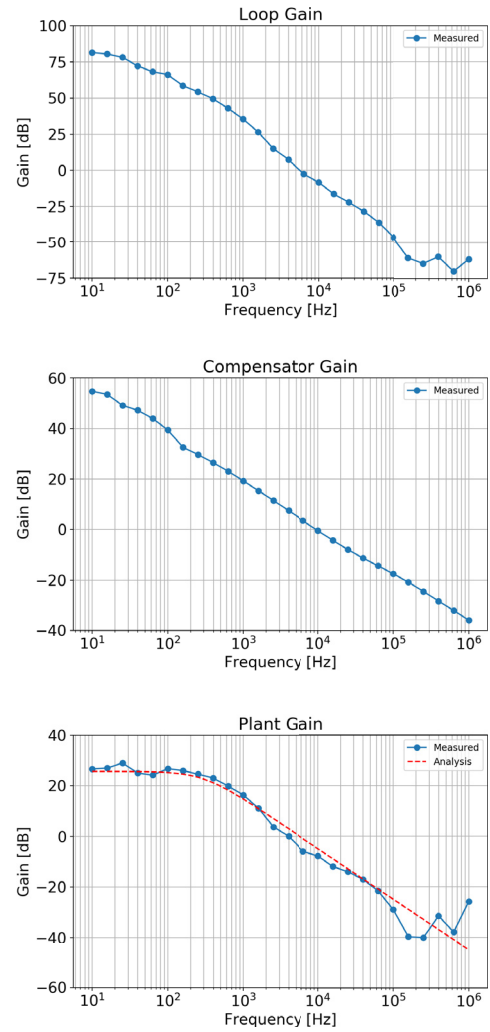


Fig. 17. Measurement results of transfer function in the prototype of three-level buck converter in DCM (a) loop gain (b) compensator gain, and (c) control-to-output gain under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 200$ μ F, $C_{FLY} = 80$ μ F, $R_{OUT} = 10$ Ω , $V_{IN} = 14$ V, $V_{OUT} = 2.4$ V

conventional buck converters have a second-order lag function in CCM. This drastic change in dynamics depending on the CCM or DCM is illustrated in Fig. 18. When I_{OUT} is less than 300 mA, the three-level buck converter operates in DCM. In contrast, when I_{OUT} is more than 500 mA, the three-level buck converter operates in CCM. To cover a wide range of I_{OUT} , a controller to manage both DCM and CCM is required. The design methodology of the controller for the three-level buck converter is the same as that for the conventional buck converter, because both converters have the same-order lag function.

In high output-power DC–DC converters (e.g. output power $P_{OUT} > 2.5$ –800 W), it is easy to employ digital control techniques, because the power overhead of the digital controller is negligible.

Many of excellent digital control techniques to cope with the significant change in the converter dynamics between CCM and DCM have been proposed including the adaptive tuning method⁽²⁵⁾ at $P_{OUT} > 2.5$ W, predictive nonlinear observer for state estimation⁽²⁶⁾ at $P_{OUT} > 800$ W, mode

estimation without current sensor⁽²⁷⁾ at $P_{OUT} > 75$ W, and current-mode controller with two correction factors⁽²⁸⁾ at $P_{OUT} > 20$ W.

In contrast, in the low-output-power DC–DC converters (e.g., output power $P_{OUT} < 1$ W), it is difficult to use the digital control scheme, because the power overhead of the digital controller causes the efficiency of the DC–DC converter to degrade. For example, one can suppose the case of the three-level buck converter, in which $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C_{FLY} = 80$ μ F, $I_{OUT} = 100$ to 500 mA, $V_{IN} = 12$ V, and $V_{OUT} = 2.4$ V. If the requirement for the analog-to-digital converter (ADC) is 12-bit, and 5-MHz sampling, the power consumption by the ADC is typically approximately 100 mW (ADC12081⁽²⁹⁾, ADS803⁽³⁰⁾). This degrades the efficiency of the DC–DC converter by 30% at low output current (~ 100 mA) only because of the ADC power consumption. Therefore, usually analog voltage-mode control without the ADC is used for low output-power DC–DC converters^{(31)–(35)}.

When the converter operates only in CCM, it is common to use a type-III compensator^{(31)–(33)(35)}, as shown in Fig. 19. The

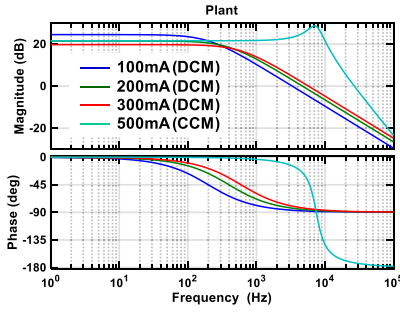


Fig. 18. Duty-to-output transfer function of three-level buck converter under conditions of $f_{SW} = 220$ kHz, $L = 4.7$ μ H, $C = 100$ μ F, $I_{OUT} = 100$ mA, 200 mA, 300 mA, 500 mA, $V_{IN} = 12$ V, $V_{OUT} = 2.4$ V

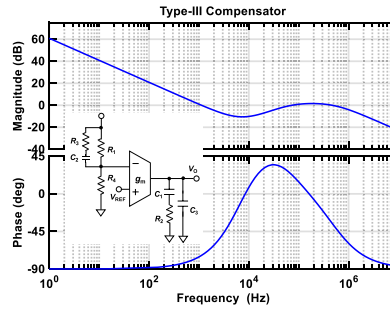


Fig. 19. Type-III Compensator with OTA: $V_o(s)/V_i(s) = \omega_0(1+s/\omega_{z1}) \cdot (1+s/\omega_{z2})/[s \cdot (1+s/\omega_{p1}) \cdot (1+s/\omega_{p2})]$, $\omega_0 = R_4/(R_1+R_4) \cdot g_m/(C_1+C_3) = 2\pi \cdot 1.1$ kHz, $\omega_{p1} = 1/R_2(1/C_1+1/C_3) = 2\pi \cdot 66$ kHz, $\omega_{p2} = 1/[(R_4R_1)/(R_4+R_1)+R_3]C_2 = 2\pi \cdot 530$ kHz, $\omega_{z1} = 1/[(R_1+R_3)C_2] = 2\pi \cdot 7.34$ kHz, $\omega_{z2} = 1/(R_2C_1) = 2\pi \cdot 7.34$ kHz

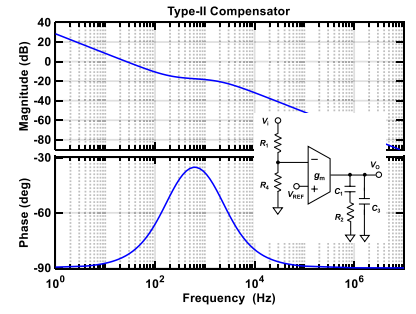


Fig. 20. Type-II compensator with OTA: $V_o(s)/V_i(s) = \omega_0(1+s/\omega_z)/[s \cdot (1+s/\omega_p)]$, $\omega_z = 1/(R_2C_1) = 2\pi \cdot 198$ Hz, $\omega_0 = R_4/(R_1+ssR_4) \cdot g_m/(C_1+C_3) = 2\pi \cdot 26.3$ Hz, $\omega_p = (C_1+C_3)/(R_2C_1C_3) = 2\pi \cdot 1.97$ kHz

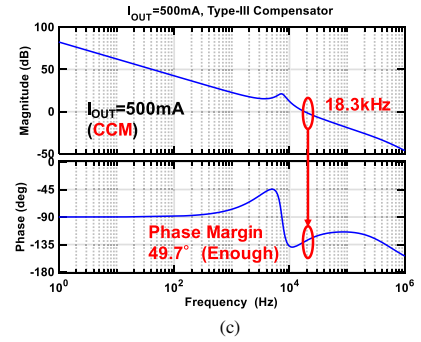
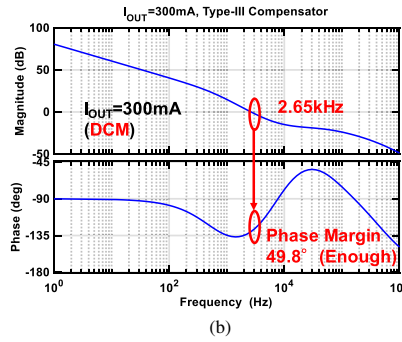
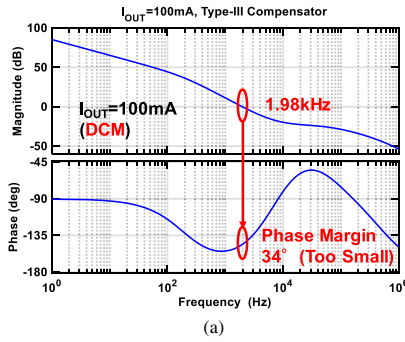


Fig. 21. Loop gain in three-level buck converter with type-III compensator (a) $I_{OUT} = 100$ mA (DCM), (b) $I_{OUT} = 200$ mA (DCM), and (c) $I_{OUT} = 500$ mA (CCM)

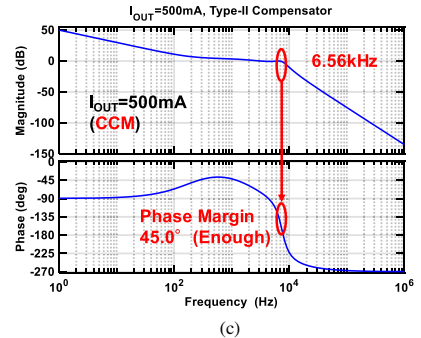
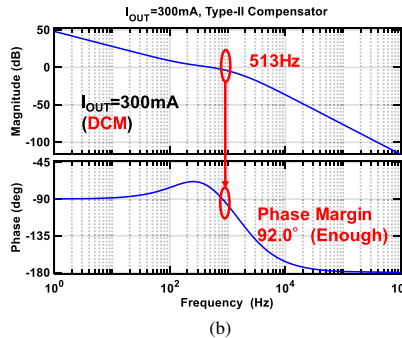
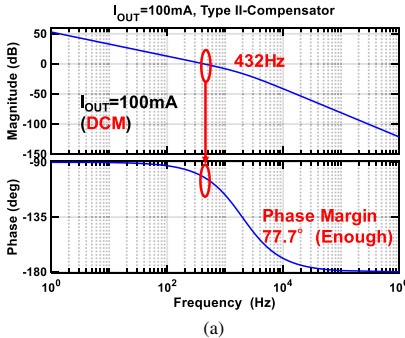


Fig. 22. Loop gain in three-level buck converter with type-II compensator (a) $I_{OUT} = 100$ mA (DCM), (b) $I_{OUT} = 200$ mA (DCM), and (c) $I_{OUT} = 500$ mA (CCM)

design parameters are shown in the figure caption of Fig. 19. The design scheme for the controller is as follows⁽³¹⁾⁻⁽³³⁾⁽³⁵⁾: two zeros are placed to cancel the double pole in the CCM transfer function. One pole is set at several times higher than unity gain frequency, and the higher-frequency pole is placed at the zero created by ESR of the output capacitor, to widen the control loop bandwidth, as in Fig. 21(c). However, if the same controller is used for the DCM operation as well, the control loop suffers from less phase margin as the output current decreases as shown in Figs. 21(a) and (b). This is because the pole frequency in the control-to-duty transfer function of the three-level buck converter in the DCM moves to the lower side as the output current decreases.

Hence, to ensure the stability for both CCM and DCM with the analog control scheme, it is necessary to use the type-II compensator⁽³⁴⁾⁽³⁵⁾ shown in Fig. 20, consisting of one integrator, one pole, and one zero at the expense of the control bandwidth. The design parameters are shown in the figure caption of Fig. 20. The design scheme for the controller is as follows⁽³⁴⁾⁽³⁵⁾: the zero in the type-II compensator is placed at the lowest pole frequency of the control-to-duty transfer function of the three-level buck converter in the DCM with the lowest output current, to cancel each other. Still, there is one degree of freedom in the location of the one pole in the type-II compensator. This pole can be placed at the higher frequency, keeping the stability of the control loop in DCM,

as in Figs. 22(a) and (b). However, if the pole is located at a higher frequency than the resonant frequency of the output LC filter in the three-level buck converter, the control loop becomes unstable in CCM operation. Therefore, the pole is placed at 0.2 times the resonant frequency, so that the phase margin, even in CCM, can be maintained at 45° , as in Fig. 22(c). In this way, the analog voltage-mode controller for the low-output-power DC-DC converters ($P_{OUT} < 1\text{ W}$) is designed.

7. Conclusion

The modeling of three-level buck converters in the DCM was conducted. The transfer function was derived analytically by using an averaged switch model and verified by time-domain small-signal-injection simulations, as well as experimental measurements using a prototype of the three-level buck converter in DCM with off-the-shelf ICs. It was revealed that, similar to conventional two-level buck converters in the DCM, three-level buck converters in the DCM have a first-order lag transfer function, while three-level buck converters in CCM have a second-order lag transfer function. Hence, a controller strategy for a conventional two-level buck converter in the DCM can be applied for three-level buck converter operation both in the DCM and the CCM, was discussed in terms of low-power application.

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