48V-to-12V Dual-Path Hybrid DC-DC Converter

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***Abstract*—A dual-path hybrid DC-DC converter with the step-down ratio of less than half is proposed for the first time. In the proposed converter, the efficiency is higher than a conventional buck converter, because the output current is divided into inductor- and capacitor-path and the conduction loss due to ESR of the inductor is reduced. In the measurement, the peak efficiency of the proposed dual-path hybrid and conventional buck converters was 97.1% and 96.0% at 120W, 48V-to-12V conversion, respectively, indicating the loss is reduced by 28.4 %. Furthermore, the efficiency of the proposed and conventional converters was 95.8% and 94.8% at 240W, respectively, indicating the loss is reduced by 30.0 %.**

Keywords—DC-DC converter, Step-down converter, Hybrid Converter, Dual-path, Series Equivalent resistance (ESR)

I. Introduction

Hybrid step-down DC-DC converters [1–12] combining a buck converter and a switched capacitor DC-DC converter could overcome the trade-off between the efficiency and the form factor of the commonly used buck converter. Compared with the conventional buck converter, the hybrid step-down DC-DC converters, reducing the inductor voltage amplitude by employing flying capacitors, have advantages, particularly effective for high input voltage and high step-down ratio applications, as follows.

1) Reduced voltage rating for switches: On-resistance per unit area in power MOSFETs increases rapidly as voltage tolerance becomes higher. For example, the drift resistance is roughly proportional to the voltage tolerance to the power of 2.5 [13]. As a result, the heavy dependence on voltage tolerance can make attractive the usage of multiple MOSFETs with low voltage ratings in series, rather than just one MOSFET with high voltage rating, considering to minimize the area for power devices.

2) Smaller inductance for a given current ripple: In case of a three-level buck converter, as an example of the hybrid buck converter, the peak inductor current ripple can be only 1/4 with the same output *LC* value and switching frequency [12], which can mean a significant reduction in inductance. This feature in the hybrid DC-DC is useful because the inductor in a conventional buck converter with high voltage and high step down ratio tends to be bulky and occupy a large portion of the entire volume [14].

3) Larger duty ratio for a given step-down ratio: The conventional buck converters with high frequency and high step-down ratio suffer from controlling narrow turn-on signals, because of switching noises and delays in controller circuits [15]. On the other hand, the duty ratio in hybrid DC-DC converters can be multiple times larger than in the conventional buck converter, for example, doubled in three-level buck converter, for a given conversion ratio. The widened duty ratio makes hybrid DC-DC converters suitable for high frequency and high step-down ratio operation.

In addition, [16–18] reported unique hybrid step-down DC-DC converters, where an inductor is indirectly connected to the output and the output current is divided into a dual-path (inductor and capacitor path) unlike the conventional buck converter and hybrid converters [1–12]. Hence, the converters [16–18] can reduce the conduction loss due to the ESR of the inductor, which is quite beneficial when the inductor loss dominates. The step-down ratio in [16–18] with two circuit states, however, is limited to more than half, thereby they cannot support numerous applications such as bus converters and point of load regulators where the sub-half step-down ratio (e.g. 48V-to-12V, 12V-to-1V, etc.) is required. Although a modification in the hybrid step-down converter with reduced inductor current to include the sub-half conversion ratio is proposed in [18], it employs three states in switching operation. Because the three-state operation causes higher complexity and prevents a simple controller design, the usual two-state operation in the hybrid step-down converter which can output less than half of the input voltage is preferable.

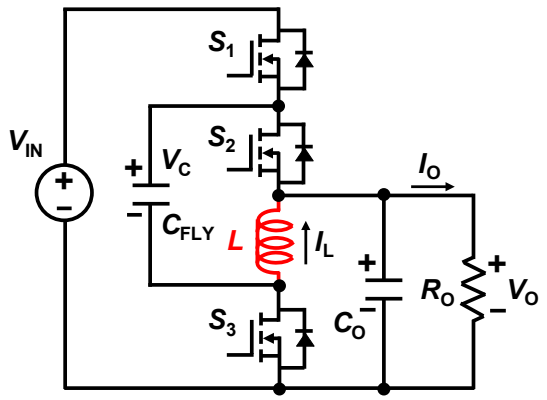
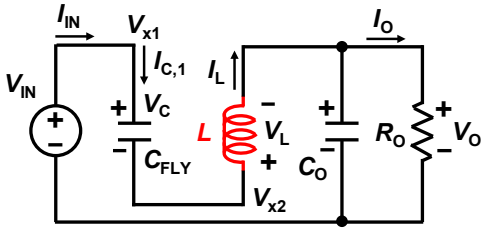


Fig. 1. Proposed dual-path hybrid DC-DC converter.

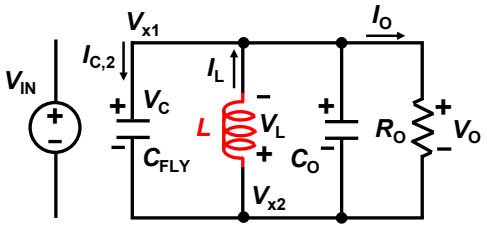
To solve the problem, a novel topology of a dual-path hybrid DC-DC converter with only two states and the step-down ratio of less than half is proposed for the first time. The proposed converter has a high step-down ratio with the advantages of 1) − 3) in the hybrid buck converter and reduced inductor current. Operation principle and basic characteristics of the novel topology such as conversion ratio, inductor current, and flying capacitor current are described analytically in detail. Also, the measurement results of the proposed converter including key waveforms, efficiency, as well as experimental comparison with a conventional buck converter using prototypes are shown.

II. Proposed Dual-Path Hybrid Converter

Fig. 1 shows the proposed dual-path hybrid DC-DC converter topology. As shown in Figs. 2 (a) and (b), the converter has two circuit states. While flying capacitor C_{FLY} is connected to inductor L in series in mode 1, C_{FLY} is in parallel with L in mode 2. Fig. 3 shows key operation waveforms in the proposed converter. By considering voltage-second balance in L, charge balance in C_{FLY} at periodic steady state,



(a) Mode 1



(b) Mode 2

Fig. 2. Two circuit states in the proposed dual-path hybrid converter.

the voltage conversion ratio M of the proposed converter can be shown as follows:

$$\begin{aligned} 0 &= \langle V_L \rangle \\ &= (V_{IN} - V_{CFLY} - V_O) DT_S + (0 - V_O)(1-D)T_S \\ &= (V_{IN} - 2V_O) DT_S - V_O (1-D) T_S \\ \Leftrightarrow \frac{V_O}{V_{IN}} &= \frac{D}{1+D} \end{aligned} \tag{1}$$

$$M = \frac{V_O}{V_{IN}} = \frac{D}{1+D} \tag{2}$$

where, V_L, V_O, V_{IN}, V_{CFLY}, $\langle V_L \rangle$, T_S and D are inductor voltage, output voltage, input voltage, flying capacitor voltage, the average of inductor voltage, switching period, and duty cycle, respectively. Fig. 4 illustrates M as a function of D in the proposed circuit in contrast with the conventional buck converter.

III. Inductor Current Analysis

A. DC current in inductor

As shown in Fig. 2 (b), the DC inductor current in the proposed circuit $I_{L,hybrid}$ can be expressed as follows:

$$I_{L,hybrid} = DI_{IN} + (1-D)(I_{C,2} + I_O), \tag{3}$$

where, I_{IN}, I_O, and $I_{C,2}$ are input current, output current and flying capacitor current in mode 2, respectively. By applying the charge balance in C_{FLY} at periodic steady-state, $I_{C,2}$ can be expressed in terms of I_{IN} as follows:

$$\begin{aligned} 0 &= \langle I_C \rangle \\ &= DI_{C,1} + (1-D) I_{C,2} \\ &= DI_{IN} + (1-D) I_{C,2} \\ \Leftrightarrow I_{C,2} &= -\frac{D}{1-D} I_{IN} \end{aligned} \tag{4}$$

where $\langle I_C \rangle$ is the average of flying capacitor current.

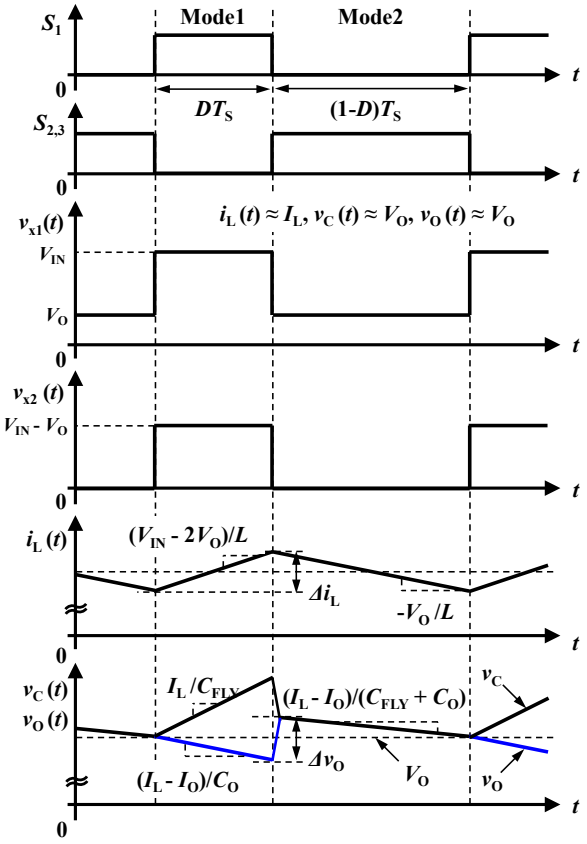


Fig. 3. Circuit operation of the proposed dual-path hybrid converter.

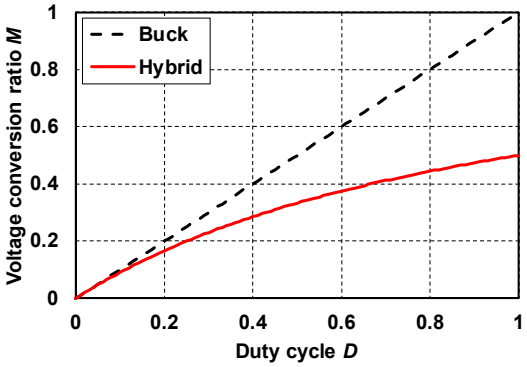


Fig. 4. Voltage conversion ratio M vs. duty cycle D.

By combining (3) and (4),

$$\begin{aligned} I_{L,hybrid} &= DI_{IN} + (1-D)\left(-\frac{D}{1-D} I_{IN} + I_O\right) \\ &= (1-D) I_O \end{aligned} \tag{5}$$

On the other hand, the DC inductor current in buck converter $I_{L,buck}$ is

$$I_{L,buck} = I_O \tag{6}$$

From (2), (5) and (6), the DC inductor current in the proposed circuit $I_{L,hybrid}$ can be reduced thanks to the

contribution of C_{FLY} to the output current in mode 2, as compared with the DC inductor current in buck converter $I_{L,buck}$ as follows:

$$K = \frac{I_{L,hybrid}}{I_{L,buck}} = 1 - D = \frac{1-2M}{1-M} \tag{7}$$

B. Ripple current in inductor

In addition, since the voltage applied to the inductor L is reduced thanks to the flying capacitor C_{FLY}, the inductor current ripple in the proposed converter $\Delta I_{L,hybrid}$ can be reduced compared with the inductor current ripple in the buck converter $\Delta I_{L,buck}$ as follows.

$\Delta I_{L,hybrid}$ can be expressed as follows considering the change in mode 1,

$$\begin{aligned}\Delta I_{L,hybrid} &= (V_{IN} - V_{CFLY} - V_O) D \frac{T_S}{L} \\ &= (V_{IN} - 2V_O) D \frac{T_S}{L} \\ &= V_{IN}(1-2M) D \frac{T_S}{L} \\ &= V_{IN}(1-2M) \frac{M}{1-M} \frac{T_S}{L} \\ &= V_{IN} \frac{M(1-2M)}{1-M} \frac{T_S}{L}\end{aligned} \tag{8}$$

Similarly, $\Delta I_{L,hybrid}$ can be also described,

$$\begin{aligned}\Delta I_{L,buck} &= (V_{IN} - V_O) D \frac{T_S}{L} \\ &= V_{IN}(1-M) M \frac{T_S}{L}\end{aligned} \tag{9}$$

By combining (8) and (9),

$$K_{ripple} = \frac{\Delta I_{L,hybrid}}{\Delta I_{L,buck}} = \frac{1-2M}{(1-M)^2} \tag{10}$$

Fig. 5 shows the inductor DC current ratio K and inductor current ripple ratio K_{ripple} vs. voltage conversion ratio M.

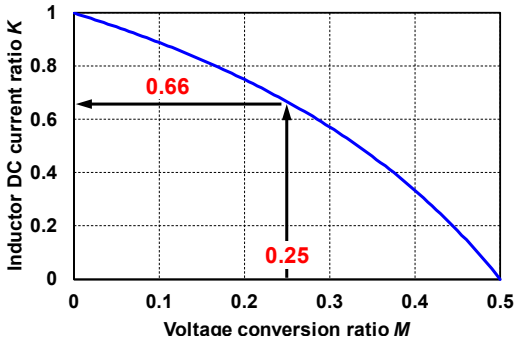
In the 48V-to-12V operation, K equals to 0.66 and K_{ripple} is given to 0.25, respectively. As a result, the proposed dual-path hybrid converter can reduce the inductor DC current by 33.3% and inductor current ripple by 12.2% compared to the conventional buck converter. This not only reduces the conduction current loss due to the equivalent series resistance of the inductor, but also helps reduce the core loss of the inductor.

IV. Experimental Verification

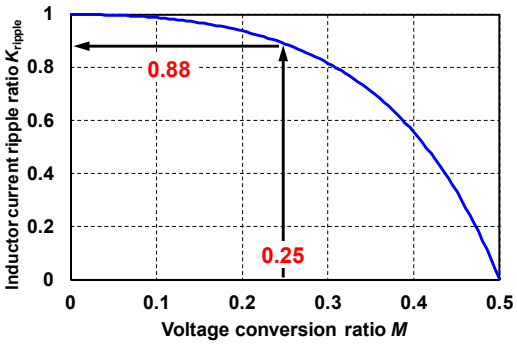
A. Experimental Setup

In order to provide a proof of concept for the dual-path hybrid topology at 48V-to-12V conversion, the proposed dual-path hybrid converter and the conventional buck converter were fabricated and measured for comparison.

Fig. 6 shows the circuit topology of the prototype converter. This circuit includes the proposed dual-path hybrid and conventional buck topologies. As shown in Fig. 6 (b), the proposed dual-path hybrid converter is composed of $S_{1\text{-}3}$, C_{FLY}, C_O, and L. Then, $S_{1\text{-}3}$ are operated as in Fig. 2 and the additional switch S_{buck} does not work in the proposed dual-path hybrid operation.



(a) Inductor DC current ratio K vs. voltage conversion ratio M



(b) Inductor current ripple ratio K_{ripple} vs. voltage conversion ratio M

Fig. 5. Comparison of inductor current between proposed dual-path hybrid converter and conventional buck converter.

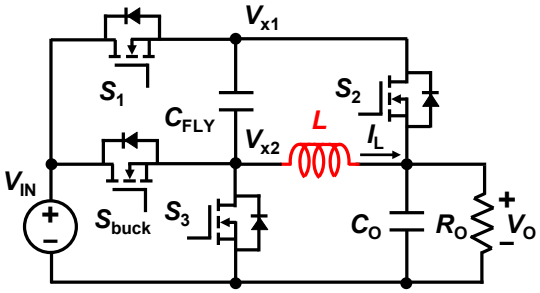
Fig. 6 (c) shows the conventional buck converter topology and it consists of S_{buck}, S_3, C_O, and L. Then, to prevent current from flowing into C_{FLY} through the freewheel diode in S_2, C_{FLY} is disconnected from the V_{x1} node in the buck operation. The switches S_{buck}, S_3 are in a synchronous rectification mode and are always operated in the continuous current mode.

Fig. 7 displays the prototype converter with key components highlighted. This converter was implemented on the 116.8mm x 61mm 2-layer PCB. The proposed dual-path hybrid topology was placed on the upper side and the conventional buck topology was implemented on the lower side. The screw terminals are attached to insert current probes of an oscilloscope. Each gate drive signal is given by an externally connected DSP (PE-PRO/F28335A, Myway-Plus), and the connection is changed by selecting the MOSFET to be used for the proposed dual-path hybrid and conventional buck operations.

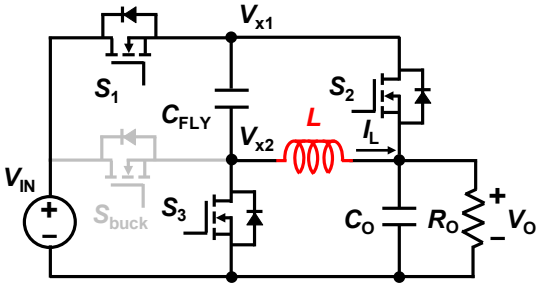
The circuit components and parameters are indicated in TABLE I. Each element and parameter is selected based on the reference design of 48V-to-12V synchronous buck converter (PMP6680, Texas instruments). Since the voltage applied to C_{FLY} and C_O is the same in the proposed circuit, the same elements were used in this design. However, the design method of C_{FLY} is extremely important because it can affect efficiency, responsiveness and stability. Therefore, the design method of C_{FLY} according to the theoretical analysis is an important future work and will be presented.

B. Operation Waveforms

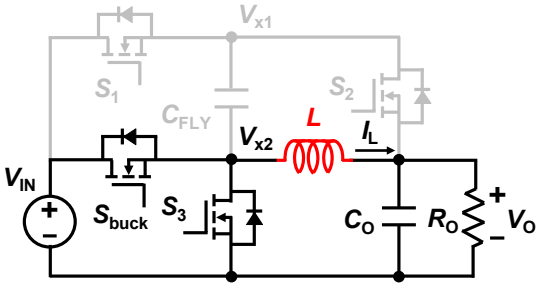
The experimental waveforms at full load condition (I_O = 20A) are shown in Fig. 8. They are measured by an



(a) Whole circuit topology



(b) Proposed dual-path hybrid topology



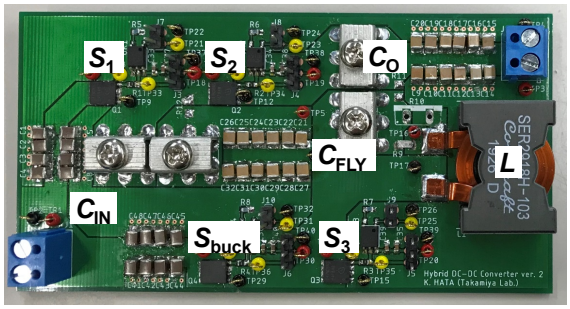
(c) Conventional buck topology

Fig. 6. Circuit topology of prototype converter.

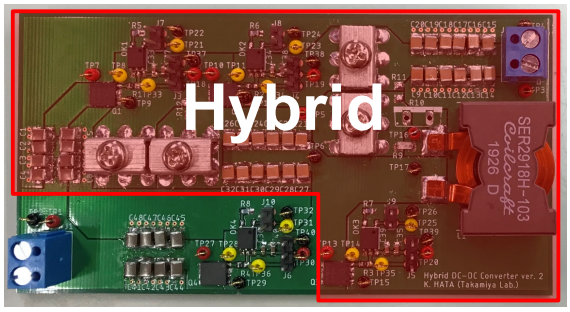
oscilloscope (TBS2104, Tektronix). In the proposed dual-path hybrid operation, V_{x1} and V_{x2} were measured, indicating that the operation shown in Fig. 2 can be successfully implemented. Additionally, V_O and I_L were also measured to show the output voltage regulation characteristics and the inductor current waveform compared to the conventional buck converter. On the other hand, since the buck operation does not change V_{x1}, only V_{x2}, V_O, and I_L are shown.

As shown in Fig. 8 (a), the operation waveform of the proposed dual-path hybrid converter is the same as in Fig. 2, and the operation mode as analyzed in section 2 can be demonstrated. Then, the voltage change at each switching node is smaller than V_{IN}, and as with other hybrid converters, it can be expected to reduce the switching loss. Additionally, the output voltage V_O was stably regulated by the proposed dual-path hybrid converter. Furthermore, in this experiment, the output current I_O was set to 20A, but the inductor current I_L was smaller than that, confirming the usefulness of the proposed dual-path hybrid converter.

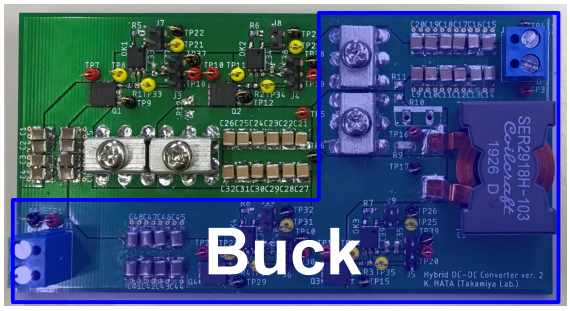
On the other hand, the conventional buck converter was demonstrated as shown in Fig. 8 (b). Although there is no particular problem with the regulation characteristics of the output voltage V_O, the voltage change at the switching node is



(a) Overview



(b) Proposed dual-path hybrid topology

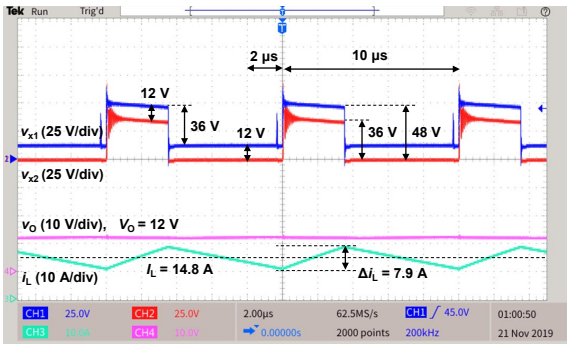


(c) Conventional buck topology

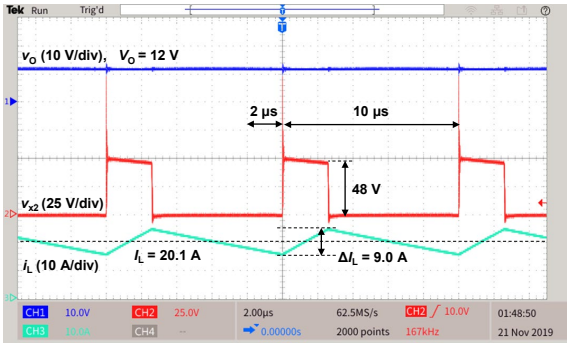
Fig. 7. Photograph of prototype converter.

TABLE I. CIRCUIT COMPONENTS AND PARAMETERS.

Parameters	Value and Design Selection
Input voltage V_{IN}	48 V
Output voltage V_O	12 V
Output current I_O	20 A_{max}
Output power P_o	240 W_{max}
Switching frequency	100 kHz
Power MOSFET $S_{1\text{-}3}$, S_{buck}	80 V, 100 A, $R_{DS(on),max}$: 5.7 mΩ, BSC057N08NS3G, Infineon
Input capacitor C_{IN}	10.56 µF (2.2 µF x 16), X7R, C3225X7R2A225K230, TDK
Flying capacitor C_{FLY}	264 µF (22 µF x 12), X7R, GRM32ER71E226KE15, Murata
Output capacitor C_O	264 µF (22 µF x 12), X7R, GRM32ER71E226KE15, Murata
Inductor L	10 µH, DCR: 2.6 mΩ, SER2918H-103KL, Coilcraft

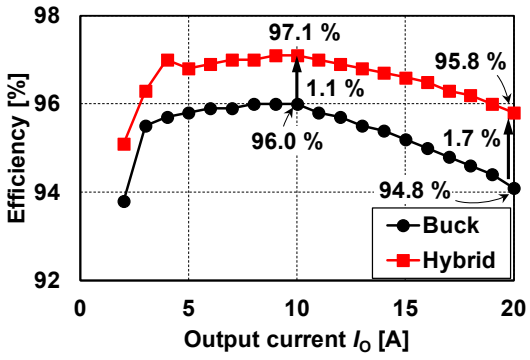


(a) Proposed dual-path hybrid converter

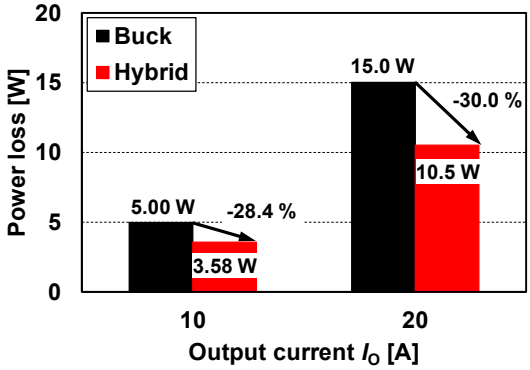


(b) Conventional buck converter

Fig. 8. Measured waveforms of prototype converter at 240 W full load condition.



(a) Efficiency



(b) Power loss

Fig. 9. Measured efficiency and power loss comparison.

equal to V_{IN}, and there is a concern that the switching loss and noise will increase more than the proposed dual-path hybrid converter.

As will be described later in the efficiency comparison, the proposed dual-path hybrid converter can reduce both the inductor DC current and ripple current compared with the conventional buck converter, and it can be confirmed from the measured waveforms that the efficiency improvement can be expected by reducing the conduction loss of the inductor.

C. *Efficiency measurement*

Fig. 9 (a) shows the measurement efficiency of the proposed and the conventional converter versus the output current I_O under a fixed conversion ratio of 0.25(=12V/48V). The efficiency at I_O = 10A is 97.1% and 96.0% in the proposed, and the conventional converter, respectively, resulting in the improvement in efficiency by 1.1%. At I_O = 20A, the efficiency is 95.8% and 94.8% in the proposed, and the conventional converter, respectively, increasing the improvement in efficiency to 1.7%. The larger efficiency improvement at higher output current can be mainly explained by a decrease in DC inductor current in the proposed dual-path hybrid converter.

Fig. 9 (b) compares the measured power loss in the proposed and the conventional converter at I_O = 10A and 20A. While the power loss decreases by 28.4% from 5.00W in the conventional, to 3.58W in the proposed at I_O = 10A, the reduction at I_O = 20A becomes much larger by 30.0% from 15.0W in the conventional to 10.5W in the proposed.

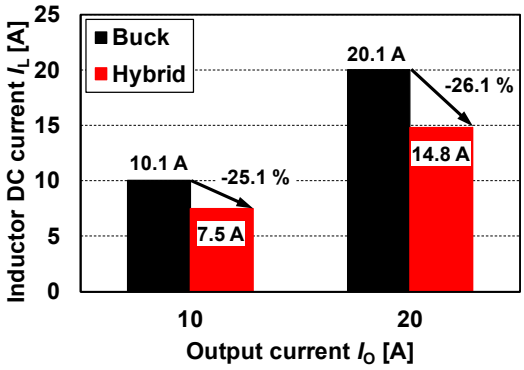
Because the conduction loss has a square dependence on current, the inductor current reduction in the proposed converter, as described in (7) and (10), is more effective at higher output current conditions for reducing the loss and improving the efficiency.

Fig. 10 (a) shows the measurement DC current in inductor, in the proposed and the conventional converter under a condition of I_O = 10A and 20A. The DC current in the inductor at I_O = 10A decreases by 25.1%, from 10.1A in the conventional to 7.5A in the proposed. Similarly, at I_O = 20A, the DC current reduces by 26.1%, from 20.1A in the conventional, to 14.8A in the proposed.

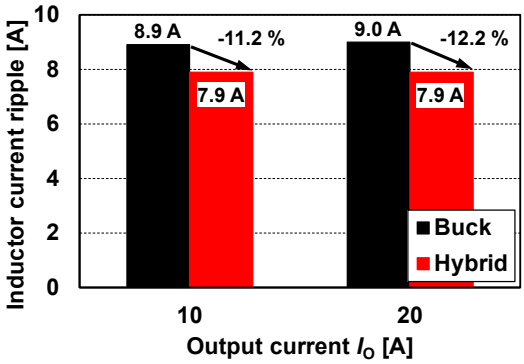
Fig. 10 (b) illustrates the measurement ripple current, in inductor in the proposed and the conventional converter under a condition of I_O = 10A and 20A. The ripple current in the inductor at I_O = 10A decreases by 11.2%, from 8.9A in the conventional to 7.9A in the proposed. Also, at I_O = 20A, the ripple current reduces by 12.2%, from 9.0A in the conventional, to 7.9A in the proposed.

V. Conclusion and Future Work

A dual-path hybrid DC-DC converter for the step-down ratio of less than half with two circuit states is proposed for the first time. In the measurement, the peak efficiency of the proposed dual-path hybrid and conventional buck converters was 97.1% and 96.0% at 120W, 48V-to-12V conversion, respectively, indicating the loss is reduced by 28.4 %. Furthermore, at 240W full load condition, the efficiency of the proposed and conventional converters was 95.8% and 94.8%, respectively, indicating the loss is reduced by 30.0 %. Since the proposed dual-path hybrid converter can reduce the



(a) Inductor DC current



(b) Inductor current ripple

Fig. 10. Measured inductor current comparison.

inductor current compared to the conventional buck converter, it was confirmed that the efficiency improvement becomes larger under heavy load conditions, which means that the conduction loss of the inductor becomes dominant.

As future works, the charge sharing loss between the flying capacitor and the output capacitor will be analyzed because it may affect the efficiency. Additionally, the proposed converter will be compared to the switched capacitor converter and the three-level buck converter to clarify the superiority of the proposed topology over other circuits.

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