Stop-and-Go Gate Drive Minimizing Test Cost to Find Optimum Gate Driving Vectors in Digital Gate Drivers

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Abstract—An active gate driving is effective to solve the trade-off between the switching loss and the current/voltage overshoot of power transistors. The test cost in the conventional digital gate drivers with four variables, however, is high, because more than 2000 measurements are required to find an optimum gate driving vector out of 644 combinations [1]. To minimize the test cost, a stop-and-go gate drive with only one variable is proposed. The switching loss and the current/voltage overshoot in turn-on/off state of IGBT of the conventional gate driver [1] and the proposed stop-and-go gate drive are measured by using a 6-bit programmable digital gate driver IC across nine conditions including different load currents (20 A, 50 A, and 80 A) and temperatures (25 °C, 75 °C, and 125 °C), and they are compared. The performance degradations of the switching loss and the current/voltage overshoot in the proposed stop-and-go gate drive over the conventional gate drive with four variables [1] is less than 8 % and 25 % across the nine conditions in turn-on/off state respectively.

Keywords—Gate driver, IGBT, Test cost, Load current, Temperature

I. INTRODUCTION

Digital gate drivers [1-15] are useful for the active gate driving, because the gate driving current is programmable with gate driving vectors using a software. However the test cost to find optimum gate driving vectors in the conventional digital gate drivers is high, because the number of variables is large (4 [1], 30 [3], and 88 [4]), the number of combinations of variables is huge, and it takes time to find the optimum vectors through trial-and-error measurements. For example, in a 6-bit programmable digital gate drivers with four variables, more than 2000 measurements are required to find an optimum gate driving vector out of 644 (1.7 x 10^2) combinations using a simulated annealing algorithm [1]. In [3], the number of combinations is 6430 (1.5 x 10^3). To make matters worse, a load current (ILOAD) and temperature dependent optimization of the gate driving vectors is required [2], because an optimum vector at a particular ILOAD and temperature does not often work at different conditions, which further increases the test cost. In the proposed stop-and-go gate drive, the test cost is less than 1/200 of the conventional gate drive with four variables [1], because the required number of measurements is less than ten.

II. PROPOSED STOP-AND-GO GATE DRIVE

A. Measurement Setup for Stop-and-Go Gate Driver

Fig. 1 shows a circuit schematic of the measurement setup for the double pulse test for turn-on and turn-off of IGBT (2MBI100VA-060-50, 600 V, 100 A) at 300 V. In order to realize a programmable 63-level drivability in the programmable gate driver, 63 parallel transistors are connected to the gate of IGBT and a 6-bit control signal is applied to specify the number of activated PMOS (NMOS) transistors, nPMOS (nNMOS) [1], respectively. In [2] shown in Fig. 2 (a), the gate driving vector is (n1, n2, n3, n4) with four 160-ns time steps in turn-on state and four 400-ns steps in turn-off state, where n1, n2, n3, and n4 are integers from 0 to 63. (n1, n2, n3, n4) means four variables. In contrast, in the proposed stop-and-go gate drive shown in Fig. 2 (b), the gate driving vector is only n1, which means one variable. In turn-on state, nPMOS is n1 for t1, and nPMOS is 0 for t2, followed by nPMOS is 63 (maximum). t1 and t2 are decided in advance based on the data sheet of power devices and fixed in the measurement. In the measurement, t1 = 320 ns and t2 = 160 ns in turn-on state, while t1 = t2 = 800 ns in turn-off state.

Fig. 1. Circuit schematic of measurement setup.
turned $= 400 \text{ns}$

$$[\text{V}]_1 \quad \text{NMOS} \quad 2 \quad \text{PMOS}$$

B. current is determined by from 0V to data sheet and set $t_{\text{rr}}$ of reverse recovery time $t_{\text{rr}}$.

Where $n_1$ in turn-on state is estimated by the gate charge at threshold voltage ($V_{\text{TH}}$). Similarly, $n_1$ in turn-off state is estimated by the gate current of $Q_2 / t_1$.

**B. How to Set $t_1$, $t_2$, and $n_1$ in Turn-on and Turn-off**

In turn-on state for example when $Q_1 = 50 \text{ nC}$ from the data sheet and set $t_1 = 800 \text{ ns}$, the necessity of turn-on current is determined by $Q_1 / t_1 = 50 \text{ nC} / 320 \text{ ns} = 156 \text{ mA}$. Where $Q_1$ is the amount of the gate charge when $V_{\text{GE}}$ reach from 0V to $V_{\text{TH}}$ as shown Fig. 2. In order to flow 156 mA by $n_{\text{PMOS}}$ driver, the strength of $n_{\text{PMOS}}$ driving number set to about $n_1 = 27$ as shown following calculation, $(156 \text{mA} / 370 \text{mA}) \times 63 = 27$. Because the full scale current of $n_{\text{PMOS}}$, that is $n_1 = 63$, is 495mA by the driver IC setting in this measurement setup.

The black curves show the results of the proposed stop-and-go gate drive, and the current $Q_2$ is calculated as follow, $(313 \text{mA} / 495 \text{mA}) \times 63 = 40$. And the time slot $t_2$ has to hold 0 until the corrector current $I_C$ settle to about 0A. Otherwise the large overshoot voltage occurred in $V_{\text{CE}}$. Although the full scale current of $n_{\text{PMOS}}$ and $n_{\text{NMOS}}$ set to about 370mA and 495mA in this setup, it can arbitrarily change by bias voltage for the driver IC. The time slot $t_1$ should be determined to meet require current under the $n_1$ of $n_{\text{NMOS}}$ and $n_{\text{PMOS}}$ is less than 63.

**III. MEASURED RESULTS**

A. Measured $E_{\text{LOSS}}$ vs. $I_{\text{OVERSHOOT}}$ and $V_{\text{OVERSHOOT}}$

In order to comprehensively compare three gate drives including the conventional single-step gate drive, the conventional digital gate drive with four variables [1], and the proposed stop-and-go gate drive, $E_{\text{LOSS}}$ and the current overshoot ($I_{\text{OVERSHOOT}}$) of IGBT is measured across nine conditions including different $I_{\text{LOAD}}$ (20 A, 50 A, and 80 A) and temperatures (25 °C, 75 °C, and 125 °C). Fig. 4 shows the measured $E_{\text{LOSS}}$ vs. $I_{\text{OVERSHOOT}}$ in turn-on state while Fig. 5 shows the measured $E_{\text{LOSS}}$ vs. $V_{\text{OVERSHOOT}}$ in turn-off state.

The black curves show the trade-off curves using the conventional single-step gate driving waveforms with varied $n_{\text{PMOS}}$ from 5 to 63. The red squares show the results of the optimized vectors in the conventional digital gate drive with four variables using a simulated annealing algorithm [1]. The blue curves show the results of the proposed stop-and-go gate drive with varied $n_1$ from 1 to 63. The turn-on object function ($f_{\text{OBJ,ON}}$) and turn-off object function ($f_{\text{OBJ,OFF}}$) are defined as

![Gate charge dependence of $V_{\text{CE}}$](image1)

**Fig. 3.** Gate charge dependence of $V_{\text{GE}}$.

**Fig. 2.** Gate charge dependence of $V_{\text{CE}}$. Gate driving vector and waveforms. (a) Conventional [1]. (b) Proposed stop-and-go gate drive.
Fig. 4 Measured \( E_{\text{LOSS}} \) vs. \( I_{\text{OVERSHOOT}} \) of three gate drives in turn-on state. Black curves: trade-off curves using the conventional single-step gate driving waveforms with varied \( n_{\text{MAX}} \) from 5 to 63. Red squares: the results of the optimized vectors in the conventional digital gate drive with four variables using a simulated annealing algorithm [1]. Blue curves: the results of the proposed stop-and-go gate drive with varied \( n_{\text{STOP}} \) from 1 to 63.

\[
\begin{align*}
    f_{\text{OBJ,ON}} &= \left( \frac{E_{\text{LOSS}}}{E_{\text{LOSS,MAX}}} \right)^2 + \left( \frac{I_{\text{OVERSHOOT}}}{I_{\text{OVERSHOOT,MAX}}} \right)^2 \quad (1) \\
    f_{\text{OBJ,OFF}} &= \left( \frac{E_{\text{LOSS}}}{E_{\text{LOSS,MAX}}} \right)^2 + \left( \frac{V_{\text{OVERSHOOT}}}{V_{\text{OVERSHOOT,MAX}}} \right)^2 \quad (2)
\end{align*}
\]

where the subscript \( \text{MAX} \) signifies the maximum of the corresponding quantity. The dotted concentric curves in Fig. 4 show the contour of \( f_{\text{OBJ}} \) defined in Eq. (1). The smaller \( f_{\text{OBJ}} \) is preferred.

In Fig. 4 the smallest value \( f_{\text{OBJ}} \) of the blue line is close to the optimized point in each nine conditions. For example, in the 25 °C with 50A condition the minimum \( f_{\text{OBJ}} \) of the blue line is obtained at \( n_{\text{STOP}} = 28 \) and it is close to the value of the optimized point as indicated red square. The minimum \( f_{\text{OBJ}} \) of the other blue lines are also close the optimized red squares. It means that the effect of proposed stop-and-go vectors are comparable to the ideal vectors.

In the 25 °C with 50A in Fig. 5, the minimum \( f_{\text{OBJ}} \) is obtained at \( n_{\text{STOP}} = 47 \) and it is also close the optimized point. In addition, the proposed stop-and-go vector has good performance in other eight conditions in turn-off state.

**B. Optimum Gate Driving Vectors \( n_{\text{STOP}} \)**

Fig. 6 shows optimum \( n_{\text{STOP}} \) at each \( I_{\text{LOAD}} \) and temperature. The optimum \( n_{\text{STOP}} \) is different across \( I_{\text{LOAD}} \) and temperature variations. Fig. 6 (a) shows optimum \( n_{\text{STOP}} \) in turn-on and Fig. 6 (b) shows that in turn-off. The number of vectors is only one variable vectors for each nine conditions. According the load current increase, the vector strength become lager in both turn-on and turn-off. Also same as temperature increasing.
<table>
<thead>
<tr>
<th>Temperature</th>
<th>$I_{LOAD}$</th>
<th>20A</th>
<th>50A</th>
<th>80A</th>
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<td>25°C</td>
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</tr>
<tr>
<td>125°C</td>
<td>✔</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
<td><img src="image9.png" alt="Image" /></td>
</tr>
</tbody>
</table>

Fig. 5. Measured $E_{LOSS}$ vs. $I_{OVERSHOOT}$ of three gate drives in turn-on state. Black curves: trade-off curves using the conventional single-step gate driving waveforms with varied $n_{MAX}$ from 5 to 63. Red squares: the results of the optimized vectors in the conventional digital gate drive with four variables using a simulated annealing algorithm [1]. Blue curves: the results of the proposed stop-and-go gate drive with varied $n_{i}$ from 1 to 63.

C. Minimum $f_{OBJ}$ of Three Gate Drives at Nine Conditions

Fig. 7 shows the minimum $f_{OBJ}$ of the three gate drives at nine conditions. The $f_{OBJ}$ of the proposed stop-and-go vector is close to that of optimum vectors and it performs drastically reduces $f_{OBJ}$ compared to the conventional single step. Quantitatively, the difference of $f_{OBJ}$ between the conventional digital gate drive with four variables and the proposed stop-and-go gate drive of turn on is less than 8%, and that of turn off is less than 25% which indicates that the performance of the proposed stop-and-go gate drive is quite good.

D. Stop-and-Go Gate Driving Vectors and measured Waveforms

Figs. 8 (a), (b), and (c) show the stop-and-go gate driving vectors and measured waveforms at 50 A, 25 °C in turn-on state at $n_{i}$ = 28 (optimum value), $n_{i}$ = 26 (optimum value − 2), and $n_{i}$ = 33 (optimum value + 5), respectively. The corresponding $E_{LOSS}$ and $I_{OVERSHOOT}$ are shown in Fig. 4. In Figs. 8 (b) and (c), larger $I_{OVERSHOOT}$ is observed, while, in Fig. 8 (a), $I_{OVERSHOOT}$ is minimized. In Fig. 8 (b) the strength $n_{i}$ is weaker than Fig. 8 (a), so the current $I_{C}$ rise time is slightly slow, and the $I_{OVERSHOOT}$ occurred because the slot time $t_{S}$ cannot absorb the reverse recovery time $t_{rr}$ within 160ns. And after that the $n_{i}$ = 63 vector is applied before the reverse recovery current $I_{RR}$ settle 0A. It results in $I_{RR}$ riders on the $I_{C}$ then $I_{OVERSHOOT}$ appeared on $I_{C}$. Also, the weak drive strength makes $E_{LOSS}$ as shown in Fig. (b). In Fig. (c) the strength $n_{i}$ is stronger than Fig. (a), so the $I_{OVERSHOOT}$ is occurred because of the reverse recovery current $I_{RR}$ of $D_{1}$. 3099
Figs. 9 (a), (b), and (c) show the stop-and-go gate driving vectors and measured waveforms at 50 A, 25 °C in turn-off state at $n_1 = 47$ (optimum value), $n_1 = 46$ (optimum value − 1), and $n_1 = 49$ (optimum value + 2), respectively. The corresponding $E_{LOSS}$ and $V_{OVERSHOOT}$ are shown in Fig. 5. In Figs. 9 (b) and (c), larger $V_{OVERSHOOT}$ is observed, while, in Fig. 9 (a), $V_{OVERSHOOT}$ is minimized.

In Fig. 9 (b) the strength $n_1$ is weaker than Fig. 9 (a), so the voltage $V_{CE}$ rise time is slightly slow, therefore there are no overshoot at rising edge of $V_{CE}$. But the large $V_{OVERSHOOT}$
occurred when vector applied to 63. Because the 63 level vector is applied to the gate of IGBT before the _L_ to reach about 0A. Also, the weak drive strength makes _E_{LSS}_, as shown in Fig. 9 (b). In Fig. 9 (c) the strength _n_ is stronger than Fig. 9 (a), so the voltage _V_{CE_} rise time is faster than Fig. 9 (a), as a result a large amount of _V_{OVERSHOOT} is appeared at the rise edge of _V_{CE_}.

IV. CONCLUSIONS

To minimize the test cost to find optimum gate driving vectors in the conventional digital gate drives, the stop-and-go gate drive with only one variable (n) is proposed. Compared with the conventional digital gate drive with four variables [1], the required number of measurements is reduced from 2000 to 9, while the _f_{DS} degradation is less than 8% and 25% across the nine conditions in turn-off state respectively. Therefore, the proposed stop-and-go gate drive with the minimized test cost is a practical method for the digital gate drivers.

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