5 V, 300 MSa/s, 6-bit Digital Gate Driver IC for GaN Achieving 69 % Reduction of Switching Loss and 60 % Reduction of Current Overshoot

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***Abstract*—A digital gate driver (DGD) is an important technology to reduce both switching loss and voltage and/or current overshoot. In this paper, a 5 V, 300 MSa/s, 6-bit DGD IC, where the gate current is varied in 64 levels for each of 16 3.3-ns time intervals, is developed using 180-nm BCD process for GaN FETs. The parameters for DGD are automatically optimized using a simulated annealing algorithm through repeated switching measurements. In the turn-on of GaN FETs at 48 V and 8 A, compared with the conventional single-step gate driving, the proposed gate drive using DGD reduces the switching loss from 3.9 µJ to 1.2 µJ by 69 % at the same the current overshoot of 3.4 A and reduces the current overshoot from 8.5 A to 3.4 A by 60 % at the same switching loss of 1.2 µJ, which clearly shows the advantage of DGD for GaN FETs.**

Keywords— digital gate driver, GaN, switching loss, overshoot

I. Introduction

GaN FETs provide low on-resistance and fast switching, which makes them suitable for realizing high efficiency and small volume power converters. GaN FETs, however, are very difficult to use because of its ultrafast switching operation, which causes large and high frequency voltage and/or current ringing, causing device reliability and EMI problems. A digital gate driver (DGD) [1-8] is an important technology to reduce both switching loss (E_{LOSS}) and voltage and/or current overshoot, because E_{LOSS} and the overshoot are in a trade-off relationship. The conventional DGDs for GaN [6-8], however, have two problems: (1) the reduction of both E_{LOSS} and overshoot in GaN FETs is not shown, because E_{LOSS} is not measured, while the reduction of both E_{LOSS} and overshoot in IGBT and SiC MOSFETs is shown in [5]; and (2) the optimal operation of DGD is not achieved, because the parameters for DGD are manually tuned.

To solve the problems, in this paper, a 5 V, 300 MSa/s, 6-bit DGD IC using 180-nm BCD process is developed. The parameters for DGD are automatically optimized using a simulated annealing algorithm, and 69 % reduction of E_{LOSS} and 60 % reduction of the current overshoot ($I_{OVERSHOOT}$) compared with the conventional single-step gate driving (CSG) in the turn-on of GaN FETs at 48 V and 8 A are demonstrated for the first time.

II. Digital Gate Driver IC for GaN FETs

Figs. 1 and 2 show a circuit schematic and a timing chart of the developed 5 V, 300 MSa/s, 6-bit DGD IC for GaN FETs, respectively. The IC is designed using only 5 V transistors and requires a single power supply of 5 V. The gate current (I_G) can be varied in 64 levels for each of 16 3.3-ns time intervals at turn-on/off of GaN FETs depending on scan-in data. 64-level I_G control from 0 A to 5 A in 80 mA increments is achieved by selectively turning on or off six nMOSFETs or pMOSFETs with binary weighted gate widths ($1W_N$, $2W_N$, $4W_N$, $8W_N$, $16W_N$, $32W_N$ in case of nMOSFETs) in the output

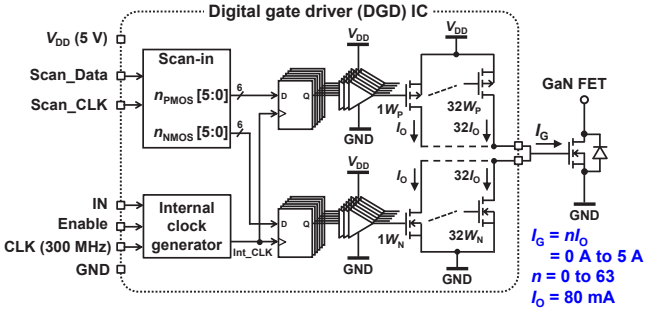

Fig. 1. Circuit schematic of 5 V, 300 MSa/s, 6-bit DGD IC for GaN FETs.

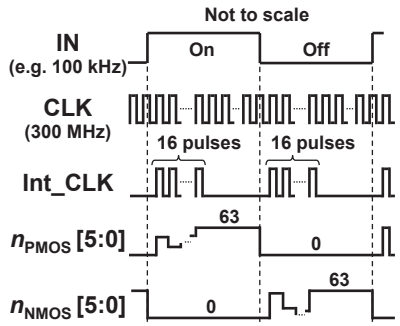

Fig. 2. Timing chart of 300 MSa/s, 6-bit DGD IC.

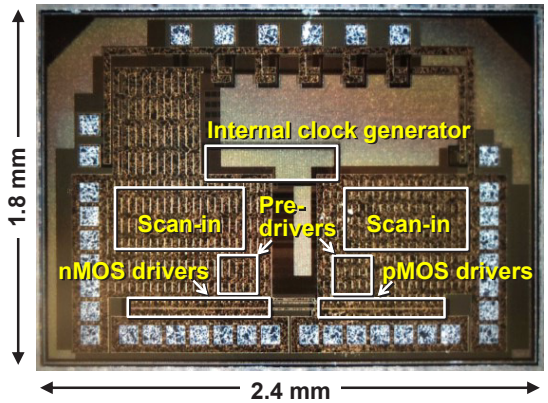

Fig. 3. Die photo of DGD IC fabricated with 180-nm BCD process.

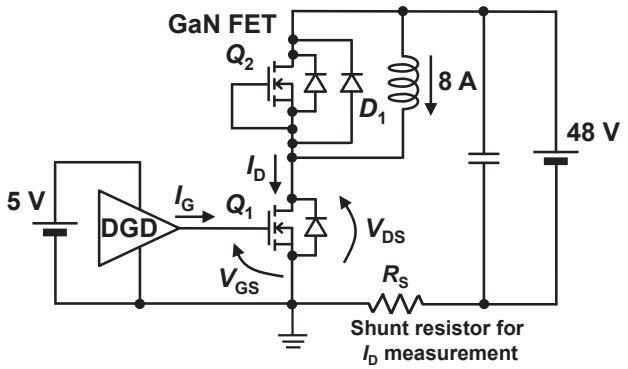

Fig. 4. Circuit schematic of fabricated GaN half bridge.

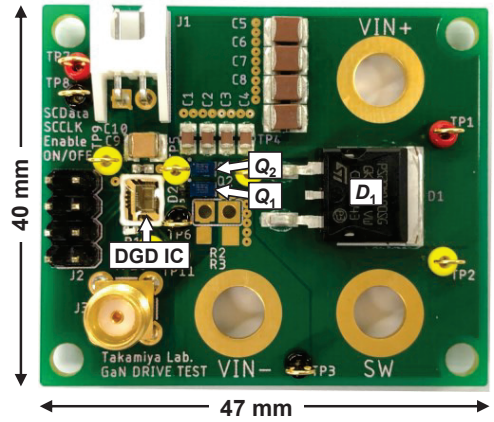

Fig. 5. Photo of PCB of GaN half bridge.

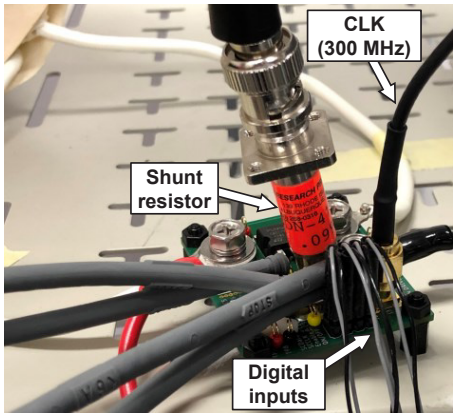

Fig. 6. Measurement setup of GaN half bridge for double pulse test.

stage with 6-bit digital signals. I_G control in 3.3-ns intervals is required, because the turn-on/off transient of GaN FETs is typically less than 10 ns. The 3.3-ns interval is defined by an externally supplied 300-MHz clock signal (CLK). The main reason why the clock frequency could be increased from 25 MHz in DGD for IGBT [5] to 300 MHz is that the high-speed digital data input is not required and the required digital data is pre-stored in on-chip memory (flip-flops) by scan-in. Fig. 3 shows a die photo of the developed DGD IC fabricated with 180-nm BCD process. The die size is 1.8 mm by 2.4 mm.

III. Measurement Setup

Figs. 4 to 6 show a circuit schematic, a photo of PCB, and a measurement setup of the GaN half bridge for the double pulse test, respectively. Table I shows circuit components and parameters. The power supply voltage of the main circuit is 48 V and the load current is 8 A. EPC2045 (100 V, 16 A rating) is used for GaN FETs. I_G waveform of the low side GaN FET (Q_1) is controlled by the developed DGD IC with the power supply of 5 V. A 3.3-nF capacitor is added between the gate and the source of Q_1 whose input capacitance is 767 pF, because I_G of the developed DGD IC is too large for Q_1. Schottky diode (D_1) is added to the high side GaN FET (Q_2) in parallel to reduce the loss during the freewheeling, where the source-to-drain voltage of Q_2 and the forward voltage of D_1 are 1.7 V and 0.7 V, respectively. A shunt resistor (0.1 Ω, 2 GHz-bandwidth) is used to measure the drain current (I_D) waveform to evaluate E_{LOSS} and $I_{OVERSHOOT}$. This paper focuses on the trade-off relationship between E_{LOSS} and $I_{OVERSHOOT}$ at turn-on, because the clear trade-off relationship between E_{LOSS} and the drain-to-source voltage (V_{DS}) overshoot at turn-off is not observed.

TABLE I. Circuit Components and Parameters of GaN Half Bridge

Component	Value and design selection
GaN FETs Q_1, Q_2	100 V, 16 A, EPC2045
Schottky diode D_1	100 V, 20 A, STPS20M100S
Shunt resistor R_S	0.1 Ω, 2 GHz-bandwidth, SDN-414-10

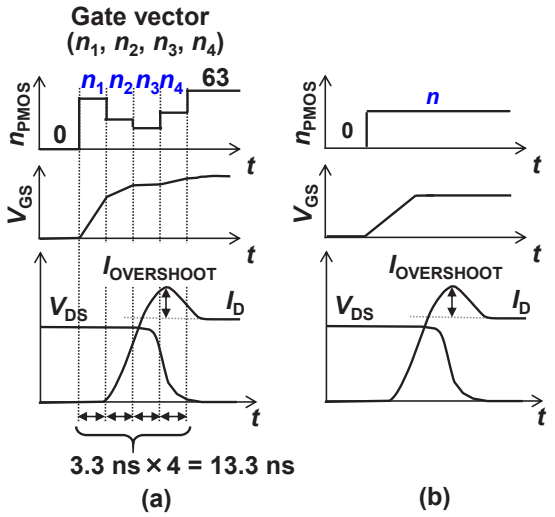

Fig. 7. Definition of gate vectors and waveforms. (a) Proposed gate drive. (b) Conventional single-step gate driving (CSG).

Figs. 7 (a) and (b) show the definition of the gate vectors and waveforms of the proposed gate drive and CSG, respectively. n_{PMOS} is the level of I_G at turn-on and is an integer from 0 to 63. In the proposed gate drive, n_{PMOS} is varied and optimized for each of 4 3.3-ns time intervals with the gate vector of (n_1, n_2, n_3, n_4), and n_{PMOS} is fixed to 63 after the fifth slot. In CSG, n is varied to emulate the conventional gate driving with fixed gate resistor and to show the trade-off relationship between E_{LOSS} and $I_{OVERSHOOT}$.

IV. Measured Results

The measured power consumption of the developed DGD IC at 300 MHz is 73 mW and the power consumption is

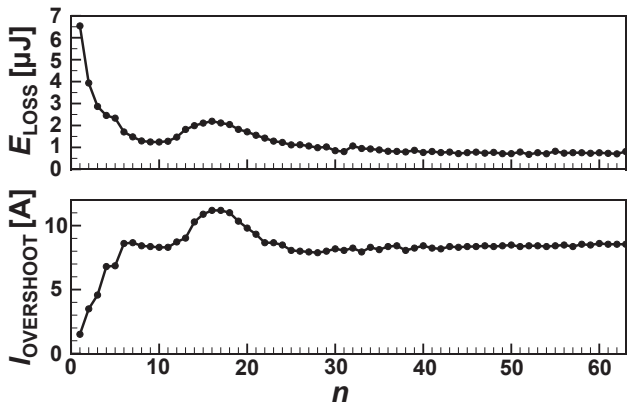

Fig. 8. Measured n dependence of E_{LOSS} and $I_{OVERSHOOT}$ of CSG.

proportional to the clock frequency. The measured maximum clock frequency for correct operation of the developed DGD IC is 460 MHz, which means 2.2-ns interval. Fig. 8 shows the measured n dependence of E_{LOSS} and $I_{OVERSHOOT}$ of CSG. The n dependence is non-monotonic due to the parasitic inductance of the gate loop and the main circuit loop, which indicates that the optimization of the parameters for DGD is complicated and a manual parameter tuning will not work.

Fig. 9 shows the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the proposed gate drive and CSG for comparison. The black line shows the trade-off curve of CSG in Fig. 8. The red star shows the proposed gate drive, where the gate vector is automatically optimized using the simulated annealing algorithm [5] using an object function (f_{OBJ}) defined in Eq. (1) [5].

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,MAX}}\right)^2 + \left(\frac{I_{OVERSHOOT}}{I_{OVERSHOOT,MAX}}\right)^2} \qquad (1)$$

where the subscript MAX signifies the maximum of the corresponding quantity. Small f_{OBJ} means low E_{LOSS} and low $I_{OVERSHOOT}$. In the simulated annealing algorithm, the gate vector (n_1, n_2, n_3, n_4) shown in Fig. 7 (a) to minimize f_{OBJ} is searched through repeated double pulse tests. In this case, 15000 double pulse measurements are done and the best gate vector achieving the minimum f_{OBJ} is adopted. Compared with CSG, the proposed gate drive using DGD reduces E_{LOSS} from 3.9 μJ to 1.2 μJ by 69 % at the same $I_{OVERSHOOT}$ of 3.4 A and reduces $I_{OVERSHOOT}$ from 8.5 A to 3.4 A by 60 % at the same E_{LOSS} of 1.2 μJ, which clearly shows the advantage of DGD for GaN FETs. The corresponding measured waveforms are shown in Fig. 10.

Fig. 10 shows measured waveforms and the gate vectors of CSG and the proposed gate drive extracted from Fig. 9. Figs. 10 (a) and (b) show CSG with n = 2 and n = 24, respectively. Fig. 10 (c) shows the proposed gate drive with the optimized gate vector (n_1, n_2, n_3, n_4) = (0, 31, 40, 1), which successfully reduces both E_{LOSS} and $I_{OVERSHOOT}$. Fig. 10 (a) has the same $I_{OVERSHOOT}$ as Fig. 10 (c) and Fig. 10 (b) has the same E_{LOSS} as Fig. 10 (c).

Table II shows a comparison table of DGD ICs. Compared with the previously published DGD ICs, the proposed DGD IC with the automatically optimized parameters and the single power supply of 5 V demonstrated the reduction of both E_{LOSS} and $I_{OVERSHOOT}$ in GaN FETs for the first time.

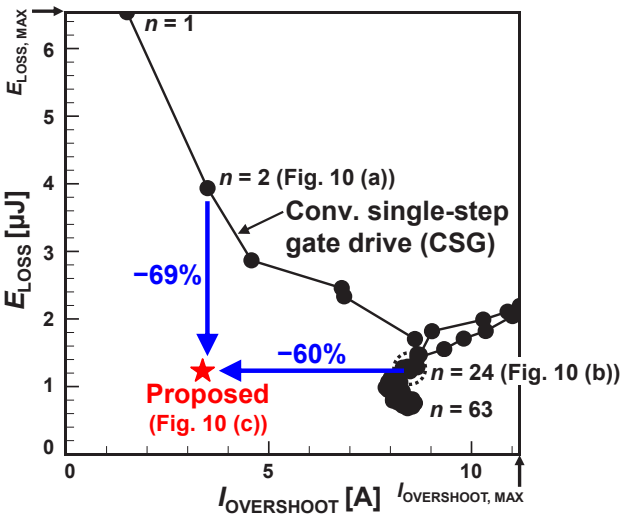

Fig. 9. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of proposed gate drive and CSG. Proposed DGD reduces both E_{LOSS} and $I_{OVERSHOOT}$.

TABLE II. COMPARISON TABLE OF DGD ICS

	TIA'17 [5]	ISPSD'20 [7]	TPEL'21 [8]	This work
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET
Process	180 nm BCD	180 nm BCD	180 nm HV CMOS	180 nm BCD
Power supply	15 V, 10 V, 5 V	5 V, 3.3 V	5 V, 1.8 V	5 V
Output voltage swing	15 V	3.3 V	5 V	5 V
Levels of I_G	6 bit	7 bit	8 bit (coarse), 6 bit (fine)	6 bit
Max. I_G	5 A	3.3 V / 0.5 Ω = 6.6 A	5 V / 0.12 Ω = 42 A	5 A
Time resolution	40 ns	0.3–3.0 ns	1.25 ns (coarse), 100 ps (fine)	3.3 ns
Time steps	No limit	8	104 (= 8 × 13)	16
E_{LOSS} measurement	Yes	No	No	Yes
Parameter optimization	Automatic	Manual	Manual	Automatic

V. CONCLUSIONS

5 V, 300 MSa/s, 6-bit DGD IC, where I_G is varied in 64 levels from 0 A to 5 A in 80 mA increments for each of 16 3.3-ns time intervals, is developed using 180-nm BCD process for GaN FETs. Novelty of this paper is E_{LOSS} measurements and the automatic optimization of the parameters for DGD in GaN FETs. In the turn-on switching measurements of GaN FETs at 48 V and 8 A, compared with CSG, the proposed gate drive using DGD reduces E_{LOSS} from 3.9 μJ to 1.2 μJ by 69 % at the same $I_{OVERSHOOT}$ of 3.4 A and reduces $I_{OVERSHOOT}$ from 8.5 A to 3.4 A by 60 % at the same E_{LOSS} of 1.2 μJ, which clearly shows the advantage of DGD for GaN FETs.

ACKNOWLEDGMENT

This work was partially supported by JST ERATO Grant Number JPMJER1501, Japan.

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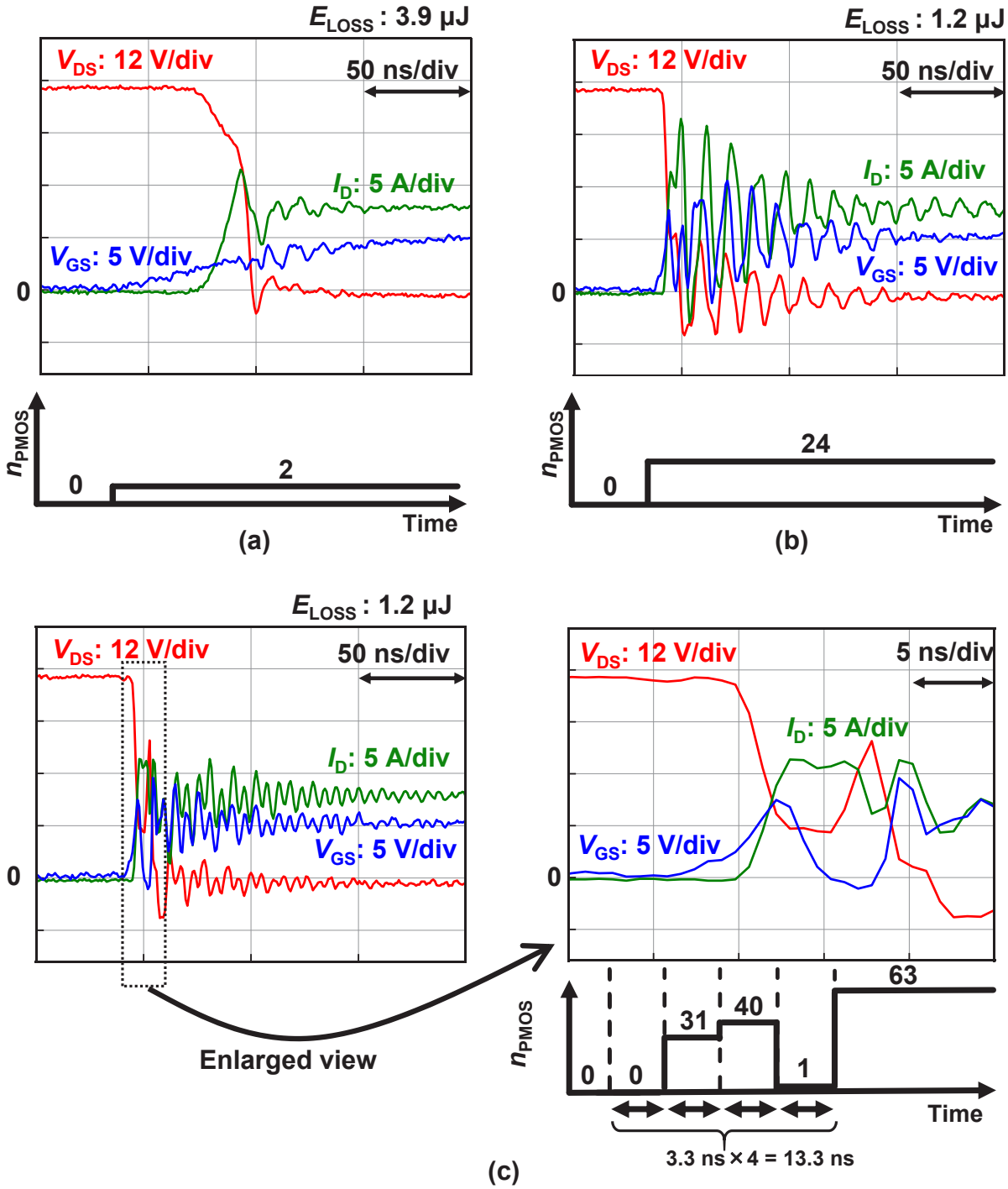

Fig. 10. Measured waveforms and gate driving vectors. (a) CSG (n = 2). (b) CSG (n = 24). (c) Proposed DGD with optimized gate vector.

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