0.55 W, 88%, 78 kHz, 48 V-to-5 V Fibonacci Hybrid DC–DC Converter IC Using 66 mm^3 of Passive Components With Automatic Change of Converter Topology and Duty Ratio for Cold-Crank Transient

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***Abstract*—For 48 V mild hybrid vehicles, a sub-0.5 W, 48 V-to-5 V dc–dc converter fulfilling: 1) high efficiency with small volume; 2) constant switching frequency of less than 500 kHz to avoid the frequency band of AM radio; and 3) constant output voltage ($V_{\rm OUT}$) against the sudden drop of input battery voltage ($V_{\rm IN}$) under cold cranking is required. To meet the requirements, a 0.55 W, 88%, 78 kHz, 48 V-to-5 V Fibonacci hybrid (FH) dc–dc converter IC using 66 mm^3 of passive components is proposed. In the FH dc–dc converter, by adding an inductor and an output capacitor to a 1/5 Fibonacci switched-capacitor (SC) dc–dc converter, the SC dc–dc converter also works as a buck converter without adding power transistors. When $V_{\rm IN}$ drops from 48 V to 20 V in 1 ms in the automotive cold cranking, the FH dc–dc converter cannot keep 5-V $V_{\rm OUT}$, because the output voltage of the internal 1/5 SC dc–dc converter drops from 9.6 to 4 V and the internal buck converter cannot generate 5-V $V_{\rm OUT}$ from 4 V. To solve the problem, a new control method named automatic change of converter topology and duty ratio (ACCD) is proposed. In ACCD, when $V_{\rm IN}$ drops less than 31 V, the converter topology automatically changes from 1/5 SC dc–dc converter to 1/3 SC dc–dc converter and the duty ratio of the pulsewidth modulation signal automatically decreases 3/5 times, thereby achieving the constant 5-V $V_{\rm OUT}$ under cold cranking. To reduce the volume of the FH dc–dc converter, all transistors and diodes, including ten power transistors, gate drivers, bootstrap circuits, and the controller, are fully integrated on 4.6 mm × 2.3 mm IC fabricated with 180 nm BCD process. In the measurements, the proposed 0.55 W, 48 V-to-5 V FH dc–dc converter IC achieved the highest efficiency (88%) with the smallest volume of passive components (66 mm^3) at the lowest switching frequency (78 kHz) compared with previous publications.**

***Index Terms*—Automotive, BCD technology, cold cranking, Fibonacci, hybrid dc–dc converter.**

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I. Introduction

THE target of this article is to develop a sub-0.5 W, 48 V-to-5 V step-down dc–dc converter IC for 48 V mild hybrid electric vehicles. In the mild-hybrid system, the battery voltage changes from conventional 12 to 48 V, while ECUs (electronic control units), including processors, memories, and sensors for the automobile, still require 5 V with less than 100 mA load current. Therefore, the conventional 12 V-to-5 V dc–dc converter should be replaced with the 48 V-to-5 V dc–dc converter. The required step-down ratio increases from 2.4:1 to 9.6:1.

Fig. 1 shows the requirements for the sub-0.5 W, 48 V-to-5 V dc–dc converter IC for the 48 V mild hybrid vehicles. The high efficiency is required because the heat generation due to the loss of the dc–dc converter will increase the cost and the volume for the heat sink. The small volume of the dc–dc converter is also required because the number of ECUs is increasing with the evolution of cars, though the total space for ECUs is constant. For sub-0.5 W output power, highly integrated dc–dc converter IC including power transistors is an effective choice to achieve the small volume. For the automotive applications, dc–dc converters with the switching frequency ($f_{\rm SW}$) of less than 500 kHz [1]–[3] or $f_{\rm SW}$ of more than 2 MHz [4]–[6] are required to avoid the electromagnetic interference (EMI) with an in-car radio receiver using the AM frequency band of 500 kHz–1.6 MHz [7], [8]. Constant $f_{\rm SW}$ is also required because fluctuating $f_{\rm SW}$ in the pulse frequency modulation (PFM) control for the dc–dc converter makes EMI countermeasures difficult [9]. The most challenging problem for the automotive dc–dc converters is the undervoltage transients of the input battery voltage ($V_{\rm IN}$). The most severe of the undervoltage transients is known as a cold crank, which occurs when the engine is initially started. As defined in the test standard of the cold cranking for the automotive dc–dc converters [10], $V_{\rm IN}$ drops from 48 to 20 V in 1 ms, when the starter motor begins turning over the engine from a dead stop. Once the engine starts, $V_{\rm IN}$ recovers to its nominal voltage of 48 V. During the cold-crank transients, the automotive dc–dc converters must keep the constant 5-V output voltage ($V_{\rm OUT}$).

Table I summarizes possible options to realize a sub-0.5 W, 48 V-to-5 V dc–dc converter IC fulfilling the above-mentioned

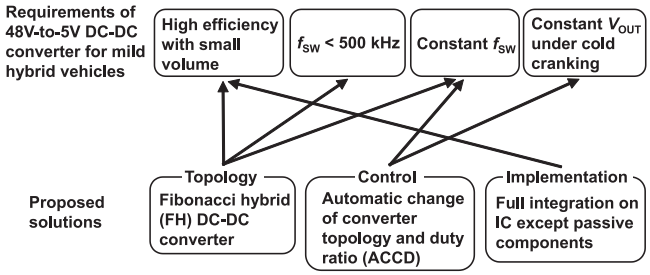


Fig. 1. Requirements for sub-0.5 W, 48 V-to-5 V dc–dc converter IC for 48 V mild hybrid vehicles.

TABLE I
POSSIBLE OPTIONS TO REALIZE SUB-0.5 W, 48 V-TO-5 V DC–DC CONVERTER IC FULFILLING REQUIREMENTS IN FIG. 1

	Buck converter	Switched-capacitor (SC) DC-DC converter (Ladder)	Hybrid DC-DC converter		
			3-level buck	ICL	
				ICH [29]	Fibonacci hybrid (Proposed)
Step-down ratio in SC DC-DC		1/8	1/2	1/2	1/5 (Normal) 1/3 (Cold cranking)
Number (#) of power transistors	2	18	4	4	10 Integrated in IC
# of L	1	0	1	1	1
# of C_{FLY}	0	15	1	1	3
High efficiency with small volume	-	++++	+	++	+++
Regulation at Constant f_{SW}	YES	NO	YES	YES	YES
Constant V_{OUT} under V_{IN} drop (48V➔20V)	YES	NO	YES	YES	NO (w/o ACCD) YES (w/ ACCD)

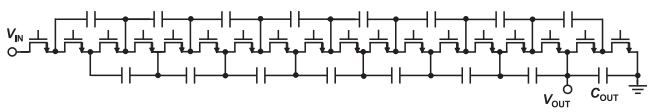


Fig. 2. Circuit schematic of 1/8 ladder SC dc–dc converter.

requirements. In Table I, five topologies of the dc–dc converters are compared from seven separate points of view, including the step-down ratio in a switched-capacitor (SC) dc–dc converter, the numbers of power transistors, inductors (L), and flying capacitors ($C_{\rm FLY}$), high efficiency with small volume, regulation at constant $f_{\rm SW}$, and constant $V_{\rm OUT}$ under $V_{\rm IN}$ drop from 48 to 20 V. The most commonly used buck converter does not achieve the high efficiency with small volume, because the efficiency and the volume are the tradeoffs in the buck converter. $f_{\rm SW}$ of less than 500 kHz requires large inductance, which results in a large volume inductor. The tradeoffs will be shown in Fig. 20. In addition, in the buck converter with 5-V $V_{\rm OUT}$, the efficiency decreases with increasing $V_{\rm IN}$ from 12 to 48 V, because the switching loss increases roughly 16 times.

The 48 V-to-5 V SC dc–dc converter will achieve the highest efficiency with the smallest volume [11], [12] because the energy density of SMD capacitors is much higher than that of SMD inductors [13], [14]. As an example, Fig. 2 shows a circuit schematic of the 1/8 ladder SC dc–dc converter. The SC dc–dc converter, however, does not achieve the $V_{\rm OUT}$ regulation at constant $f_{\rm SW}$ and the constant $V_{\rm OUT}$ under $V_{\rm IN}$ drop, because the step-down ratio is intrinsically determined by the converter topology.

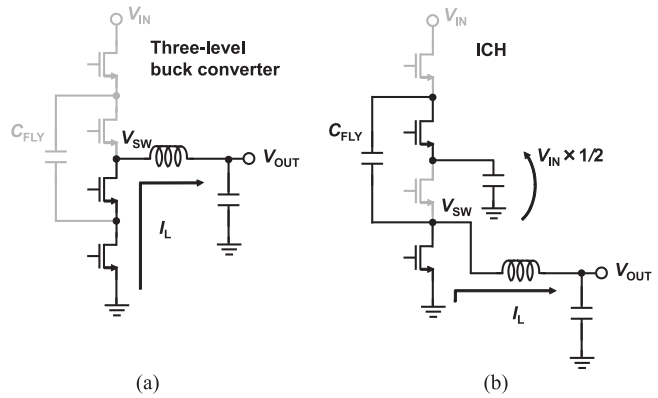


Fig. 3. Circuit schematics of (a) 3-level buck converter and (b) ICH [29].

Hybrid dc–dc converters [4], [15]–[28], where inductive dc–dc converter and capacitive dc–dc converter are merged, are the strong candidates for the converter fulfilling the above-mentioned requirements because the hybrid dc–dc converters solve the tradeoffs between the efficiency and the volume in the buck converter. Among a variety of the hybrid dc–dc converters, a three-level buck converter [4], [26]–[28] and LTC7821 [29] are shown in Table I. In this article, LTC7821 is named as ICH because an inductor is connected to the half $V_{\rm IN}$ switching node in an SC dc–dc converter. Fig. 3 (a) and (b) shows the circuit schematics of the three-level buck converter and ICH [29], respectively. In Fig. 3(a) and (b), $V_{\rm IN}$ /2 is generated by a 1/2 SC dc–dc converter and the switching node ($V_{\rm SW}$) changes between $V_{\rm IN}$ /2 and 0 V. As shown in Table I, in the 48 V-to-5 V conversion, the efficiency of ICH will be higher than that of the three-level buck converter, because the number of serially connected turn-ON power transistors of the three-level buck converter when $V_{\rm SW}$ is connected to 0 V, is more than that of ICH. Specifically, the number of turn-ON power transistors in Fig. 3(a) is two, while that in Fig. 3(b) is one. In ICH, however, the $V_{\rm SW}$ amplitude of $V_{\rm IN}$/2 is still too large and a smaller $V_{\rm SW}$ amplitude will be required for the 48 V-to-5 V conversion because the required step-down ratio is 9.6:1.

To solve the problems of the previous converters and to meet the requirements shown in Fig. 1, a 0.55 W, 88%, 78 kHz, 48 V-to-5 V Fibonacci hybrid (FH) dc–dc converter IC using 66 mm^3 of passive components is proposed in this article.

This article has three major proposed solutions including topology, control, and implementation of the dc–dc converter.

1) A new converter topology of the FH dc–dc converter is proposed to achieve a highly efficient 48 V-to-5 V dc–dc converter with a small volume and a constant $f_{\rm SW}$ of less than 500 kHz.
2) A new control method named automatic change of converter topology and duty ratio (ACCD) for the FH dc–dc converter is proposed to achieve the constant 5-V $V_{\rm OUT}$ under the cold cranking at constant $f_{\rm SW}$.
3) A new implementation of the FH dc–dc converter is proposed. All transistors and diodes of the FH dc–dc converter, including ten power transistors, gate drivers, bootstrap circuits, and the controller, are fully integrated

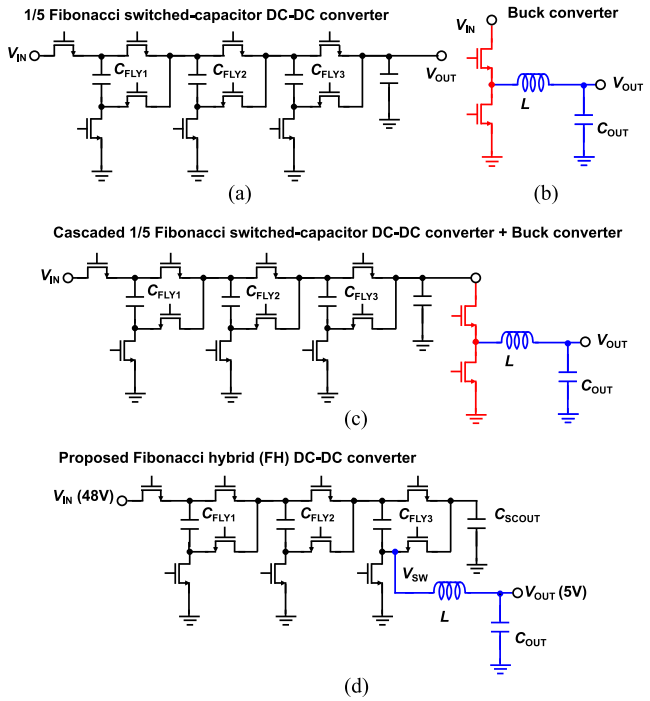


Fig. 4. Circuit schematics of (a) 1/5 Fibonacci SC converter, (b) buck converter, (c) cascaded converter, and (d) proposed 48 V-to-5 V FH dc–dc converter.

on IC fabricated with 180 nm BCD process to reduce the volume of the dc–dc converter.

As shown in Table I, because of the three proposed solutions, the proposed FH dc–dc converter successfully meets the requirements shown in Fig. 1. In the measurements, the proposed 0.55 W, 48 V-to-5 V FH dc–dc converter IC achieved the highest efficiency (88%) with the smallest volume of passive components (66 mm^3) at the lowest switching frequency (78 kHz) compared with previous publications.

In this article, in Section II, the concept of the proposed FH dc–dc converter is shown and the operation is analyzed to compare with conventional converters. In Section III, the circuit design of the proposed FH dc–dc converter IC, including the bootstrap circuits for gate drivers and ACCD for the cold-crank transient, is shown. In Section IV, chip implementation and measured results of the proposed FH dc–dc converter IC are shown. In Section V, the proposed FH dc–dc converter IC is compared with the state-of-the-art 48V-to-5V dc–dc converter ICs where the power transistors are integrated on IC. Finally, Section VI concludes this article.

II. Principle of Proposed FH DC–DC Converter

Fig. 4 shows the circuit schematics of the proposed 48 V-to-5 V FH dc–dc converter, merging a 1/5 Fibonacci SC dc–dc converter and a buck converter. Note that the proposed FH dc–dc converter is not the cascade connection of the SC dc–dc converter and the buck converter, as shown in Fig. 4(c). In the case of the naive cascade connection, the converter's overall efficiency is simply determined by the SC efficiency times the buck efficiency. In the proposed FH dc–dc converter, by adding an inductor (L) and an output capacitor ($C_{\rm OUT}$) to $V_{\rm SW}$ of the 1/5 Fibonacci SC dc–dc converter, the SC dc–dc converter also works as the cascaded converter without adding power transistors. Compared with the 12 power transistors in Fig. 4(c), the proposed FH dc–dc converter can achieve higher efficiency because the number of power transistors is ten in Fig. 4(d). The concept of adding an inductor to the lowest voltage switching node in an SC dc–dc converter is similar to ICH in Fig. 3(b). In this article, the concept is named as ICL, because an inductor is connected to the lowest voltage switching node in an SC dc–dc converter, and ICL is shown in Table I. ICL is important to achieve high efficiency in the 48 V-to-5 V conversion, because the number of turn-ON power transistors is one when $V_{\rm SW}$ is connected to 0 V, and the conduction loss is minimum. The difference between ICH and the proposed FH dc–dc converter is the $V_{\rm SW}$ amplitude. Compared with ICH, the $V_{\rm SW}$ amplitude of the proposed FH dc–dc converter is reduced from $V_{\rm IN}/2$ to $V_{\rm IN}/5$ to achieve higher efficiency with smaller volume by replacing 1/2 SC dc–dc converter with the 1/5 Fibonacci SC dc–dc converter. The design procedure of the topology's selection from the system point of view is as follows.

Step 1: The target step-down ratio is 5V/48V = 1/9.8.

Step 2: The proposed hybrid dc–dc converter combining the SC dc–dc converter and the buck converter has a design constraint that the SC dc–dc converter and the buck converter need to operate in the same duty cycle. The typical duty ratio for hybrid dc–dc converters is determined as 50%, because the SC dc–dc converter usually works at a duty ratio of 50%.

Step 3: The conversion ratio of the buck converter inside the hybrid dc–dc converter is half at the duty ratio = 50%. Therefore, the conversion ratio for the SC dc–dc converter inside the hybrid dc–dc converter should be 1/4.8.

Step 4: It is needed to select the SC dc–dc converter topology with a step-down ratio close to 1/5 and the minimum number of external $C_{\rm FLY}$s to minimize the volume of the off-chip passive components. 1/5 Fibonacci dc–dc converter shown in Fig. 4(a) is the selected topology with the least number of $C_{\rm CFLY}$s [30], [31].

The operation principle of the proposed FH dc–dc converter is explained and analyzed to compare with the conventional buck converter and ICH. The reason why the two are selected for the comparison is because in all topologies, the number of serially connected turn-ON power transistors when $V_{\rm SW}$ is connected to 0 V is one. Note that as for multilevel buck converters, such as 3-level converter, the number is two. Hence, it is not included in the analytical comparison here.

Fig. 5 shows two states of operations of the proposed FH dc–dc converter. 3/5 $V_{\rm IN}$ is applied to $C_{\rm FLY1}$, 2/5 $V_{\rm IN}$ is applied to $C_{\rm FLY2}$, and 1/5 $V_{\rm IN}$ is applied to $C_{\rm FLY3}$ and $C_{\rm SCOUT}$. $V_{\rm SW}$ is 1/5 $V_{\rm IN}$ in state A, while $V_{\rm SW}$ is 0 V in state B. Assuming that the duty ratio (D) is ideally controlled between 0 and 1, $V_{\rm OUT}$ is regulated between 1/5 $V_{\rm IN}$ and 0 V. The conversion ratio (M) is shown as follows:

$$M = V_{\rm OUT}/V_{\rm IN} = D/5. \quad (1)$$

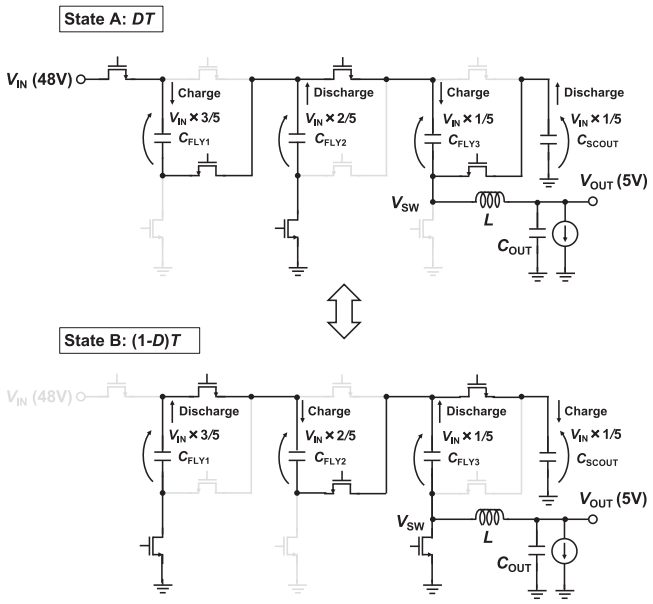


Fig. 5. Two states of proposed FH dc–dc converter in 1/5 mode.

Note that M is limited between 0.2 and 0 in the proposed FH dc–dc converter. The inductor current ripples in the conventional buck converter $\Delta I_{\mathrm{L,\ Buck}}$, that in ICH $\Delta I_{\mathrm{L,\ ICH}}$, and that in the proposed FH dc–dc converter $\Delta I_{\mathrm{L,\ Proposed}}$, are expressed as follows:

$$\Delta I_{\mathrm{L,Buck}} = \frac{V_{\mathrm{IN}}}{L f_{\mathrm{SW}}} (1 - M)\, M \tag{2}$$

$$\Delta I_{\mathrm{L,ICH}} = \frac{V_{\mathrm{IN}}}{L f_{\mathrm{SW}}} (1 - 2M)\, M \tag{3}$$

$$\Delta I_{\mathrm{L,Proposed}} = \frac{V_{\mathrm{IN}}}{L f_{\mathrm{SW}}} (1 - 5M)\, M. \tag{4}$$

Fig. 6(a) shows the calculated M dependence of the normalized inductor current ripple (ΔI_{L}) of the three converters at the same V_{IN}, L, and f_{SW}. Compared with the conventional buck converter and ICH, at the target M of 0.1, the proposed FH dc–dc converter reduces ΔI_{L} by 44% and 38%, respectively. Reduced ΔI_{L} suggests that the conduction loss due to power transistors and the inductor is reduced, thereby achieving high efficiency.

Another interpretation of (2)–(4) is possible. The switching frequency ratios (K_{ICH} and K_{Proposed}) of ICH and the proposed FH dc–dc converter normalized to the conventional buck converter at the same ΔI_{L}, V_{IN}, and L are defined as follows:

$$K_{\mathrm{ICH}} = \frac{f_{\mathrm{SW,ICH}}}{f_{\mathrm{SW,Buck}}} = \frac{1 - 2M}{1 - M} \tag{5}$$

$$K_{\mathrm{Proposed}} = \frac{f_{\mathrm{SW,Proposed}}}{f_{\mathrm{SW,Buck}}} = \frac{1 - 5M}{1 - M}. \tag{6}$$

Fig. 6(b) shows calculated M dependence of K_{ICH} and K_{Proposed} at the same ΔI_{L}, V_{IN}, and L. At the target M of 0.1, K_{ICH} and K_{Proposed} are 0.89 and 0.56, respectively. Reduced K_{Proposed} suggests that the same efficiency is achieved with the reduced f_{SW}, which is important to achieve the requirements shown in Section I.

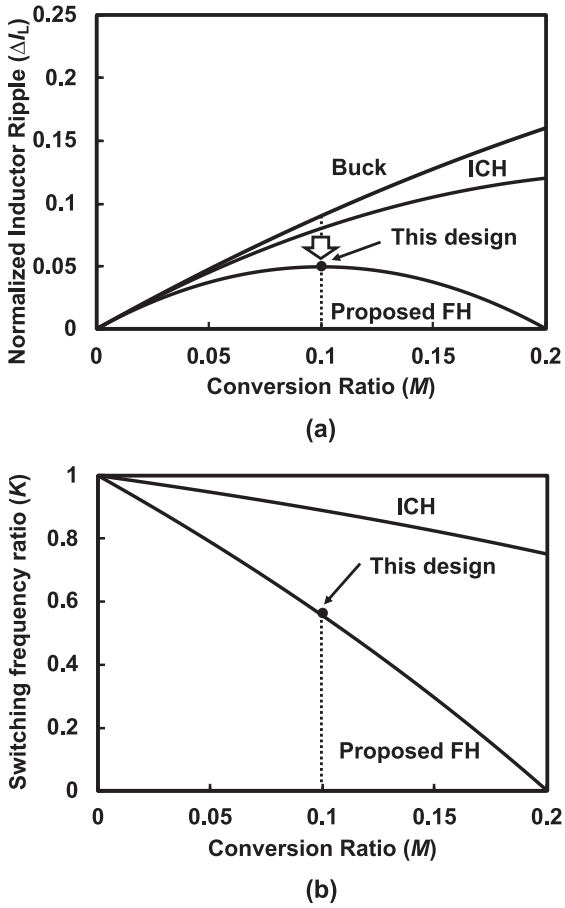


Fig. 6. (a) Calculated M dependence of normalized inductor current ripple (ΔI_{L}) of three converters at same V_{IN}, L, and f_{SW}. (b) Calculated M dependence of K_{ICH} and K_{Proposed} at same ΔI_{L}, V_{IN}, and L.

III. Circuit Design of Proposed FH DC–DC Converter IC

A. Architecture

Fig. 7 shows a block diagram of the proposed FH dc–dc converter IC. The power converter topology is the same as Fig. 4. V_{IN} of 48V is converted to V_{SCOUT} of 9.8 V by the 1/5 Fibonacci SC dc–dc converter, and V_{SCOUT} is converted to V_{OUT} of 5 V by the buck converter (M_{10}, M_8, and L). V_{OUT} is fed back to a voltage mode PWM controller with a type-III compensator for the regulation of V_{OUT}. The PWM signals are distributed to ten power transistors (M_1–M_{10}) via the gate signal logic, level shifters, and the gate drivers. All power supply voltages of the gate drivers for power transistors (M_1, M_2, M_4, M_6, M_7, M_9, M_{10}) are generated by bootstrap circuits, which will be explained in Section III-B. The ACCD controller and the programmable ramp generator are used for ACCD to achieve the constant 5-V V_{OUT} under the cold cranking at constant f_{SW}, which will be explained in Section III-C. All the reference voltages (V_{REF1}–V_{REF5}) are generated by a V_{REF} generator. As shown in Table I, compared with the conventional buck converter, one of the design challenges of the proposed FH dc–dc converter is the increased number of power transistors from two to ten. To avoid the large volume due to the ten power transistors and related gate

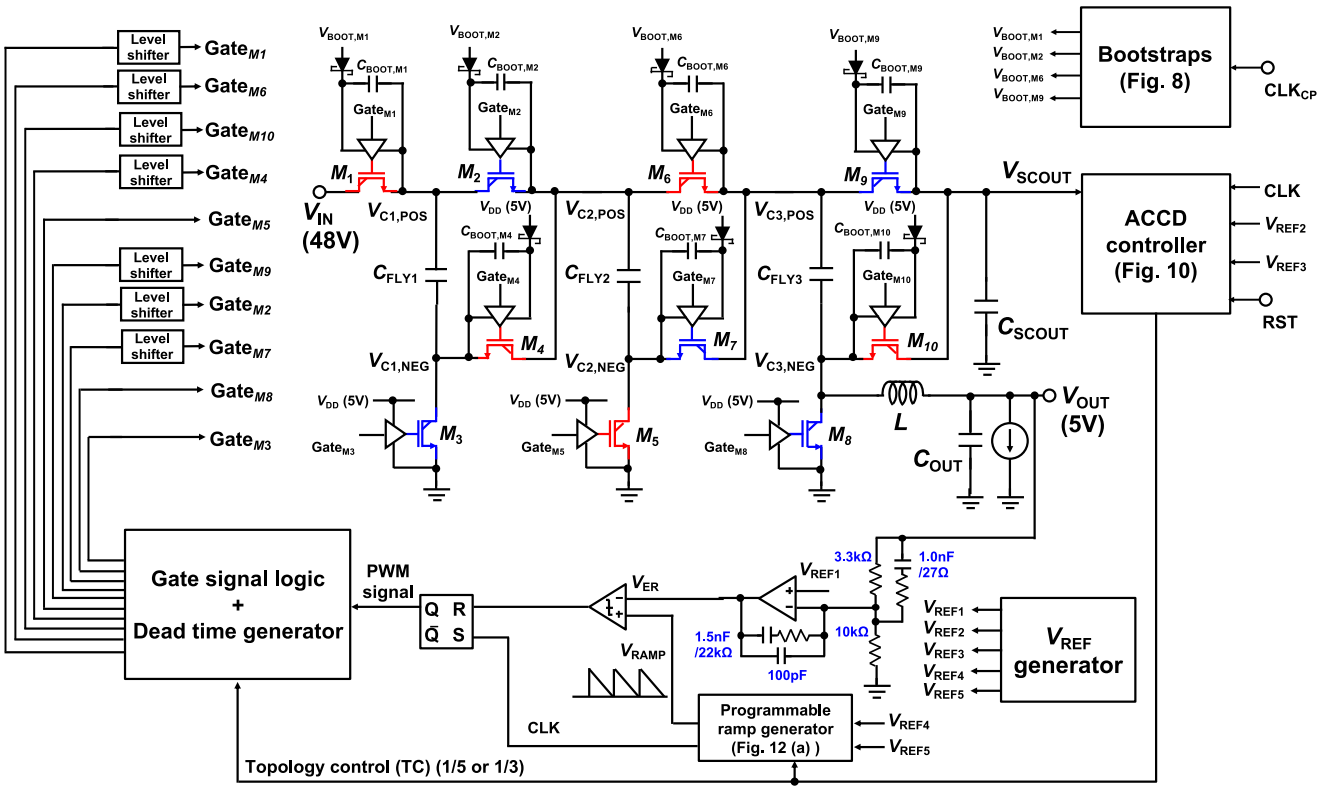


Fig. 7. Block diagram of the proposed FH dc–dc converter IC.

drivers and bootstrap circuits, all transistors and diodes in Fig. 7 are fully integrated on IC to reduce the volume of the dc–dc converter. All voltages and signals, except for the 5-V power supply voltage (V_{DD}) for the controller and the clock signal for the bootstraps ($\mathrm{CLK_{CP}}$), are generated on IC. In contrast, inductor L and all capacitors and resistors, including those for the compensator, are discrete components placed in the PCB, which will be explained in Section IV.

B. Bootstrap Circuits for Gate Drivers

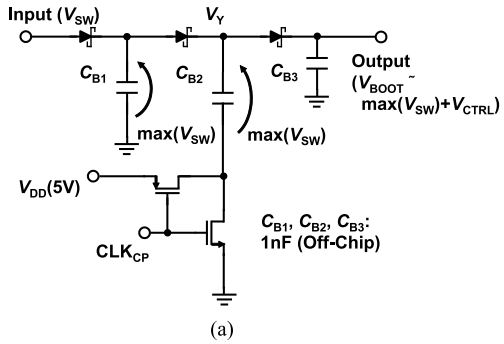
One of the design challenges of the proposed FH dc–dc converter is how to generate seven different power supply voltages of the gate drivers for the power transistors ($\mathrm{M_1}$, $\mathrm{M_2}$, $\mathrm{M_4}$, $\mathrm{M_6}$, $\mathrm{M_7}$, $\mathrm{M_9}$, and $\mathrm{M_{10}}$) because the source voltages of the power transistors is not 0 V. For each power transistor ($\mathrm{M_1}$, $\mathrm{M_2}$, $\mathrm{M_4}$, $\mathrm{M_6}$, $\mathrm{M_7}$, $\mathrm{M_9}$, and $\mathrm{M_{10}}$), the power supply voltage for the gate-to-source voltage of 5 V is required.

In the previously published 1/5 Fibonacci SC dc–dc converter [33], ten isolated dc–dc converters are used to generated the power supply voltages of the gate drivers for ten power transistors, which is unacceptable in this article, because ten bulky transformers will increase the volume of the dc–dc converter.

In the previously published 1/11 SC dc–dc converter [11], an additional fully integrated ladder SC dc–dc converter is used to generate the power supply voltages of the gate drivers. The large area overhead due to the ladder converter, however, is not acceptable, because the ladder converter occupies roughly half the die area of the main 1/11 SC dc–dc converter, which will increase the cost of IC.

To solve the problems, in this article, a new integrated bootstrap circuit for the FH dc–dc converter IC is proposed. In Fig. 7, two types of bootstrap circuits are required. For the power transistors ($\mathrm{M_4}$, $\mathrm{M_7}$, and $\mathrm{M_{10}}$), the conventional bootstrap circuit works, because the source voltages of the power transistors are connected 0 V in state A or state B, as shown in Fig. 5. In contrast, for the power transistors ($\mathrm{M_1}$, $\mathrm{M_2}$, $\mathrm{M_6}$, and $\mathrm{M_9}$), the conventional bootstrap circuit does not work, because the source voltages of the power transistors are not connected 0 V and a new bootstrap circuit is required. For example, $V_{\mathrm{BOOT1,M1}}$ for $\mathrm{M_1}$ in Fig. 7 should be 53 V (= 48 V + 5 V) when $V_{\mathrm{C1,POS}}$ is 48 V in state A in Fig. 5, while $V_{\mathrm{BOOT1,M1}}$ should be 33.8 V (= 28.8 V + 5 V) when $V_{\mathrm{C1,POS}}$ is 28.8 V (= V_{IN} x 3/5) in state B. To generate $V_{\mathrm{BOOT1,M1}}$ of 33.8 V, a new bootstrap circuit is proposed.

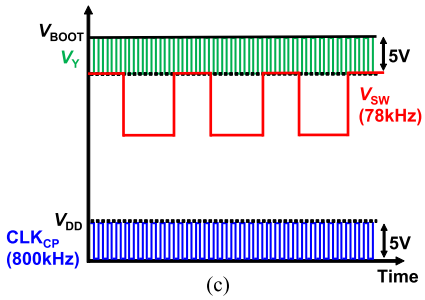
Fig. 8 shows the proposed bootstrap circuit for the power transistors ($\mathrm{M_1}$, $\mathrm{M_2}$, $\mathrm{M_6}$, and $\mathrm{M_9}$). Fig. 8 (a)–(c) shows the circuit schematic, input and output connections of the bootstrap circuit, and operating waveforms, respectively. In Fig. 8(a), high-voltage Schottky diodes are also integrated on IC. For example, in order to generate $V_{\mathrm{BOOT1,M1}}$ of 33.8 V for $\mathrm{M_1}$, the input of Fig. 8(a) is connected to $V_{\mathrm{C2,POS}}$ in Fig. 7, and the output of Fig. 8(a) is connected to $V_{\mathrm{BOOT1,M1}}$ in Fig. 7. $V_{\mathrm{C2,POS}}$ changes between 2/5 V_{IN} and 3/5 V_{IN}, as shown in Fig. 8(b) and (c). In Fig. 8(a), the maximum voltage of the input (V_{SW}) is sampled in $C_{\mathrm{B,1}}$ and the maximum voltage is equal to 3/5 V_{IN} (= 28.8 V). Using $C_{\mathrm{B,2}}$ and the 800-kHz clock signal ($\mathrm{CLK_{CP}}$), V_{Y} changes between



(a)

Bootstrap Circuit #	Input (V_{SW})	Output (V_{BOOT})
1	$V_{C2,POS}$ = { 2/5 V_{IN} (State A); 3/5 V_{IN} (State B) }	$V_{BOOT,M1}$
2	$V_{C3,POS}$ = { 2/5 V_{IN} (State A); 1/5 V_{IN} (State B) }	$V_{BOOT,M2}$
3	V_{SCOUT} = 1/5 V_{IN}	$V_{BOOT,M6}$, $V_{BOOT,M9}$

(b)



(c)

Fig. 8. Proposed bootstrap circuit for power transistors (M_1, M_2, M_6, and M_9). (a) Circuit schematic. (b) Input and output connections of the bootstrap circuit. (c) Operating waveforms.

28.8 and 33.8 V (= 28.8 V + 5 V), as shown in Fig. 8(c). The maximum voltage of V_Y is sampled in $C_{B,3}$ and the output voltage ($V_{BOOT1,M1}$) of 33.8 V is successfully obtained. In a similar way, $V_{BOOT1,M2}$, $V_{BOOT1,M6}$, and $V_{BOOT1,M9}$ are obtained by changing the input connection, as shown in Fig. 8(b). The proposed bootstrap circuit for $V_{BOOT1,M6}$, and $V_{BOOT1,M9}$ is shared.

A sophisticated point of the proposed bootstrap circuit is that existing switching nodes in the FH dc–dc converter are used for the input of the bootstrap circuit. For example, $V_{C2,POS}$ is used for $V_{BOOT1,M1}$, and note that M_1 is far from $V_{C2,POS}$, as shown in Fig. 7.

C. ACCD for Cold-Crank Transient

As shown in Section I, the most challenging problem for the automotive dc–dc converters is the cold-crank transients where V_{IN} drops from 48 to 20 V in 1 ms. During the cold-crank transients, the automotive dc–dc converters must keep the constant 5-V V_{OUT}. As shown in Fig. 9, one of the issues of the proposed FH dc–dc converter is that the FH dc–dc converter cannot keep 5-V V_{OUT} under cold cranking, because $V_{C3,NEG}$ drops from 9.6 V (= 48 V/5) to 4 V (= 20 V/5) and the buck converter (M_{10}, M_8, and L) cannot generate 5-V V_{OUT} from 4 V.

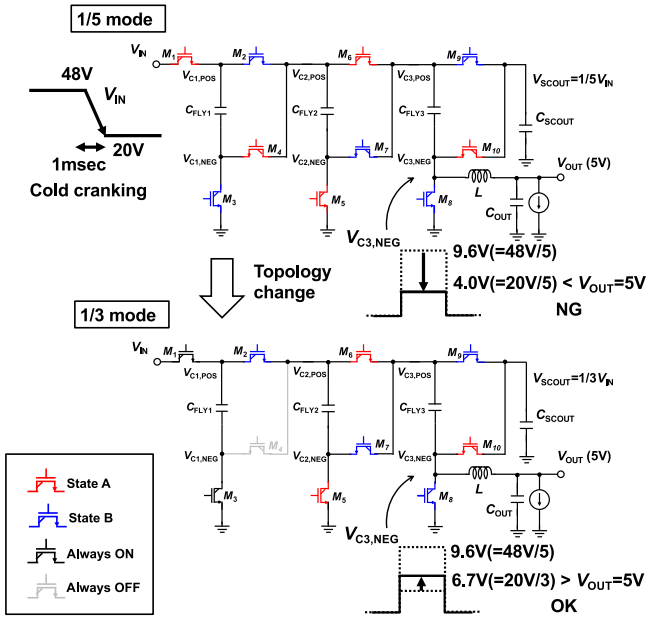


Fig. 9. Converter topology change from 1/5 mode to 1/3 mode in the proposed FH dc–dc converter.

To solve the problem, ACCD is proposed. In ACCD, when V_{IN} drops less than 31 V, both the converter topology and the duty ratio of the PWM signal automatically change. Specifically, the converter topology changes from 1/5 SC dc–dc converter to 1/3 SC dc–dc converter and the duty ratio of the PWM signal decreases 3/5 times, thereby achieving the constant 5-V V_{OUT} with constant f_{SW} under cold cranking. The duty ratio change, as well as the converter topology change, is required, because the converter topology change suddenly increases $V_{C3,NEG}$ 5/3 times and V_{OUT} is suddenly increased. Subsequently, when V_{IN} recovers more than 31 V, the converter topology changes from 1/3 SC dc–dc converter to 1/5 SC dc–dc converter and the duty ratio of the PWM signal increases 5/3 times. As shown in Fig. 7, V_{IN} drop is detected by the ACCD controller by monitoring V_{SCOUT}, and the ACCD controller gives the topology control (TC) signal to a gate signal logic and a programmable ramp generator to change both the converter topology and the duty ratio.

The circuit implementation of ACCD is explained. Fig. 9 shows the converter topology change from 1/5 mode to 1/3 mode in the proposed FH dc–dc converter. By always turning ON M_1 and M_3 and turning OFF M_4, 1/5, the Fibonacci SC dc–dc converter changes to 1/3 Fibonacci SC dc–dc converter. In 1/3 mode, under cold cranking, the FH dc–dc converter can keep 5-V V_{OUT} under cold cranking, because the amplitude of $V_{C3,NEG}$ of 6.7 V (= 20 V/3) is larger than 5 V. In 1/3 mode, the proposed bootstrap circuit, shown in Fig. 8, still works. In 1/3 mode, though the efficiency of the FH dc–dc converter is degraded by the always-ON M_1, the efficiency degradation is not an issue, because cold cranking is an instant event.

Fig. 10 shows a circuit schematic of the ACCD controller. To detect V_{IN} drop, resistor-divided V_{SCOUT} is sample-and-held and compared with V_{REF3} by a clocked comparator, because $V_{C3,NEG}$ is the most important node for the buck converter, and

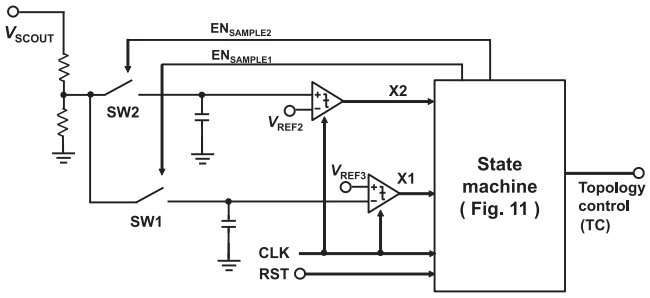


Fig. 10. Circuit schematic of ACCD controller.

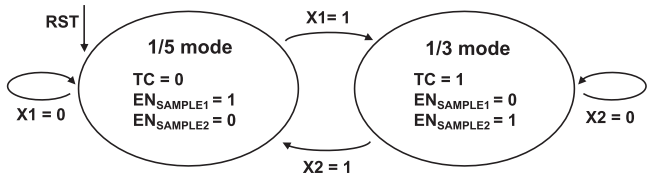


Fig. 11. State machine in ACCD controller.

V_{SCOUT} is the dc voltage that determines $V_{\mathrm{C3,NEG}}$. V_{REF3} is designed to detect 80% duty ratio of $V_{\mathrm{C3,NEG}}$, which corresponds to V_{IN} of 31 V ($=5$ V/0.8 $\times$ 5). Fig. 11 shows a state machine in the ACCD controller. At first, the state machine is in 1/5 mode and TC $=0$. When V_{IN} drops less than 31 V, X1 changes from 0 to 1 and TC changes from 0 to 1. As a result, the state machine changes from 1/5 mode to 1/3 mode, the converter topology changes from 1/5 SC dc–dc converter to 1/3 SC dc–dc converter, and the duty ratio of the PWM signal decreases 3/5 times. When V_{IN} recovers more than 31 V, X2 changes from 0 to 1, TC changes from 1 to 0, and the state machine changes from 1/3 mode to 1/5 mode.

Fig. 12(a) shows a circuit schematic of the programmable ramp generator, which is a relaxation oscillator where a capacitor (C_{RAMP}) is charged by a constant current (I_{RAMP}), and the output (V_{RAMP}) is reset to 0 V when V_{RAMP} crosses V_{REF4} or V_{REF5}. The design target of the programmable ramp generator is to change the duty ratio of the PWM signal 3/5 times or 5/3 times with constant f_{SW} depending on the TC signal. For example, to decrease the duty ratio of the PWM signal 3/5 times at constant f_{SW}, both the gradient and the amplitude of V_{RAMP} is increased 5/3 times. The gradient of V_{RAMP} is increased 5/3 times by increasing I_{RAMP} 5/3 times and the amplitude of V_{RAMP} is increased 5/3 times by changing V_{REF4} to V_{REF5} ($=5/3 \times V_{\mathrm{REF4}}$). Fig. 12(b) shows a timing chart of the FH dc–dc converter with and without the proposed duty ratio change under cold cranking. When V_{IN} drops less than 31 V under cold cranking, TC changes from 0 (1/5 mode) to 1 (1/3 mode) and V_{SCOUT} increases 5/3 times. Without the proposed duty ratio change, V_{OUT} shows overvoltage transient due to the increase of V_{SCOUT}. In contrast, with the proposed duty ratio change, V_{OUT} shows small overvoltage transient, because the increase of V_{SCOUT} is canceled by the 3/5 times duty ratio change.

Fig. 13 shows the simulated V_{OUT} waveforms with and without the proposed duty ratio change under cold cranking. The proposed duty ratio change successfully reduces V_{OUT} transient from $+490$ mV/-0 mV to $+81$ mV/-200 mV.

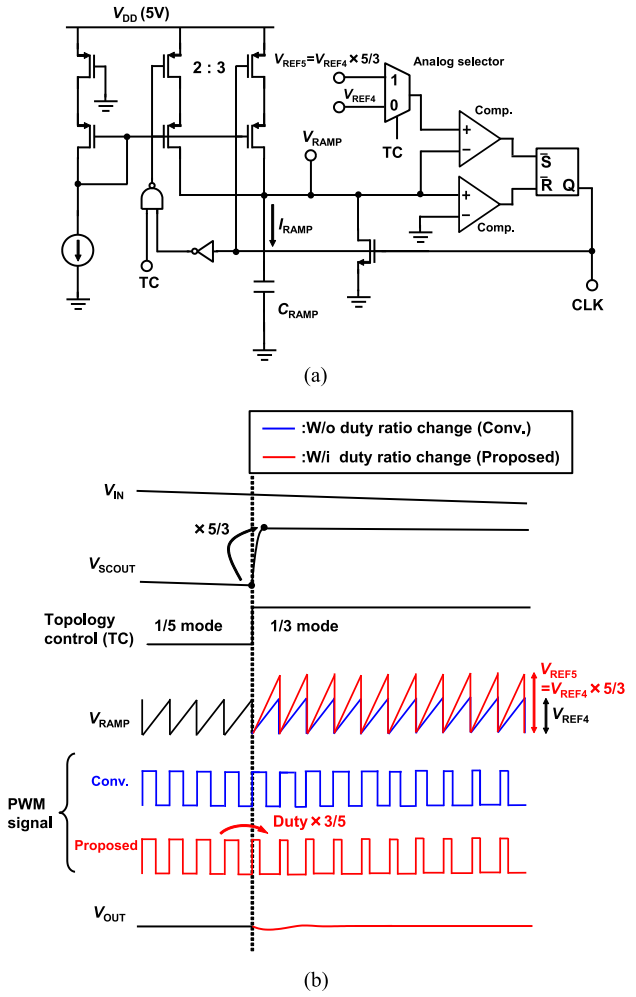


Fig. 12. (a) Circuit schematic of programmable ramp generator. (b) Timing chart of FH dc–dc converter with and without the proposed duty ratio change under the cold cranking.

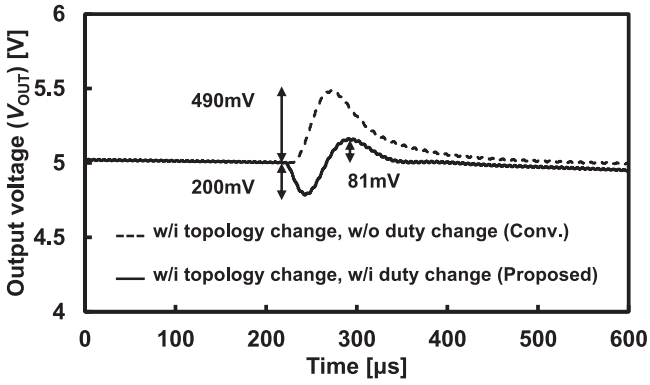


Fig. 13. Simulated V_{OUT} waveforms with and without the proposed duty ratio change under topology change during cold cranking.

IV. Chip Implementation and Measurements

Fig. 14 shows a micrograph of the proposed FH dc–dc converter IC, including ten power transistors, gate drivers, bootstrap circuits, and the controller, fabricated with a 180-nm BCD process. To reduce the volume of the FH dc–dc converter, all transistors and diodes are fully integrated on a 4.6 mm $\times$ 2.3

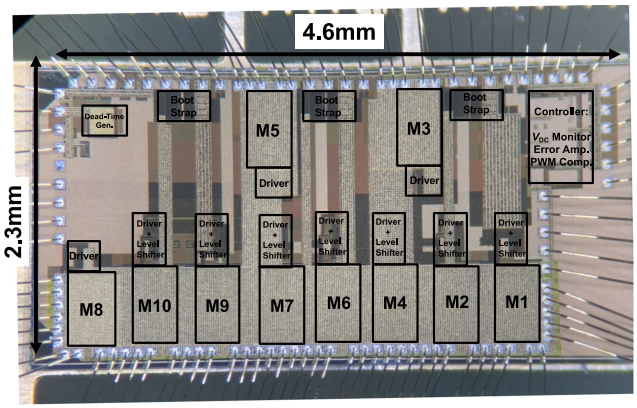


Fig. 14. Micrograph of the proposed FH dc–dc converter IC fabricated with 180 nm BCD process.

TABLE II
DETAILS OF INDUCTOR AND CAPACITORS

Name	Model Number	Value	Rating	Size	ESR
L	TDK:VLCF4028T-101MR33-2	100μH	550mA	4.0mm x 4.0mm x 2.8mm	870mΩ
C_{OUT}	Murata:GRM188R60J476ME15D	47μF	6.3V	1.6mm x 0.8mm x 0.8mm	3mΩ
C_{FLY1}, C_{FLY2}, C_{FLY3}, C_{SCOUT}	Murata:GRM188R6YA106MA73D	10μF	35V	1.6mm x 0.8mm x 0.8mm	10mΩ
$C_{BOOT,M1}$, $C_{BOOT,M2}$, $C_{BOOT,M4}$, $C_{BOOT,M6}$, $C_{BOOT,M7}$, $C_{BOOT,M9}$, $C_{BOOT,M10}$	Murata:GRM1885C1H102GA01D	1nF	50V	1.6mm x 0.8mm x 0.8mm	10mΩ

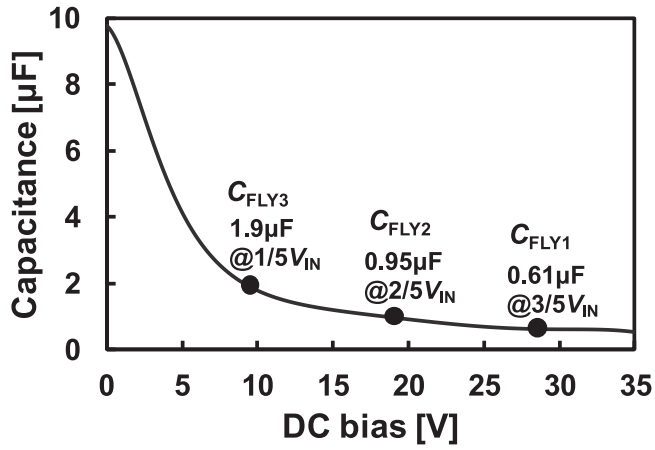


Fig. 15. DC bias dependence of capacitance of 10-μF capacitors used for C_{FLY1}, C_{FLY2}, and C_{FLY3}.

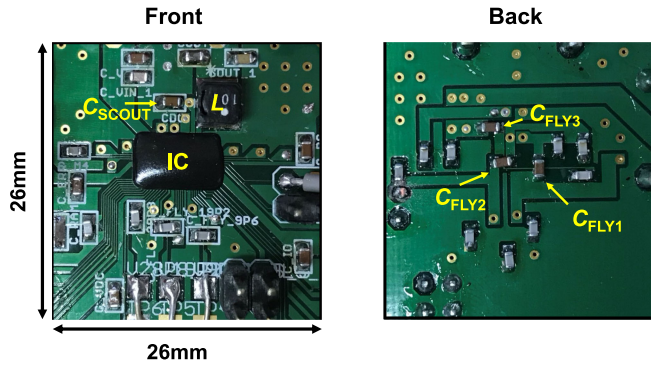


Fig. 16. Partly enlarged photograph of PCB for the proposed FH dc–dc converter IC.

mm IC. In the IC implementation, three types of transistors are used. Lateral double-diffused MOSFETs (LDMOSs) with the 60-V rated drain-to-source voltage and the 5-V rated gate-to-source voltage are used for nine power transistors except for M_8. LDMOS with the 20-V rated drain-to-source voltage and the 5-V rated gate-to-source voltage are used for M_8 because the drain-to-source voltage of M_8 is less than 9.8 V ($= 1/5\ V_{\mathrm{IN}}$) and the 20-V rated LDMOS has lower ON-resistance than the 60-V rated LDMOS at a fixed IC area. MOSFETs with the 5-V rated drain-to-source voltage and the 5-V rated gate-to-source voltage are used for all circuits except ten power transistors.

An inductor (L) and all capacitors are put on PCB. In total, 21 capacitors shown in Figs. 7 and 8 are used. Table II shows the model number, value, rating, size, and equivalent series resistance (ESR) of the inductor and the capacitors. The size of the capacitors is 1.6 mm × 0.8 mm × 0.8 mm. Note that ESR of L is much higher than that of the capacitors, which indicates that using a lot of capacitors will not degrade the efficiency of the hybrid dc–dc converter.

Also note that the capacitance value in Table II is not actually available in the FH dc–dc converter, because the ceramic capacitors have bias-dependence [11]. Fig. 15 shows the dc bias dependence of the capacitance of the 10-μF capacitors used for C_{FLY1}, C_{FLY2}, and C_{FLY3}. The 10-μF capacitor is the maximum capacitance in the 35-V-rated 1608 ceramic capacitors. A substantial decrease from the initial value (10 μF) is observed, 0.61 μF at 28.8 V ($= 3/5\ V_{\mathrm{IN}}$) for C_{FLY1}, 0.95 μF at 19.2 V ($= 2/5\ V_{\mathrm{IN}}$) for C_{FLY2}, and 1.9 μF at 9.6 V ($= 1/5\ V_{\mathrm{IN}}$) for C_{FLY3}. While the capacitance dependence on dc bias voltage is unavoidable in every ceramic capacitor, the choice of identical 10 μF capacitors results in C_{FLY1}: C_{FLY2}: $C_{\mathrm{FLY3}} = 0.61$ μF: 0.95 μF: 1.9 μF. As stated in [11], interestingly, the ratio is accidentally similar to the optimal ratio of C_{FLY1}: C_{FLY2}: C_{FLY3} = 1:1:2 derived from the charge vector analysis theory [32].

Fig. 16 shows a partly enlarged photo of the PCB for the proposed FH dc–dc converter IC. Note that C_{FLY1}, C_{FLY2}, and C_{FLY3} are placed on the backside of the PCB to minimize the parasitic resistance of PCB.

A. *Efficiency*

Fig. 17 shows the measured output current (I_{OUT}) dependence of the efficiency of the proposed FH dc–dc converter IC at V_{IN} of 48 V, V_{OUT} of 5.08 V, and f_{SW} of 78 kHz. I_{OUT} is varied from 10 to 110 mA. The quiescent power of the controller of 6.3 mW ($= 5$ V × 1.26 mA) is included in the efficiency measurement. Peak efficiency of 88% is obtained at I_{OUT} of 90 mA. At the design target of I_{OUT} of 100 mA, the efficiency is 87%.

Fig. 18(a) and (b) shows the measured waveforms of V_{IN}, V_{OUT}, V_{RAMP}, and $V_{\mathrm{C3,NEG}}$ at I_{OUT} of 20 and 100 mA,

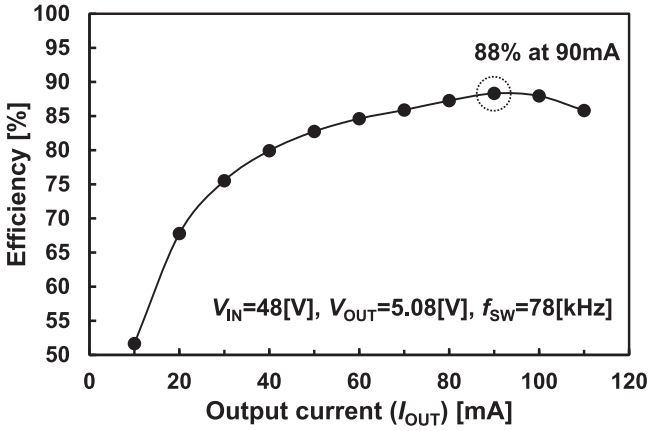


Fig. 17. Measured I_{OUT} dependence of efficiency of the proposed FH dc–dc converter IC.

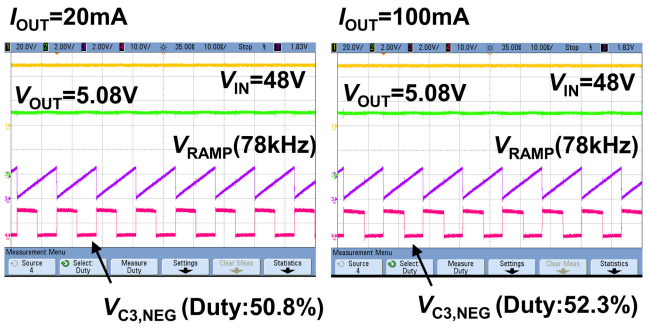


Fig. 18. Measured waveforms of V_{IN}, V_{OUT}, V_{RAMP}, and $V_{\mathrm{C3,NEG}}$ at I_{OUT} of (a) 20 mA and (b) 100 mA.

respectively, at V_{IN} of 48 V and f_{SW} of 78 kHz. V_{OUT} is successfully regulated to 5.08 V at I_{OUT} of 20 and 100 mA. Note that the duty ratio of $V_{\mathrm{C3,NEG}}$ increases from 50.8% [see Fig. 18 (a)] to 52.3% [see Fig. 18 (b)] for the V_{OUT} regulation.

B. V_{OUT} *Regulation Under Cold Cranking*

To demonstrate the effectiveness of the proposed ACCD control to achieve the constant 5-V V_{OUT} under cold cranking at constant f_{SW}, V_{OUT} is measured under cold cranking. Fig. 19(a) and (b) shows the measured waveforms of V_{IN}, V_{OUT}, V_{RAMP}, and $V_{\mathrm{C3,NEG}}$ under the cold cranking at I_{OUT} of 10 mA without and with the proposed ACCD, respectively. V_{IN} drops from 48 to 20 V in 1 ms as the defined test specification of cold cranking [10]. Without the proposed ACCD in Fig. 19(a), after V_{IN} crossed 25 V ($= 5 \times 5$ V), V_{OUT} drops to 0 V, because the duty ratio of $V_{\mathrm{C3,NEG}}$ reaches 100% and the PWM regulation loop fails to work, as explained in Section III-C. In contrast, with the proposed ACCD in Fig. 19(b), when V_{IN} drops less than 31 V, the converter topology automatically changes from 1/5 mode to 1/3 mode and the duty ratio of $V_{\mathrm{C3,NEG}}$ automatically decreases 3/5 times by increasing both the gradient and the amplitude of V_{RAMP} 5/3 times, as explained in Section III-C. Note that the cold-crank transient is a phenomenon in which the input voltage V_{IN} drops from 48 to 20 V in 1 ms [10]. Thus, V_{IN} does not keep a constant voltage around 31 V. Even if V_{IN} remains around 31 V,

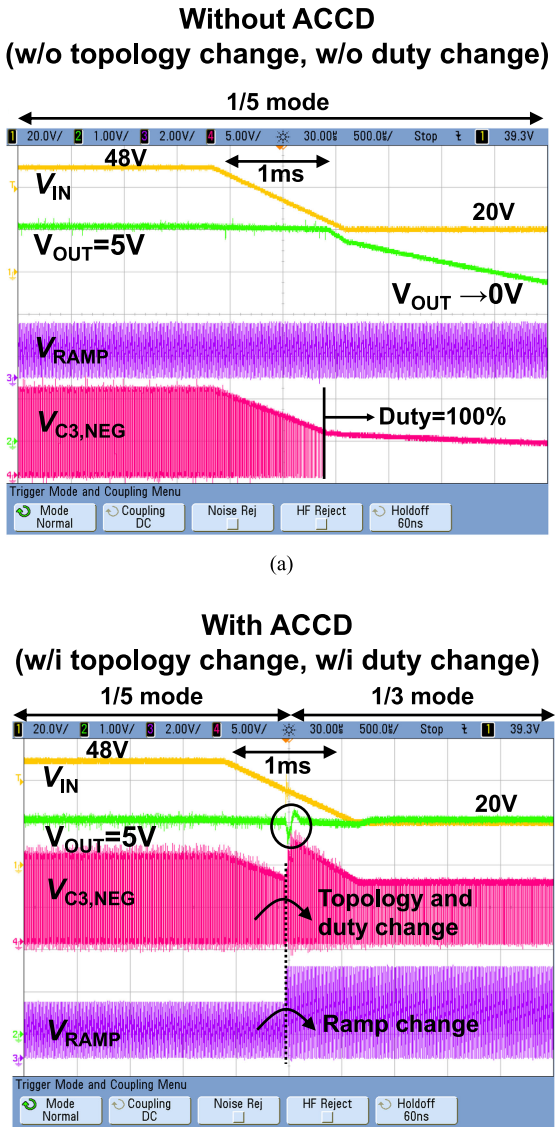


Fig. 19. Measured waveforms of V_{IN}, V_{OUT}, V_{RAMP}, and $V_{\mathrm{C3,NEG}}$ under cold cranking at I_{OUT} of 10 mA. (a) Without ACCD (neither topology change nor duty change). (b) With proposed ACCD (both topology change and duty change).

mode transitions between 1/5 mode and 1/3 mode continue to occur because trigger signals in the mode transitions X1 and X2 are generated from different threshold voltages V_{REF2} and V_{REF3}, as in Fig. 10. Thus, the proposed ACCD controller does not cause the output voltage disturbance. In Fig. 19(b), the sudden increase of $V_{\mathrm{C3,NEG}}$ because of the topology change, and the sudden increase of V_{RAMP} because of the increased amplitude are clearly observed. Because of the proposed ACCD control, the constant 5-V V_{OUT} with constant f_{SW} under the cold cranking is achieved. In Fig. 19(b), the measured V_{OUT} transient is $+214$ mV/-323 mV. The V_{OUT} transient discrepancy between the measurement in Fig. 19(a) and SPICE simulation in Fig. 13 (solid line) is due to the dc bias dependency of flying capacitors C_{FLY1}, C_{FLY2}, C_{FLY3}, and C_{SCOUT}. For example, in the cold crank, as shown in Fig. 9, the circuit topology switches from

TABLE III
COMPARISON WITH STATE-OF-THE-ART 48 V-TO-5 V DC–DC CONVERTER ICS WHERE POWER TRANSISTORS ARE INTEGRATED ON IC

	MAXM17501 [1]	LTC8630 [2]	LM46000 [3]	APEC'16 [6]	JSSC'16 [4]	JSSC'18 [5]	TCAS-I'18 [12]	JSSC'15 [11]	This work
Topology	Buck	Buck	Buck	Buck	Three-level buck	Parallel resonant buck	Switched-capacitor + LDO	Switched-capacitor	Fibonacci hybrid
V_{OUT} regulation	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Technology	BiCMOS	N. A.	N. A.	180nm BCD	0.5μm 120V CMOS	180nm BCD	350nm HV-MOS	140nm SOI BCD	180nm BCD
V_{IN}	12-60V	12-100V	12-100V	48V	12-100V	12-48V	6-60V	37.42V	48V
V_{OUT}	5V	5V	5V	5V	10V	5V	5V	3.3 V	5V
f_{SW}	600kHz	PFM 100-700kHz	200kHz	10MHz	2 MHz	9-25MHz	100-180kHz	52-100kHz	78kHz
L	47μH	47μH	100μH	500nH	1.5μH	1.5μH, 300nH	None	None	100μH
Max. I_{OUT}	500mA	600mA	1.0A	300mA	500mA	500mA	400mA	42.2 mA	110mA
Max. P_{OUT}	2.0W	1.2W	5.0W	1.5W	5.0W	5.0W	2.0W	0.14W	0.55W
Efficiency @I_{OUT}=100mA (48V-to-5V)	65%	75%	80%	60 %	N. A. (75%@100mA, 48V-to-10V)	N.A. (55%@300mA, 48V-to-5V)	N. A. (53%@250mA, 48V-to-5V)	N.A. (95.5%@21mA, 37.42V-to-3.3V)	87%
Max. efficiency (48V-to-5V)	83% @450mA	84% @400mA	85% @1A	64% @150mA					88% @90mA
Number of external L and C	2	3	3	3	3	3	5	5	22
Volume of external L* and C	126 mm^3 (L Only)	235 mm^3 (L Only)	428 mm^3 (L Only)	N.A.	N. A.	N.A.	N.A.	5.1 mm^3 (C x 5)	66mm^3 (L + C x 21)

∗ Recommended in evaluation board.

1/5 mode to 1/3 mode, and the dc voltage applied to C_{SCOUT} changes from 6 V (= 31 V/5) to 10 V (= 31 V/ 3). As a result, due to the dc voltage dependence of the MLCC capacitance shown in Fig. 15, the capacitance of C_{SCOUT} changes from 3.4 to 1.8 μF. Unfortunately, the SPICE model for capacitors taking into account the dc voltage dependence is not available, and SPICE simulation in Fig. 15 was performed with a constant capacitance of $C_{\mathrm{SCOUT}} = 1.9\,\mu$F for the nominal 1/5 mode condition. SPICE simulation with the dc voltage dependence of capacitance is a future design challenge.

V. COMPARISON WITH CONVENTIONAL 48 V-TO-5 V DC–DC CONVERTER ICS INTEGRATING POWER TRANSISTORS

In Table III, the proposed FH dc–dc converter IC is compared with the state-of-the-art 48 V-to-5 V dc–dc converter ICs where the power transistors are integrated on IC. The volume of passive components is calculated by the volume of inductors for the buck converters, capacitors for the SC dc–dc converters, and inductors and capacitors for the hybrid converters. Note that to simplify the comparison, we discuss the volume of external passive components necessary in the main circuit and gate drivers in Table III, excluding external passive components for compensators. In this work, the volume of passive components, including one inductor and 21 capacitors, is 66 mm^3.

As described in Section I, the SC dc–dc converter does not achieve the V_{OUT} regulation at constant f_{SW}, though the SC dc–dc converter [11] achieves the highest efficiency with the smallest volume. The buck converters [4]–[6] in Table III with f_{SW} of above 2 MHz suffer from the efficiency degradation.

Compared with previous publications, the proposed 0.55 W, 48 V-to-5 V FH dc–dc converter IC achieved the highest efficiency (88%) with the smallest volume of passive components (66 mm^3) at the lowest switching frequency (78 kHz).

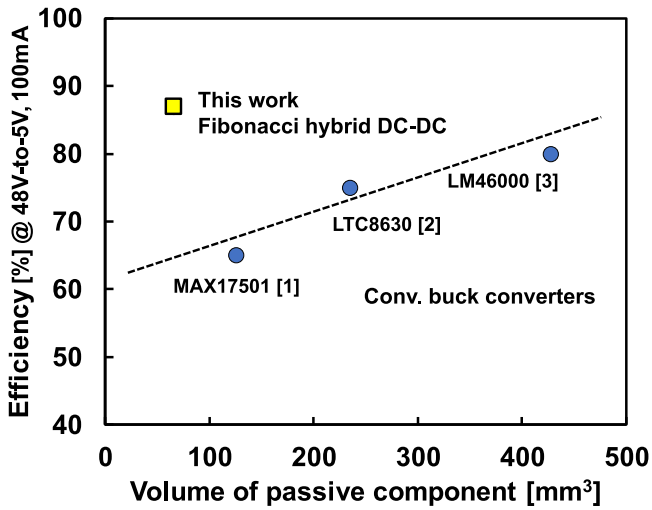


Fig. 20. Efficiency of 48 V-to-5 V dc–dc converters at I_{OUT} of 100 mA and volume of passive components in commercially available buck converter ICs [1]–[3] and proposed FH dc–dc converter IC.

Fig. 20 shows the efficiency of the 48 V-to-5 V dc–dc converters at I_{OUT} of 100 mA and the volume of passive components in the commercially available buck converter ICs [1]–[3] and the proposed FH dc–dc converter IC. As described in Section I, the buck converter ICs show a clear tradeoff between the efficiency and the volume. In contrast, the proposed FH dc–dc converter IC solves the tradeoff. Compared with the conventional buck converter, the required voltage rating of the power transistors in the hybrid dc–dc converters is reduced, and the loss due to the power transistors is also reduced [34].

VI. Conclusion

To meet the requirements for 48 V mild hybrid vehicles, a 0.55 W, 88%, 78 kHz, 48 V-to-5 V FH dc–dc converter IC is proposed. The proposed ACCD enables the constant 5-V V_{OUT} under cold cranking. Compared with previous publications, the proposed 48 V-to-5 V FH dc–dc converter IC achieved the highest efficiency (88%) with the smallest volume of passive components (66 mm^3) at the lowest switching frequency (78 kHz).

Acknowledgment

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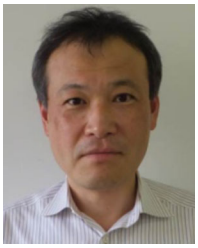

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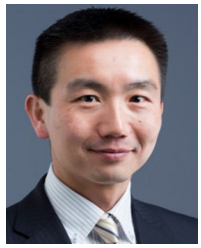

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