Digital Gate Driving (DGD) is Double-Edged Sword: How to Avoid Huge Voltage Overshoots Caused by DGD for GaN FETs

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***Abstract*— In this paper, a problem of huge voltage overshoots ($V_{OVERSHOOT}$) of V_{DS} in GaN FETs, which rarely happens during an automatic search of optimum gate driving parameters in a digital gate driving (DGD), is clarified for the first time, and a solution to avoid the problem is proposed. The highest $V_{OVERSHOOT}$ in 165k measurements, where parameters of 6-bit DGD IC in 6 time slots in 3.3-ns time intervals are randomly changed in the turn-off of GaN FET at 20 V and 10 A, is 27.6 V, which is 115 % larger than the conventional single-step gate driving (CSG) and is almost equal to the maximum rated voltage of the GaN FET. To solve the problem, a safe and fast search method of optimum parameters for DGD is proposed, which achieved 61 % reduction of the switching loss and 59 % reduction of $V_{OVERSHOOT}$ compared with CSG.**

Keywords*— *digital gate drive, GaN FET, switching loss, overshoot

I. Introduction

Fast switching of GaN FETs reduces the switching loss (E_{LOSS}), while current overshoot ($I_{OVERSHOOT}$) and voltage overshoot ($V_{OVERSHOOT}$) increase, which is a critical problem in GaN FETs, because a huge overshoot that exceeds the maximum rating of GaN FETs causes serious device damage. Active gate driving [1] and digital gate driving (DGD) [2-3] are important technologies to reduce both $V_{OVERSHOOT}$ and E_{LOSS} in GaN FETs. The advantage of DGD is its programmability in supporting a wide variety of power devices [4] and its ease of use, because the parameters of DGD can be automatically optimized using software [4-5].

In this paper, however, it is shown for the first time that DGD is a double-edged sword. As far as the authors know, no previous papers show the risk of DGD. Specifically, DGD with good parameters achieves lower $V_{OVERSHOOT}$ and E_{LOSS} than the conventional single-step gate driving (CSG), while DGD with bad parameters causes higher $V_{OVERSHOOT}$ and E_{LOSS} than CSG, which suggests a risk of overvoltage breakdown of GaN FETs during the random parameter search process for DGD. In order to understand the cause of the problem and to avoid it, in this paper, the principle of huge $V_{OVERSHOOT}$ generation is analyzed and a safe and fast search method for the parameters, that achieves low E_{LOSS} and $V_{OVERSHOOT}$ without generating huge $V_{OVERSHOOT}$, is proposed.

II. Digital Gate Driver IC for GaN FETs [6]

Figs. 1 and 2 show a circuit schematic and a timing chart of the developed 5 V, 300 MSa/s, 6-bit DGD IC for GaN FETs, respectively. The IC is designed using only 5 V transistors and requires a single power supply of 5 V. The gate current (I_G) can be varied in 64 levels for each of the 16 3.3-ns time intervals during turn-on/off of the GaN FETs depending on scan-in data. 64-level I_G control from 0 A to 5 A in 80 mA increments is achieved by selectively turning on or off six nMOSFETs or pMOSFETs with binary weighted gate widths ($1W_N$, $2W_N$, $4W_N$, $8W_N$, $16W_N$, and $32W_N$ in case of nMOSFETs) in the output stage with 6-bit digital signals. I_G control in 3.3-ns intervals is required, because the turn-on/off

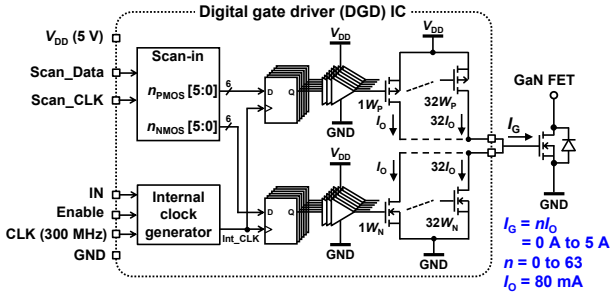


Fig. 1. Circuit schematic of 5 V, 300 MSa/s, 6-bit DGD IC for GaN FETs.

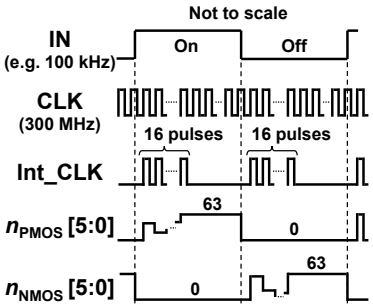


Fig. 2. Timing chart of 5 V, 300 MSa/s, 6-bit DGD IC for GaN FETs.

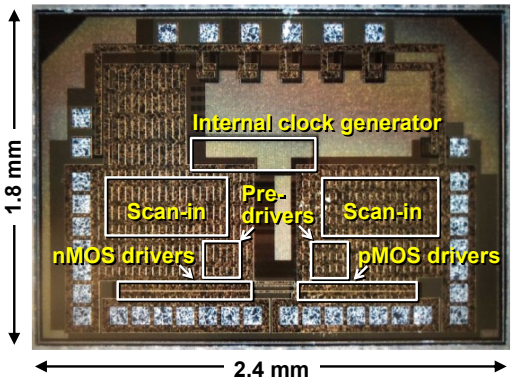


Fig. 3. Die photo of DGD IC fabricated with 180-nm BCD process.

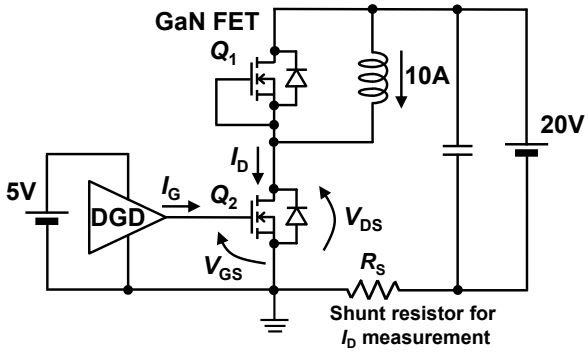


Fig. 4. Circuit schematic of fabricated GaN half bridge.

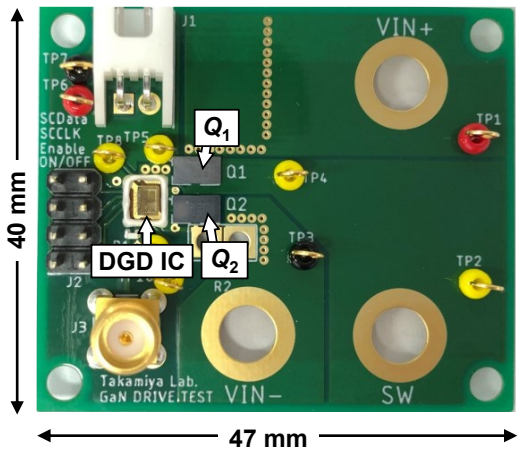


Fig. 5. PCB of GaN half bridge.

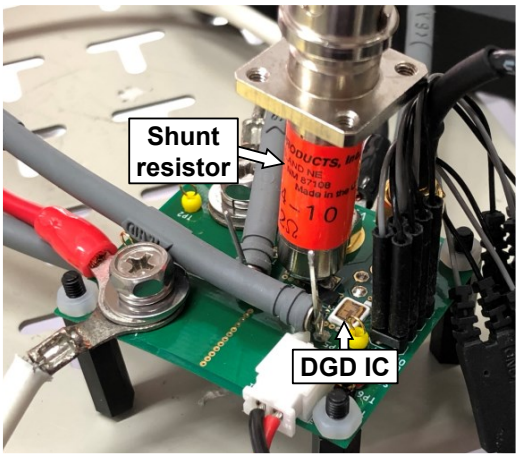


Fig. 6. Measurement setup of GaN half bridge for double pulse test.

transient of GaN FETs is typically less than 10 ns. The 3.3-ns interval is defined by an externally supplied 300-MHz clock signal (CLK). To increase the clock frequency to 300 MHz, the need for high-speed digital data input is eliminated and the required digital data is pre-stored in on-chip memory (flip-flops) by the scan-in circuit.

Fig. 3 shows a die photo of the developed DGD IC fabricated with 180-nm BCD process. The die size is 1.8 mm by 2.4 mm.

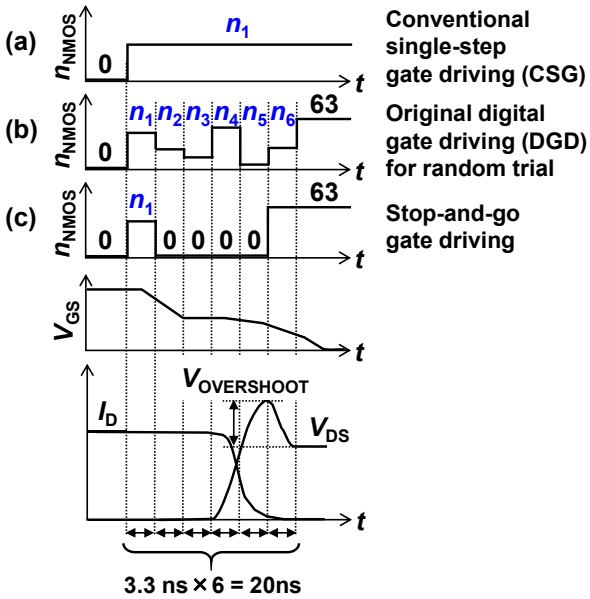


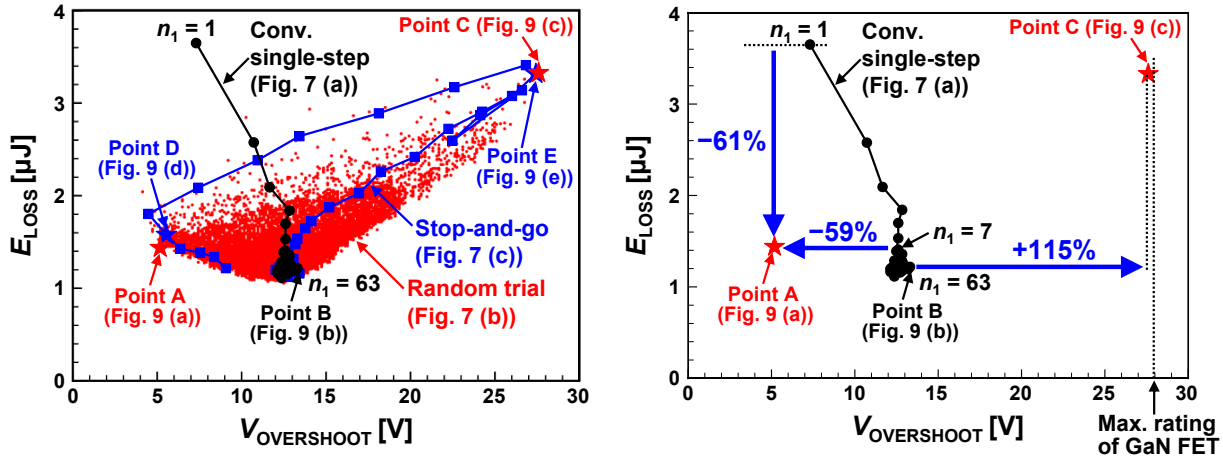
Fig. 7. Three types of gate driving vectors (GVs) compared in this paper.

III. Voltage Overshoot and Switching Loss in DGD for GaN FETs

In order to investigate the relationship between $V_{OVERSHOOT}$ and E_{LOSS} in DGD with different parameters, the switching characteristics of GaN FETs are measured by double pulse tests. Figs. 4 to 6 show a circuit schematic, a photo of PCB, and a measurement setup of the GaN (EPC2030, 40 V, 48 A) half bridge for the double pulse test at 20 V and 10 A, respectively. I_D was measured using a high-bandwidth shunt resistor (SDN-414-10, T&M Research Products), and V_{GS} and V_{DS} were measured using high voltage differential probes (BUMBLEBEE, PMK).

In this paper, only turn-off is discussed, because the measured maximum $I_{OVERSHOOT}$ at turn-on is 11 A, which is much smaller than the maximum rated pulse current of the GaN FET of 490 A. Fig. 7 shows the definition of three types of DGD compared in this paper. n_{NMOS} is an integer from 0 to 63 indicating I_G at turn-off and $I_G = n_{NMOS} \times 80$ mA. Fig. 7 (b) shows the original gate driving vectors (GVs) for DGD with 6 time slots. In this paper, GVs are defined as (n_1, n_2, …, n_6), where n_1, n_2, and n_6 are integers from 0 to 63. Six 3.3-ns time intervals are used. Fig. 7 (c) shows GVs of the stop-and-go gate driving [7] with only one variable (n_1), which was proposed to reduce the test cost to find optimum GVs. Fig. 7 (a) shows GVs of CSG for comparison.

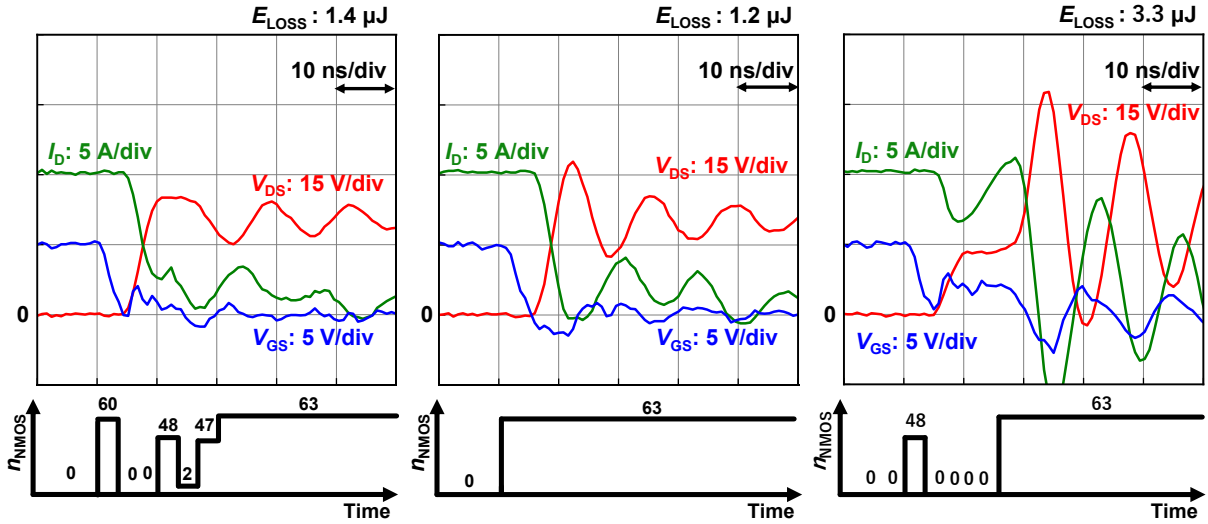
Fig. 8 shows the measured E_{LOSS} and $V_{OVERSHOOT}$. The black line shows the trade-off curve of CSG with varied n_1 from 1 to 63, where E_{LOSS} decreases and $V_{OVERSHOOT}$ increases with increasing n_1. Point B shows the measured point at n_1 = 63. The red small dots show 165k measurements of the random trial of the original GVs with 6 time slots in Fig. 7 (b), where GVs in 6 time slots are randomly changed to investigate the range of E_{LOSS} and $V_{OVERSHOOT}$ covered by the original GVs. They are meaningful measurements to give an overview of the range of E_{LOSS} and $V_{OVERSHOOT}$, though the 165k measurements covers only less than 0.0003 % of the number



(a) Measured points and trajectories

(b) Improvement and deterioration results

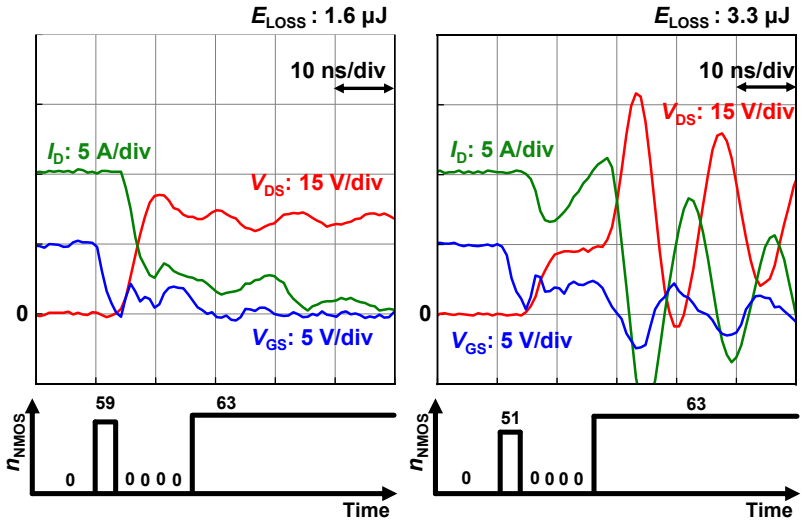
Fig. 8. Measured E_{LOSS} vs. $V_{OVERSHOOT}$ of conventional single-step gate driving, digital gate driving for random trial, and stop-and-go gate driving.



(a) Point A

(b) Point B

(c) Point C



(d) Point D

(e) Point E

Fig. 9. Gate vectors and measurement waveforms at each measured point.

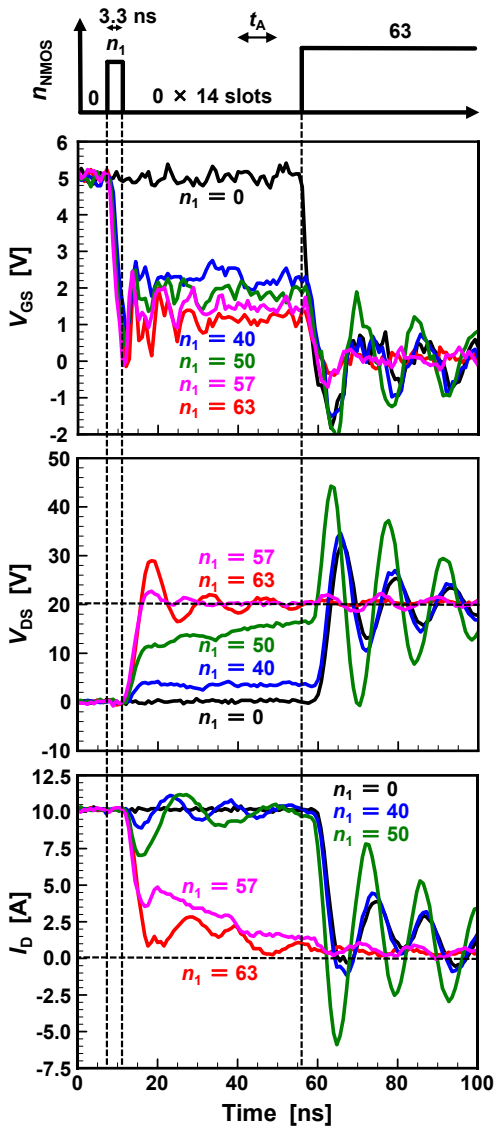


Fig. 10. GV and measured waveforms with varied n_1 in stop-and-go gate driving.

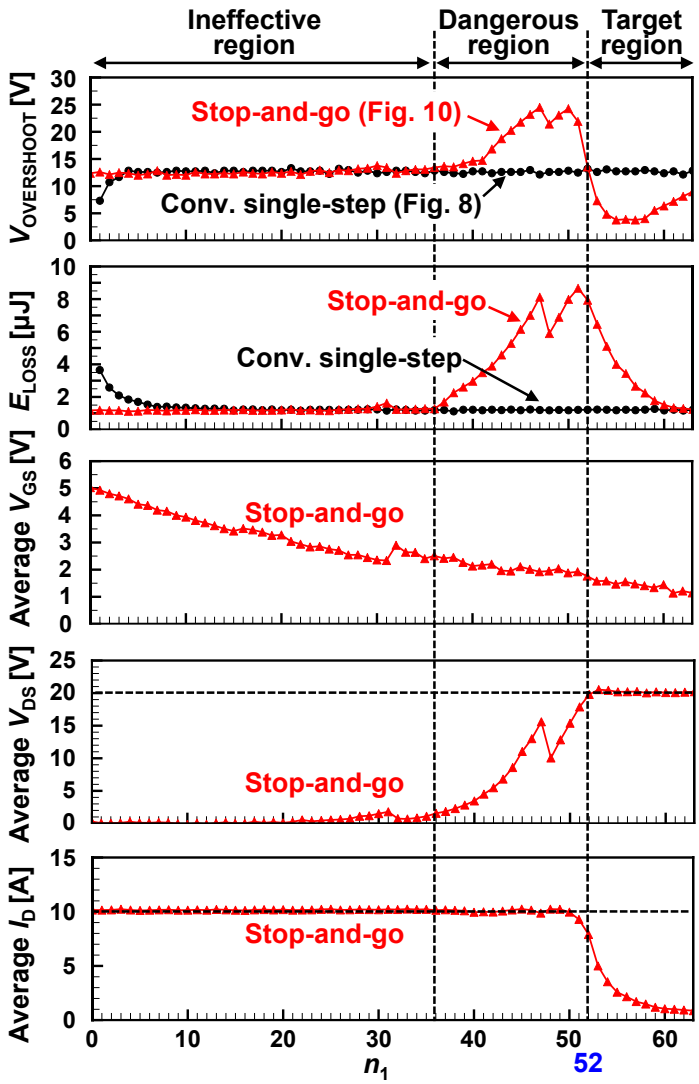


Fig. 11. measured n_1 dependence of $V_{OVERSHOOT}$, E_{LOSS}, average V_{GS}, average V_{DS}, and average I_D.

of combinations of 64^6 (~ 69G) in 6-bit and 6-slot GVs. Point A shows the best measured point achieving both small E_{LOSS} and low $V_{OVERSHOOT}$, while Point C shows the worst measured point with the highest $V_{OVERSHOOT}$. As shown in Fig. 8 (b), compared with CSG, Point A reduces E_{LOSS} by 61 % at the similar $V_{OVERSHOOT}$ and reduces $V_{OVERSHOOT}$ by 59 % at the same E_{LOSS}. $V_{OVERSHOOT}$ of Point C is 27.6 V and V_{DS} reaches 47.6 V, which is almost equal to the maximum rated voltage of 48 V and the GaN FET could be destroyed. Compared with Point B, Point C increases $V_{OVERSHOOT}$ by 115 %.

Figs. 9 (a) – (c) show the GVs and measured waveforms of Point A to Point C, respectively. In Fig. 9 (a), V_{GS} increases temporarily when GV changes from 60 to 0, dI_D / dt is reduced, and $V_{OVERSHOOT}$ is reduced. In contrast, in Fig. 9 (c), V_{GS} increases temporarily when GV changes from 48 to 0, the GaN FET is turned-on again, and V_{DS} stays at halfway voltage (13 V). After that, the highest $V_{OVERSHOOT}$ is generated when GV changes from 0 to 63, because the turn-off voltage overshoot is added to the halfway voltage.

The meaning of GVs of Point A and Point C is discussed. Interestingly, GVs of both Point A and Point C include a lot of zeros. Specifically, GV of Point A includes two zeros between 60 and 48, and GV of Point C includes four zeros between 48 and 63. The stop-and-go gate driving [7] in Fig. 7 (c) also include a lot of zeros and the driving with only one variable (n_1) may be used to understand the cause of the problem of Point C, because the original GVs with 64^6 combinations is too complicated to understand.

The blue line in Fig. 8 (a) shows the stop-and-go gate driving in Fig. 7 (c) varied n_1 from 0 to 63. Interestingly, the blue line covers most of the red small dots, which suggests that the only 64 measurements with the stop-and-go gate driving cover most of E_{LOSS} and $V_{OVERSHOOT}$ of 165k measurements with the original GVs. The blue line also covers Point A to Point C. Point D and Point E are the measured points of the stop-and-go gate driving close to Point A and Point C, respectively, and their GVs and measured waveforms are shown in Figs. 9 (d) and (e). The only difference in GVs

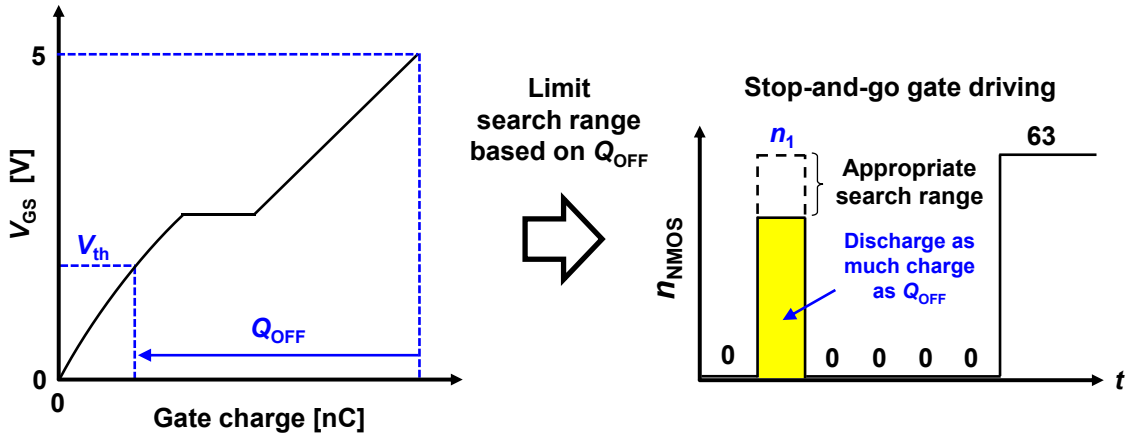


Fig. 12. Safe and fast search method of optimum GVs for DGD with discharging gate charge more than Q_{OFF} in the period of n_1.

between Point D and Point E is n_1, which suggests that n_1 in the stop-and-go gate driving is an important parameter to determine $V_{OVERSHOOT}$ and E_{LOSS} in DGD.

IV. How to Avoid Huge Voltage Overshoots

In order to analyze n_1 dependence of $V_{OVERSHOOT}$ and E_{LOSS}, Fig. 10 shows the GV and measured waveforms with varied n_1 in the stop-and-go gate driving and Fig. 11 shows the measured n_1 dependence of $V_{OVERSHOOT}$, E_{LOSS}, average V_{GS}, average V_{DS}, and average I_D. Fig. 11 also includes CSG for comparison. Instead of the four zero segments in Fig. 7 (c), 14 zero slots are used to analyze the steady state of V_{GS}, V_{DS}, and I_D in detail. The voltage and current averaging is carried out for the period of t_A shown in Fig. 10. Fig. 11 can be classified into three regions including an ineffective region, a dangerous region, and a target region. In the ineffective region, n_1 does not work effectively. In the dangerous region, both $V_{OVERSHOOT}$ and E_{LOSS} increase, because the average V_{DS} is increased, while the average I_D is constant. In the target region, $V_{OVERSHOOT}$ is less than that of CSG, because the GaN FET is turned-off in the period of n_1 and the average I_D is reduced.

In this case, the boundary between the dangerous region and the target region is n_1 of 52, which can be explained by the device characteristics. The discharged gate charge by DGD in the period of n_1 is 13.7 nC (= 52 × 80 mA × 3.3 ns), while the gate charge required to discharge from V_{GS} = 5 V to V_{GS} = 1.5 V (= threshold voltage V_{th}) is 13.9 nC according to the gate charge curve [8]. Both values are consistent and reasonable. This gate charge is defined as Q_{OFF} shown in Fig. 12 and the stop-and-go gate driving with discharging the same amount of charge as Q_{OFF} in the period of n_1 operates at the boundary between the dangerous region and the target region. In conclusion, it is important to discharge enough gate charge to turn off the GaN FET in the first time slot of the stop-and-go gate driving to avoid huge $V_{OVERSHOOT}$.

Therefore, in order to achieve low E_{LOSS} and $V_{OVERSHOOT}$ without generating huge $V_{OVERSHOOT}$, the stop-and-go gate driving with discharging the gate charge exceeding Q_{OFF} in the period of n_1 is practical as the safe and fast search method of the optimum GVs for DGD, which suggests that the search range of n_1 should be appropriately limited according to the specifications of GaN FETs and DGD IC as shown in Fig. 12.

V. Conclusions

This paper clarified the risk of DGD, where huge $V_{OVERSHOOT}$ generated during the random parameter search process for DGD could destroy GaN FETs. In order to achieve low E_{LOSS} and $V_{OVERSHOOT}$ without generating huge $V_{OVERSHOOT}$, the stop-and-go gate driving with discharging the gate charge exceeding Q_{OFF} in the period of n_1 is practical as the safe and fast search method for DGD. In the future, the proposed search method will be experimentally demonstrated.

Acknowledgment

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