Equalization of DC and Surge Components of Drain Current of Two Parallel-Connected SiC MOSFETs Using Single-Input Dual-Output Digital Gate Driver IC

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***Abstract*— A single-input, dual-output (SIDO) digital gate driver (DGD) IC, integrating two 6-bit DGDs, two current sensors, and a controller, is proposed to equalize the drain current (I_D) variation of two parallel-connected SiC MOSFETs. The DC and surge components of I_D of each MOSFET are equalized by digitally controlling the gate voltage amplitude and the gate current at turn-on, respectively. In the double pulse test at 300 V and 40 A using two parallel SiC MOSFETs with different threshold voltages of 0.5 V, the proposed SIDO DGD IC reduces the differences in the DC and surge components of I_D of the two MOSFETs from 2.6 A to 0.13 A by 95 % and from 1.9 A to 0.32 A by 83 %, respectively. The automatic equalization of the DC components of I_D of the two MOSFETs using SIDO DGD IC is also successfully demonstrated.**

Keywords*— *Parallel connected, SiC, DC current, Surge current, Gate driver

I. Introduction

In power electronics systems, when large current exceeding the rated current of a power device is applied, it is common to connect multiple power devices in parallel. Due to variations in the characteristics of the power devices, however, the current concentrates in part of the devices and the heat generation due to losses is localized, which degrades the reliability of the power devices. In the conventional method of parallel connection of power devices, the characteristics of the power devices are measured in advance, and power devices with matching characteristics are selected for parallel connection, which will increase the cost. Therefore, a technology to automatically equalize the current of power devices connected in parallel is required. The problem with the previous papers of current equalization is that they require a lot of ICs including such as current sensors [1–2], timing control circuits [1–4], and regulators for gate voltage amplitude control [5–6], which will also increase the cost.

In this paper, a single-input, dual-output (SIDO) digital gate driver (DGD) IC, integrating all necessary circuits including two 6-bit DGDs, two current sensors, and a controller, is proposed to automatically equalize the drain current (I_D) of two parallel-connected SiC MOSFETs. DGD that can digitally control the gate waveform is gaining attention as a technology to reduce both loss and noise during switching of power devices [7]. The proposed SIDO DGD IC will enable a high-performance power electronics systems using SiC MOSFETs at low cost, because SiC MOSFETs with large variations can be connected in parallel without prior testing and selection.

II. Proposed Drain Current Equalization Using SIDO DGD IC

Fig. 1 shows a circuit schematic of the fabricated half-bridge circuit and SIDO DGD IC. The half-bridge consists of three SiC MOSFETs (Q_1 – Q_3 : SCT3030AL, 650V, 70A) including the low-side two-parallel Q_1 and Q_2. In order to equalize DC ($I_{D1,DC}$, $I_{D2,DC}$) and surge ($I_{D1,SURGE}$, $I_{D2,SURGE}$) components of I_D of Q_1 and Q_2 (I_{D1}, I_{D2}) with variations in device characteristics by controlling the gate waveforms, SIDO DGD IC is newly developed. Except for two PCB Rogowski coils [8], all the necessary circuits including two 6-bit DGDs, two current sensors, and a controller are fully integrated into a single chip.

Fig. 2 shows the circuit schematic of the current sensor to measure $I_{D1,DC}$ and $I_{D2,DC}$. The current sensor cannot measure the high-frequency $I_{D1,SURGE}$ and $I_{D2,SURGE}$ waveforms. Two current sensors are integrated on SIDO DGD IC. In order to obtain the current waveform, the output of the PCB Rogowski coil is integrated.

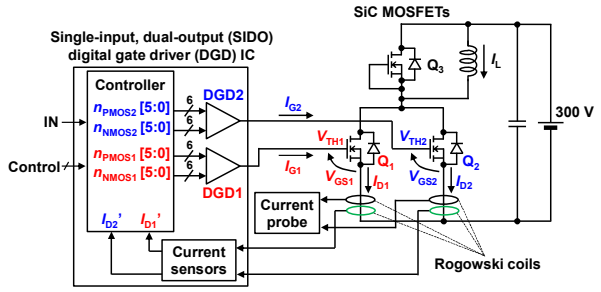

Fig. 1. Circuit schematic of fabricated half-bridge circuit and proposed SIDO DGD IC.

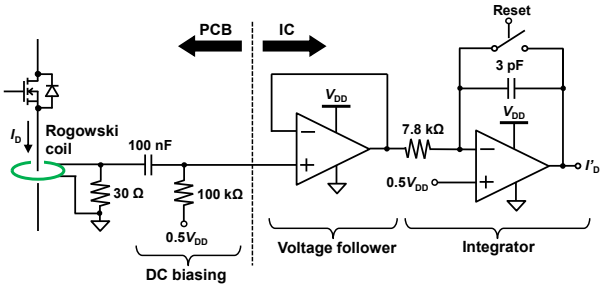

Fig. 2. Circuit schematic of current sensor to measure $I_{D1,DC}$ and $I_{D2,DC}$.

SIDO DGD IC has 24 bits of control bits. n_{PMOS1} [5:0] and n_{NMOS1} [5:0] control the gate current (I_{G1}) for Q_1, while n_{PMOS2} [5:0] and n_{NMOS2} [5:0] control the gate current (I_{G2}) for Q_2. Fig. 3 shows the circuit schematic of DGD1 for Q_1 in Fig. 1. I_{G1} can be varied in 64 levels at turn-on depending on 6-bit digital signals n_{PMOS1} [5:0], which is defined as n_{PMOS1}, where n_{PMOS1} is an integer between 0 and 63. The 64-level I_{G1} control from 0 A to 6 A in 95 mA increments at turn-on of Q_1 is achieved by selectively turning on or off six pMOSFETs with binary weighted gate widths (W_P, $2W_P$, $4W_P$, $8W_P$, $16W_P$, $32W_P$) in the output stage depending on n_{PMOS1} [5:0]. The same design is applied to the turn-off of Q_1 by controlling n_{NMOS1} [5:0].

Fig. 4 shows the timing chart of the proposed SIDO DGD IC. In this paper, the threshold voltage of Q_1 (V_{TH1}) is assumed to be lower than that of Q_2 (V_{TH2}). Among the eight parameters of n_{PMOS1}, n_{NMOS1}, n_{PMOS2}, and n_{NMOS2} in the on and off states of Q_1 and Q_2, n_{NMOS1} in the on state is controlled to equalize $I_{D1,DC}$ and $I_{D2,DC}$ by digitally controlling the gate voltage amplitude, and n_{PMOS2} in the on state is controlled to equalize $I_{D1,SURGE}$ and $I_{D2,SURGE}$ by digitally controlling the gate current at turn-on. Vice versa, if $V_{TH1} > V_{TH2}$, n_{NMOS2} and n_{PMOS1} are controlled.

Fig. 5 shows the conventional gate driving and the proposed gate driving to equalize $I_{D1,DC}$ & $I_{D2,DC}$ and $I_{D1,SURGE}$ & $I_{D2,SURGE}$ using SIDO DGD IC. In the conventional gate driving where the gate drive is identical for Q_1 and Q_2 in Fig. 5 (a), $I_{D1,DC} > I_{D2,DC}$ and $I_{D1,SURGE} > I_{D2,SURGE}$, because of $V_{TH1} < V_{TH2}$. In order to equalize $I_{D1,DC}$ and $I_{D2,DC}$, Fig. 5 (b) shows the V_{GS1} amplitude control by increasing n_{NMOS1} from zero. Fig. 6 shows the principle of operation of the proposed DGD-based

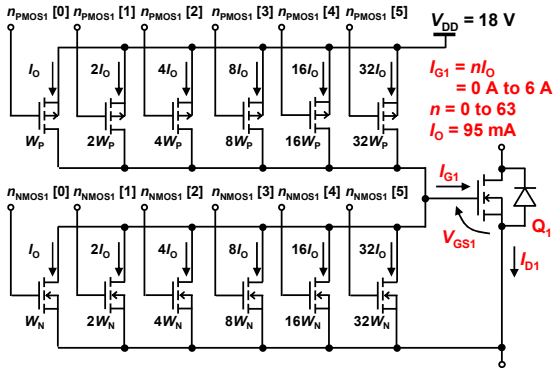

Fig. 3. Circuit schematic of DGD1 for Q_1.

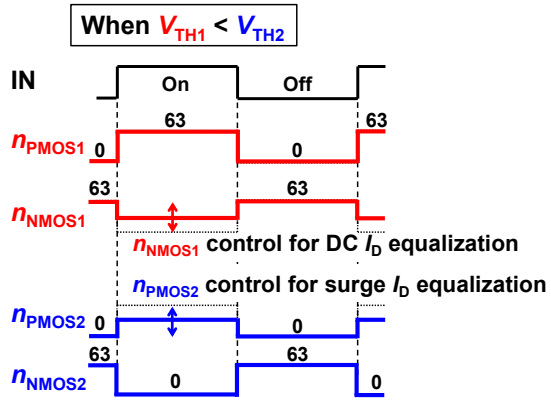

Fig. 4. Timing chart of proposed SIDO DGD IC.

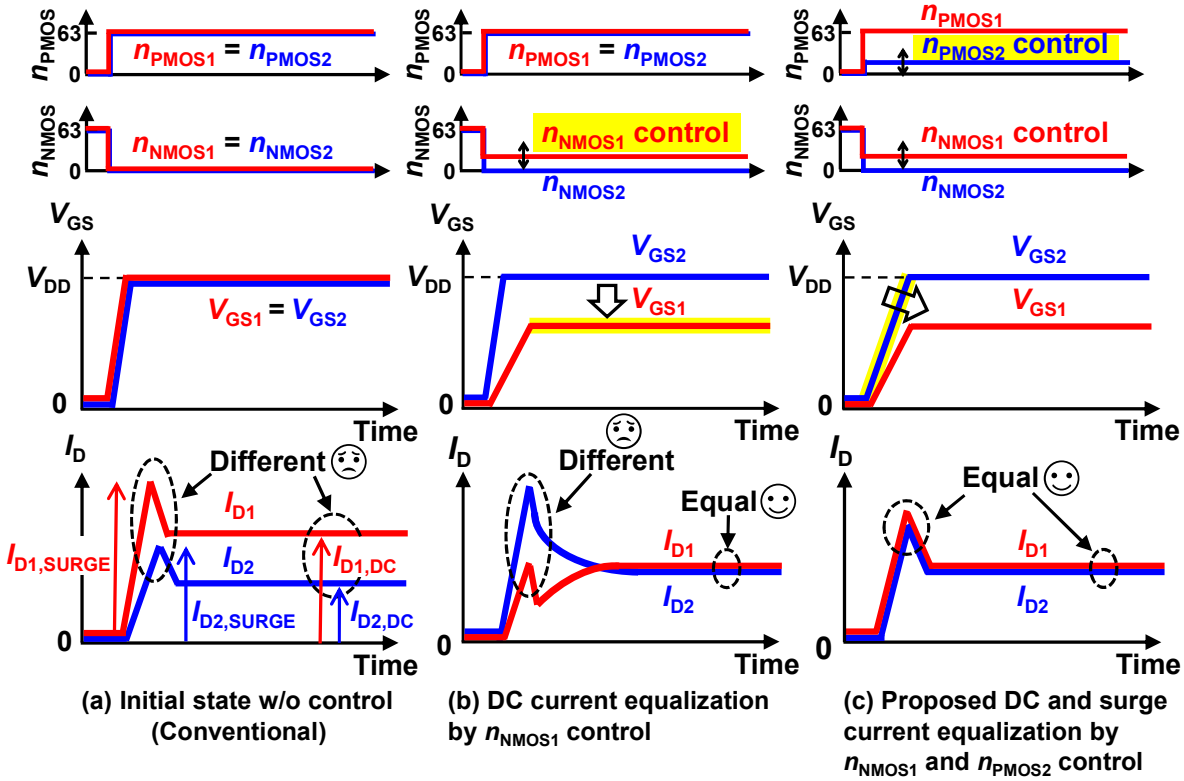

Fig. 5. Conventional gate driving and proposed gate driving to equalize $I_{D1,DC}$ & $I_{D2,DC}$ and $I_{D1,SURGE}$ & $I_{D2,SURGE}$ using SIDO DGD IC.

V_{GS1} amplitude control. In the conventional gate driving in Fig. 6 (a), V_{GS1} is equal to the supply voltage (V_{DD}), because n_{NMOS1} in the on state is zero. In contrast, in the proposed V_{GS1} amplitude control in Fig. 6 (b), V_{GS1} amplitude can be digitally controlled by n_{NMOS1} on the principle of a shunt regulator, where all six pMOSFETs and some of the six nMOSFETs in Fig. 3 are turned on. The IC includes a new circuit technology that solves the large DC power of the shunt regulator. The details, however, will not be discussed in this paper. Fig. 7 shows the flowchart to control n_{NMOS1} and n_{NMOS2} to equalize $I_{D1,DC}$ and $I_{D2,DC}$. The flowchart is implemented in the controller in SIDO DGD IC in Fig. 1. First, when $I_{D1,DC}$ is greater than $I_{D2,DC}$, n_{NMOS1} is incremented from 0. Next, a steady state is reached at the value of n_{NMOS1} where $I_{D1,DC}$ and $I_{D2,DC}$ are equal. Similarly, when $I_{D12,DC}$ is smaller than $I_{D2,DC}$, n_{NMOS2} is incremented from 0. Then, a steady state is reached at the value of n_{NMOS2} where $I_{D1,DC}$ and $I_{D2,DC}$ are equal. In Fig. 5 (b), $I_{D1,DC}$ and $I_{D2,DC}$ are adjusted to be equal, by reducing V_{GS1} amplitude below V_{GS2} amplitude, while $I_{D1,SURGE} < I_{D2,SURGE}$, because $I_{G1} < I_{G2}$ at turn-on due to the increased n_{NMOS1}. Please note that $I_{D1,SURGE} > I_{D2,SURGE}$, in Fig. 5 (a), while $I_{D1,\ SURGE} < I_{D2,SURGE}$, in Fig. 5 (b). In order to equalize $I_{D1,SURGE}$ and $I_{D2,SURGE}$, Fig. 5 (c) shows the proposed gate driving by controlling n_{NMOS1} and n_{PMOS2}. $I_{D1,\ SURGE}$ and $I_{D2,SURGE}$ are equalized by decreasing I_{G2} at turn-on by decreasing n_{PMOS2} from 63. In conclusion, $I_{D1,DC}$ and $I_{D2,DC}$ are equalized by tuning n_{NMOS1}, and $I_{D1,\ SURGE}$ and $I_{D2,SURGE}$ are equalized by tuning n_{PMOS2}.

III. Measured Equalization of DC and Surge Components of Drain Current

Fig. 8 shows a die photo of SIDO DGD IC fabricated with 180-nm BCD process. Fig. 9 shows a photo of PCB of the half bridge. PCB is designed symmetrically so that the parasitic inductances of Q_1 and Q_2 are equal. As shown in Fig. 1, I_{D1} and I_{D2} are measured using two commercial current probes (SS-284A, IWATSU) and our developed two current sensors in DGD IC. The current probes are used in Figs. 11 – 17 to measure I_{D1} and I_{D2} waveforms, while the current sensors are used in Fig. 17 to automatically equalize $I_{D1,DC}$ and $I_{D2,DC}$. Fig. 10 shows the measured $I_D - V_{GS}$ characteristics of Q_1 and Q_2 at $V_{DS} = 10$ V using a curve tracer, where $V_{TH2} - V_{TH1} = 0.5$ V. $I_{D1,DC}$, $I_{D2,DC}$, $I_{D1,SURGE}$, and $I_{D2,SURGE}$ are measured with the double pulse test at 300 V and the load current (I_L) of 5 A, 10 A, 20 A, and 40 A.

Figs. 11 – 13 show the measured n_{NMOS1} dependence of V_{GS1} amplitude, $I_{D1,DC}$ and $I_{D2,DC}$, and $I_{D1,SURGE}$ and $I_{D2,SURGE}$ at $n_{PMOS2} = 63$, respectively, corresponding to the DC current equalization by n_{NMOS1} control shown in Fig. 5 (b). At $I_L = 40$ A, by increasing n_{NMOS1} from 0 to 18, V_{GS1} amplitude reduces from 18 V to 15.9 V (Fig. 11) and the difference between $I_{D1,DC}$ and $I_{D2,DC}$ reduces from 2.6 A to 0.13 A by 95 % (Fig. 12), while the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ increases from 1.9 A to 9.8 A (Fig. 13). To equalize the surge, Fig. 14 shows the measured n_{PMOS2} dependence of $I_{D1,SURGE}$ and $I_{D2,SURGE}$ at $n_{NMOS1} = 18$, corresponding to the proposed DC and surge current equalization by n_{NMOS1} and n_{PMOS2} control shown in Fig. 5 (c). At $I_L = 40$ A, by decreasing n_{PMOS2} from 63 to 28, the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ reduces from 9.8 A to 0.32 A by 97 %. Fig. 15 shows the measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} corresponding to Figs. 5 and 11 – 14 at $I_L = 40$ A. Compared with the conventional gate driving (Fig. 15 (a)), the proposed gate driving (Fig. 15 (c)) with n_{NMOS1} and n_{PMOS2} control reduces the difference between $I_{D1,DC}$ and $I_{D2,DC}$ from 2.6 A to 0.13 A by 95% and the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ from 1.9 A to 0.32 A by 83%.

Fig. 16 shows the measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} corresponding to Figs. 5 and 11 – 14 at $I_L = 20$ A.

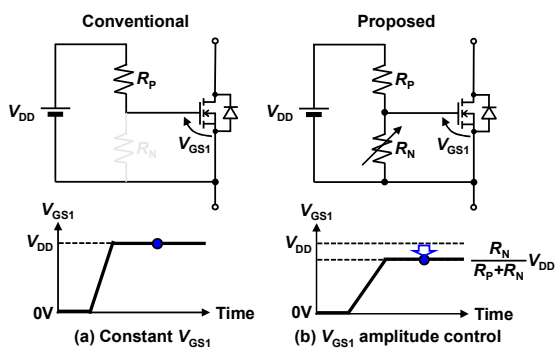

Fig. 6. Principle of operation of proposed DGD-based V_{GS1} amplitude control.

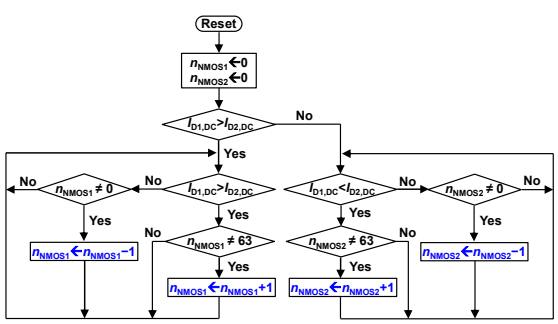

Fig. 7. Flowchart to control n_{NMOS1} and n_{NMOS2} to equalize $I_{D1,DC}$ and $I_{D2,DC}$.

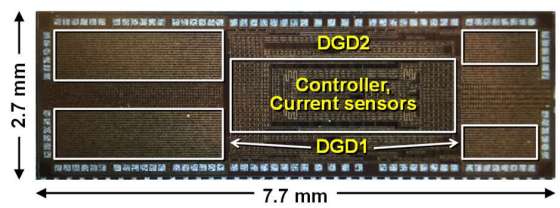

Fig. 8. Die photo of SIDO DGD IC fabricated with 180-nm BCD process.

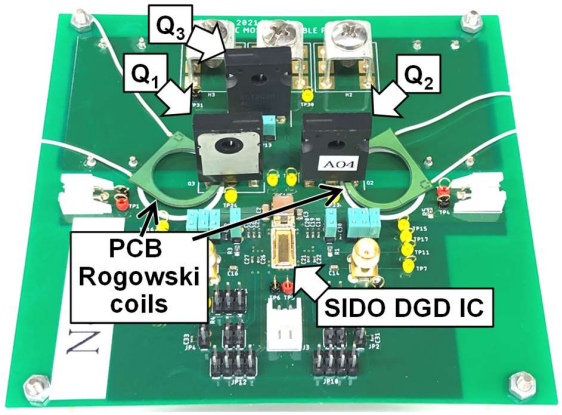

Fig. 9. Photo of PCB of half bridge.

Compared with the conventional gate driving (Fig. 16 (a)), the proposed gate driving (Fig. 16 (c)) with n_{NMOS1} and n_{PMOS2} control reduces the difference between $I_{D1,DC}$ and $I_{D2,DC}$ from 1.3 A to 0.07 A by 95% and the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ from 0.61 A to 0.05 A by 92%.

Finally, the automatic equalization of $I_{D1,DC}$ and $I_{D2,DC}$ by the feedback control of n_{NMOS1} shown in Fig. 5 (b) using SIDO DGD IC is demonstrated. Fig. 17 shows the measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} of the conventional gate driving (Fig. 5 (a)) and DC current equalization by n_{NMOS1} control (Fig. 5 (b)) in multi pulse test at 300 V. In the conventional gate driving in Fig. 17 (a), $V_{GS1} = V_{GS2}$ and $I_{D1,DC} - I_{D2,DC} = 2.3$ A. In contrast, in DC current equalization by n_{NMOS1} control in Fig. 17 (b), V_{GS1} amplitude is automatically regulated to $V_{GS2} - V_{GS1} = 1.8$ V by the feedback control of n_{NMOS1}, achieving $I_{D1,DC} - I_{D2,DC} = 0.24$ A. The automatic equalization of $I_{D1,SURGE}$ and $I_{D2,SURGE}$ by the feedback control of n_{PMOS2} using SIDO DGD IC is a future research topic, because the current sensor in this work cannot accurately measure the high-frequency $I_{D1,SURGE}$ and $I_{D2,SURGE}$ waveforms.

Table I shows a comparison table of DGD ICs. This work is the world's first IC that achieves I_D equalization of two parallel MOSFETs by integrating two DGDs, two current sensors, and a controller.

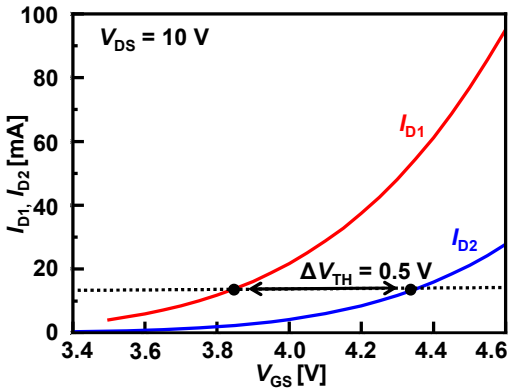

Fig. 10. Measured $I_D - V_{GS}$ characteristics of Q_1 and Q_2 at V_{DS} = 10 V.

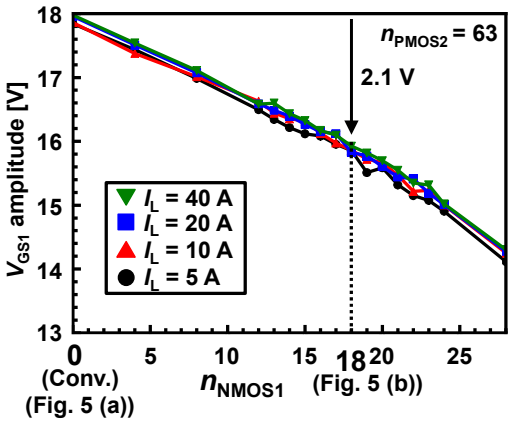

Fig. 11. Measured n_{NMOS1} dependence of V_{GS1} amplitude, corresponding to DC current equalization by n_{NMOS1} control shown in Fig. 5 (b).

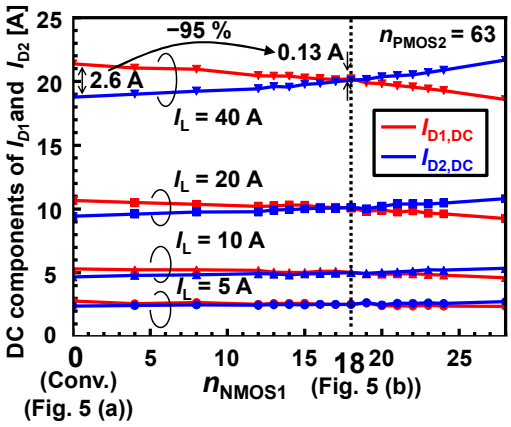

Fig. 12. Measured n_{NMOS1} dependence of $I_{D1,DC}$ and $I_{D2,DC}$, corresponding to DC current equalization by n_{NMOS1} control shown in Fig. 5 (b).

IV. Discussion on Conduction Loss

In order to gain a better understanding of the advantages and disadvantages of the proposed equalization of $I_{D1,DC}$ and $I_{D2,DC}$ using SIDO DGD IC, the conduction losses of Q_1 and Q_2 are discussed. Fig. 18 shows the calculated conduction

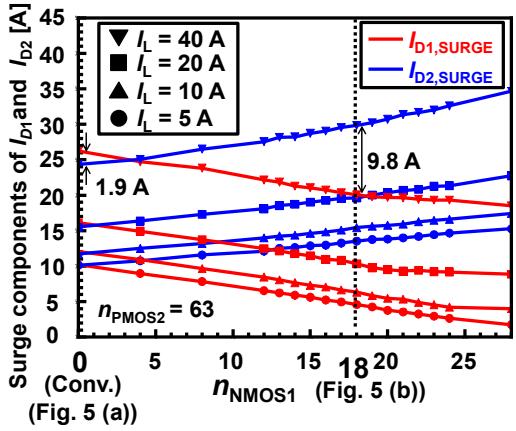

Fig. 13. Measured n_{NMOS1} dependence of $I_{D1,SURGE}$ and $I_{D2,SURGE}$, corresponding to DC current equalization by n_{NMOS1} control shown in Fig. 5 (b).

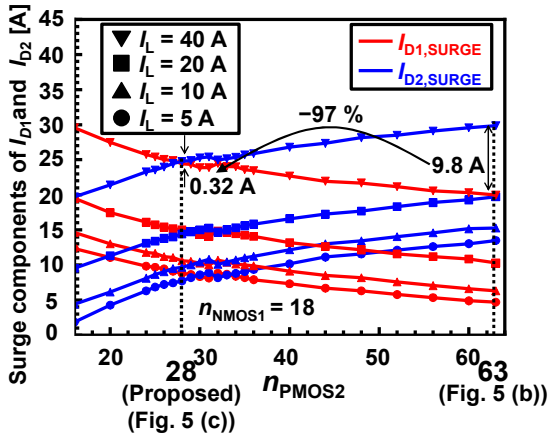

Fig. 14. Measured n_{PMOS2} dependence of $I_{D1,SURGE}$ and $I_{D2,SURGE}$ at n_{NMOS1} = 18, corresponding to proposed DC and surge current equalization by n_{NMOS1} and n_{PMOS2} control shown in Fig. 5 (c).

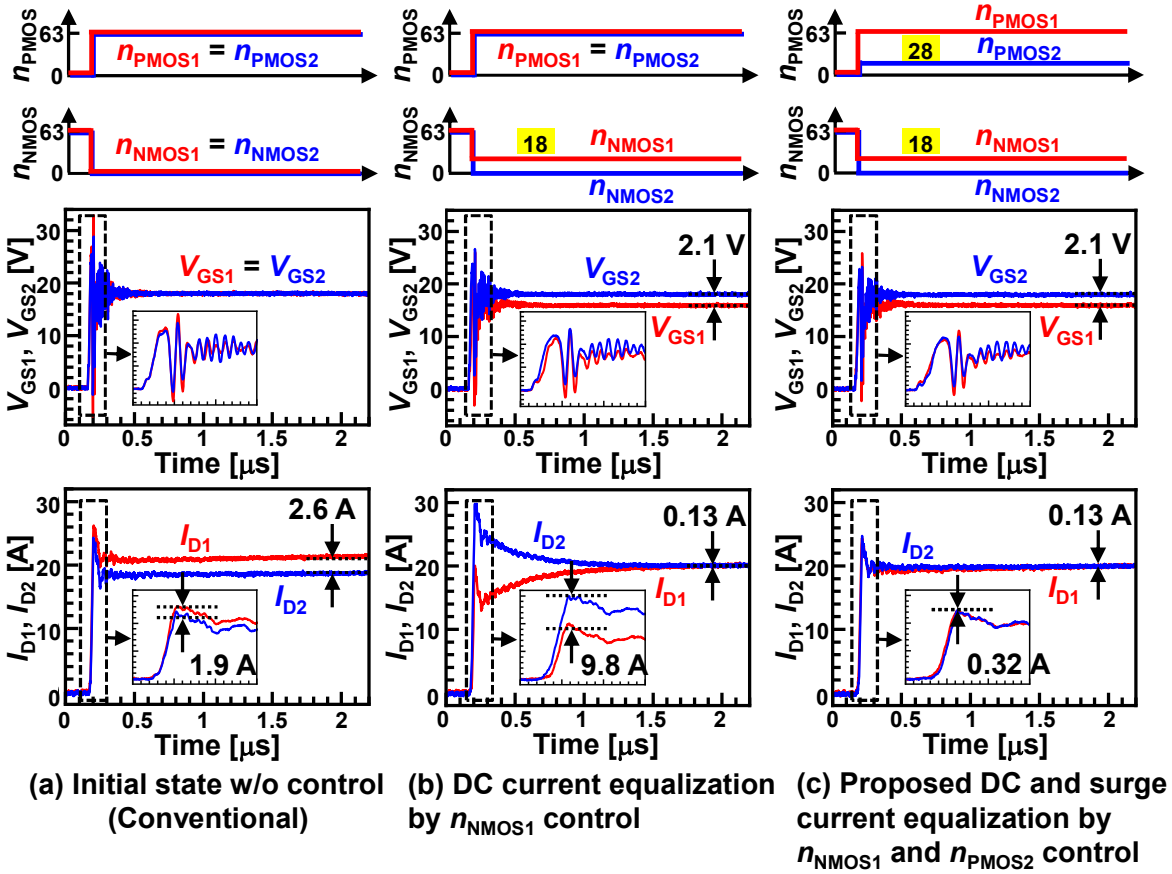

Fig. 15. Measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} corresponding to Figs. 5 and 11 – 14 at I_L = 40 A.

Table I Comparison table of DGD ICs.

	TIA'17 [7]	TPEL'21 [9]	ISPSD'20 [10]	ISPSD'21 [11]	This work
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	SiC MOSFET
Process	180 nm BCD	180 nm HV CMOS	180 nm BCD	180 nm BCD	180 nm BCD
Number of outputs	1	1	1	1	2
Output voltage swing	15 V	5 V	3.3 V	5 V	18 V
Levels of I_G	6 bit	8 bit (coarse), 6 bit (fine)	7 bit	6 bit	6 bit
Max. I_G	5 A	5 V / 0.12 Ω = 42 A	3.3 V / 0.5 Ω = 6.6 A	5 A	6 A
Functions integrated into IC	1 driver	1 driver	1 driver	1 driver	2 drivers, 2 current sensors, controller
Drain current equalization of two parallel MOSFETs	No	No	No	No	Yes

losses of Q_1 and Q_2 in the conventional gate driving (Fig. 15 (a)) and the proposed gate driving (Fig. 15 (c)) at I_L = 40 A. The proposed gate driving reduces the difference between the conduction loss of Q_1 and that of Q_2 from 1.57 W to 0.04 W by 97%, while the proposed gate driving increases the total conduction loss of from 24.1 W to 26.4 W by 9.5%. Therefore, variation of heat generation between Q_1 and Q_2 is reduced, while total heat generation of Q_1 and Q_2 is increased.

The reason can be understood from $I_D - V_{DS}$ characteristics. Fig. 19 shows the measured $I_D - V_{DS}$ characteristics of Q_1 and Q_2 at V_{GS} = 18 V using a curve tracer. To achieve I_L = 40 A, $I_{D1} + I_{D2}$ should be equal to 40 A. In the conventional gate driving (Fig. 15 (a)), V_{DS} = 0.60 V, while V_{DS} = 0.66 V in the proposed gate driving (Fig. 15 (c)) because on-resistance of Q_1 is increased by decreasing V_{GS1} from 18 V to 15.9 V to equalize $I_{D1,DC}$ and $I_{D2,DC}$. The 10% increase of V_{DS} from 0.60 V to 0.66 V agrees well with 9.5% increase of the total conduction loss. If the increase of the total conduction loss is not preferred, V_{GS1} is fixed to 18 V and V_{GS2} should be increased more than 18 V to equalize $I_{D1,DC}$ and $I_{D2,DC}$.

V. Conclusions

In the switching measurements of two parallel SiC MOSFETs at 300 V and 40 A, the proposed SIDO DGD IC reduces the difference between $I_{D1,DC}$ and $I_{D2,DC}$ from 2.6 A to 0.13 A by 95% and the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ from 1.9 A to 0.32 A by 83%. The automatic equalization of $I_{D1,DC}$ and $I_{D2,DC}$ by the feedback control of n_{NMOS1} using SIDO DGD IC is also successfully demonstrated. The proposed SIDO DGD IC will enable a high-performance power electronics systems using SiC MOSFETs at low cost, because SiC MOSFETs with large variations can be connected in parallel without prior testing and selection.

Acknowledgment

This work was partly supported by NEDO (JPNP14004).

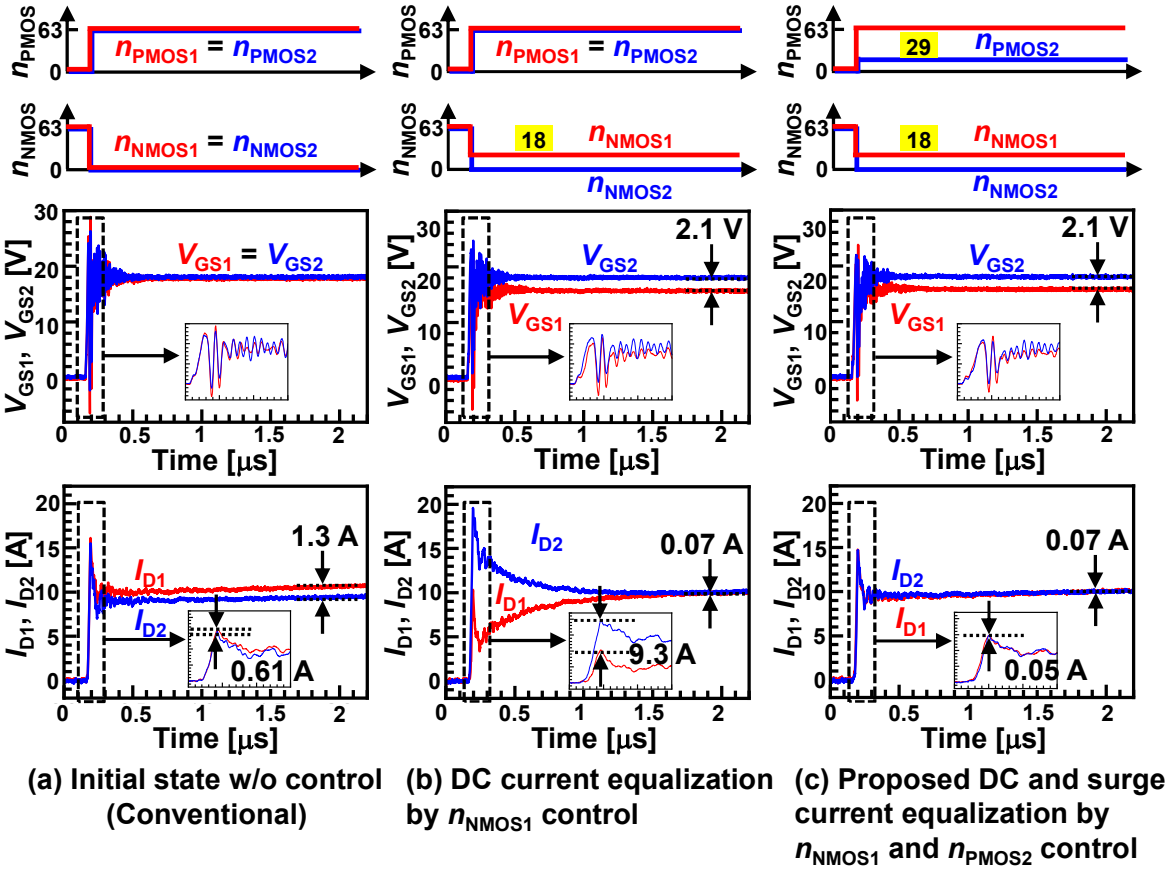

Fig. 16. Measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} corresponding to Figs. 5 and 11 – 14 at I_L = 20 A.

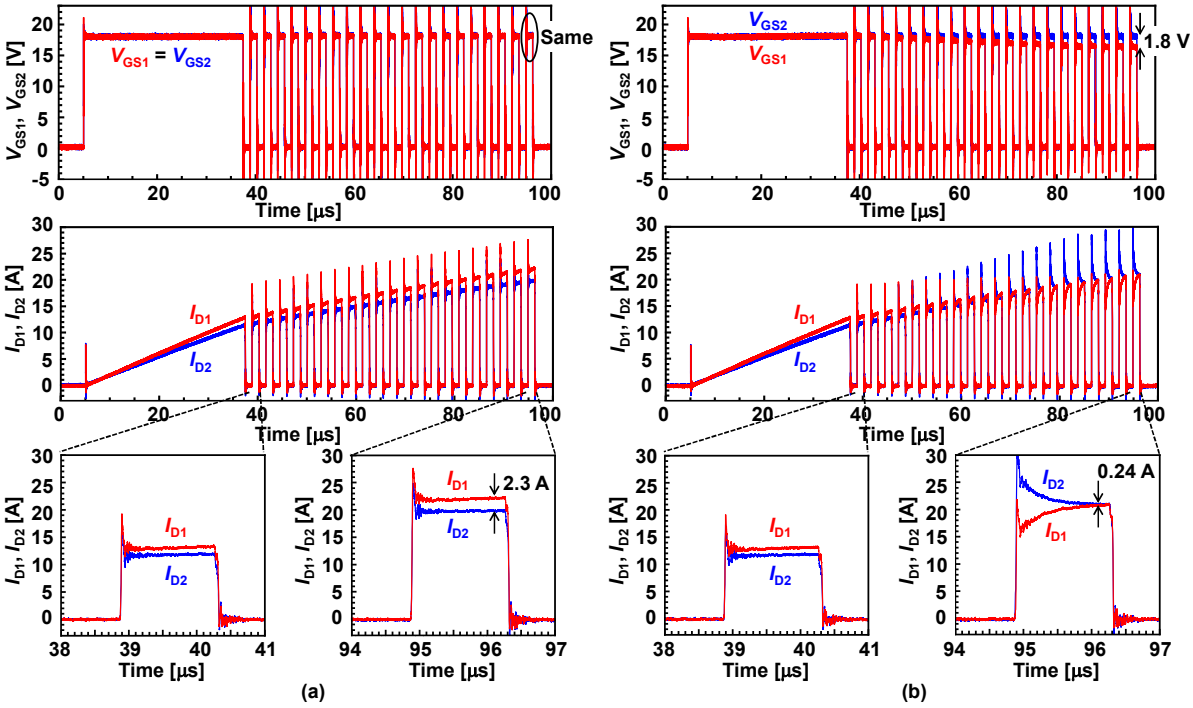

Fig. 17. Measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} in multi pulse test. (a) Conventional gate driving (Fig. 5 (a)). (b) DC current equalization by n_{NMOS1} control (Fig. 5 (b)).

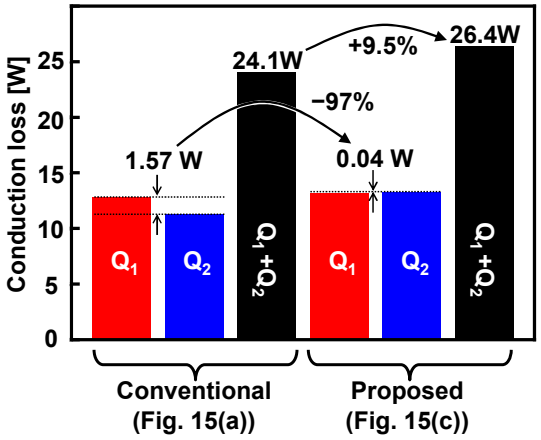

Fig. 18. Calculated conduction losses of Q_1 and Q_2 in conventional gate driving (Fig. 15 (a)) and proposed gate driving (Fig. 15 (c)) at $I_L = 40$ A.

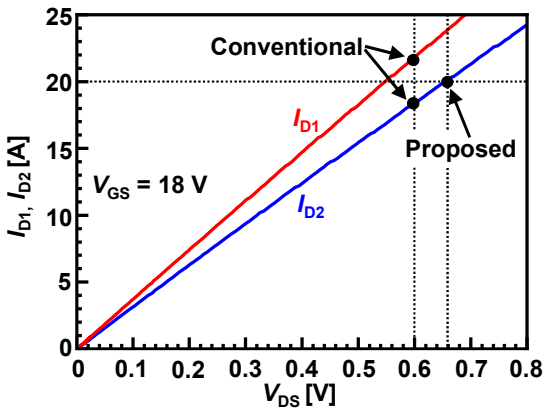

Fig. 19. Measured $I_D - V_{DS}$ characteristics of Q_1 and Q_2 at $V_{GS} = 18$ V.

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