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Large Current Output Digital Gate Driver Using Half-Bridge Digital-to-Analog Converter IC and Two Power MOSFETs

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***Abstract*—An 8-bit digital gate driver (DGD) using a half-bridge digital-to-analog converter (HB DAC) IC and two power MOSFETs is proposed to enable the output voltage swing of ± 15 V and the large gate current up to 58 A for a 6500 V, 1000 A IGBT module. In the turn-on measurements of IGBT at 3000 V and 1000 A, compared with the conventional single-step gate driving, the proposed active gate driving using DGD reduces the switching loss from 6.9 J to 4.8 J by 30 % at the same current overshoot of 1.3 kA and reduces the current overshoot from 1560 A to 1330 A by 15 % at the same switching loss of 5 J, which clearly shows the advantage of DGD for the 6500 V, 1000 A IGBT module. This paper is the first to demonstrate the advantages of DGD in the high-voltage, large-current IGBT modules.**

Keywords—gate driver, IGBT, switching loss, high voltage

I. Introduction

High-voltage, large-current IGBT modules (e.g. ratings of 6500 V, 1000 A) are used in many social infrastructure fields including high-voltage DC transmission systems and train traction systems [1]. In addition to improving IGBTs themselves, gate driving technologies can be used to reduce the loss of IGBTs. Recently, many papers have been published on the simultaneous reduction of both switching loss (E_{LOSS}) and switching noise by active gate waveform control using digital gate drivers (DGDs) [2-8]. Conventional DGDs, however, are difficult to apply to the 6500 V, 1000 A IGBT modules, because the modules require DGD with (1) the output voltage swing (V_{SWING}) of ± 15 V to prevent a false turn-on and (2) the gate current (I_G) of up to around 20 A because of the large gate capacitance. For example, V_{SWING} is 3.3 V [3], 5 V [4–5, 7], 15 V [2], 18 V [6] and 20 V [8], and the maximum I_G is between 5 A [2, 4] and 42 A [5].

To solve the problems, in this paper, an 8-bit DGD using a half-bridge digital-to-analog converter (HB DAC) IC and two power MOSFETs is proposed to enable V_{SWING} of ± 15 V and large I_G up to 58 A for the 6500 V, 1000 A IGBT modules. 30 % reduction of E_{LOSS} and 15 % reduction of the current overshoot ($I_{OVERSHOOT}$) compared with the conventional single-step gate driving in the turn-on of the 6500 V, 1000 A IGBT module at 3000 V and 1000 A are experimentally shown. This paper is the first to demonstrate the advantages of DGD in the high-voltage, large-current IGBT modules.

II. Design of Digital Gate Driver Using HB DAC IC and Two Power MOSFETs

Figs. 1 to 3 show a circuit schematic of the proposed DGD including HB DAC IC and two power MOSFETs (Q_1 and Q_2 : BSC094N06LS5, 60 V, 47 A), a block diagram of the proposed HB DAC IC, and a timing chart of DGD, respectively. DGD is a current-source gate driver. The novelty of this work is that power MOSFETs are used as the output stage of the gate driver to achieve large I_G, and DGD operation is achieved by digitally controlling the gate amplitude (V_{GSH} and V_{GSL}) of the power MOSFETs operating in the saturation region instead of the linear region using the proposed HB DAC IC to achieve the current-source gate driver. As shown in Fig. 2, HB DAC IC includes two DACs operating with different power supply rails, shift registers for serial inputs to reduce the number of input pins, and an edge detector to generate pulse signals from externally supplied "Timing" signal. HB DAC IC does not include the driver transistors. If all the functions are integrated into a single IC, the chip size will be huge and the cost will be high. By controlling the gate voltage of Q_1 (V_{GSH}) with a 16-bit input DAC (Fig. 2), I_G can be digitally varied four times at turn-on (Fig. 3). The four periods from t_1 to t_4 are determined by "Timing" signal, and t_1 to t_4 can be changed independently. The same is true for turn-off.

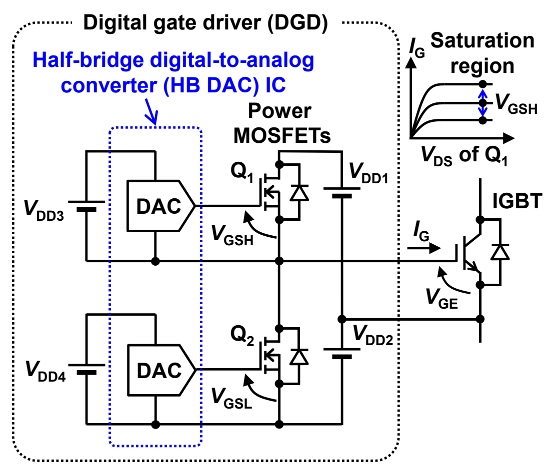

Fig. 1. Circuit schematic of proposed digital gate driver (DGD) including HB DAC IC and two power MOSFETs.

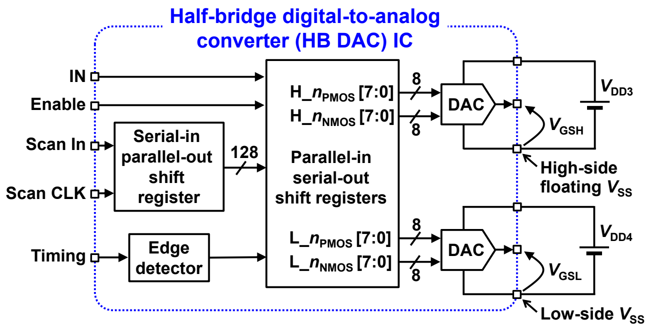

Fig. 2. Block diagram of proposed half-bridge digital-to-analog converter (HB DAC) IC.

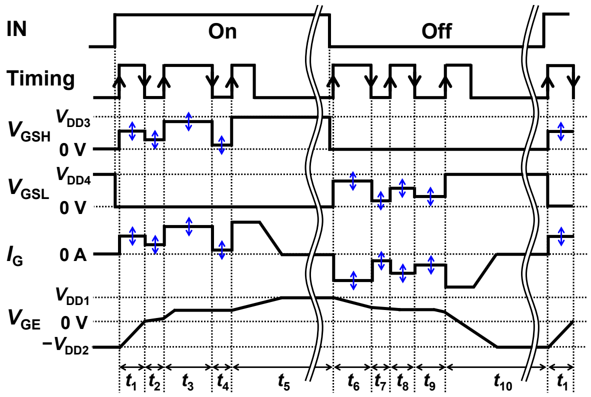

Fig. 3. Timing chart of DGD.

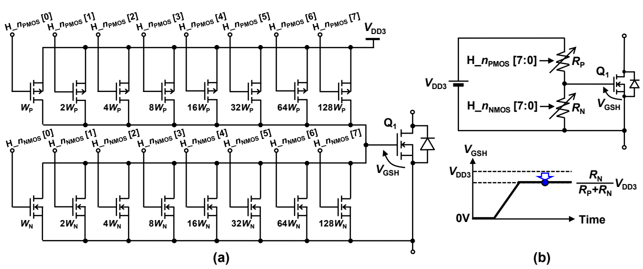

Fig. 4. 16-bit input DAC for Q_1. (a) Circuit schematic. (b) Equivalent circuit.

Figs. 4 (a) and (b) show a circuit schematic and an equivalent circuit of the 16-bit input DAC for Q_1, respectively. This DAC has a similar circuit configuration to DGD with binary weighted gate widths (W_P, $2W_P$, $4W_P$, $8W_P$, $16W_P$, $32W_P$, $64W_P$, $128W_P$) in the output stage [4], however, the method of operation is different. V_{GSH} can be digitally controlled by H_n_{PMOS} [7:0] and H_n_{NMOS} [7:0] on the principle of a shunt regulator, where some of the eight pMOSFETs and some of the eight nMOSFETs in Fig. 4 (a) are turned on. This DAC has 16-bit inputs, however, for simplicity, 8-bit digital signals H_n_{NMOS} [7:0] are fixed and 8-bit digital signals H_n_{PMOS} [7:0] are varied in this paper. V_{GSH} can be varied in 256 levels depending on H_n_{PMOS} [7:0], which is defined as H_n_{PMOS}, where H_n_{PMOS} is an integer between 0 and 255. Similarly, H_n_{NMOS} is an integer between 0 and 255.

Fig. 5 shows a die micrograph of HB DAC IC fabricated with 180-nm BCD process. The die size is 2.5 mm by 1.0 mm. Fig. 6 shows a photo of PCB of DGD. HB DAC IC is mounted on the surface of the PCB, and Q_1 and Q_2 are mounted on the back of the PCB.

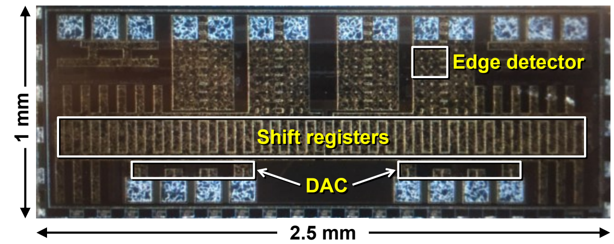

Fig. 5. Die micrograph of HB DAC IC.

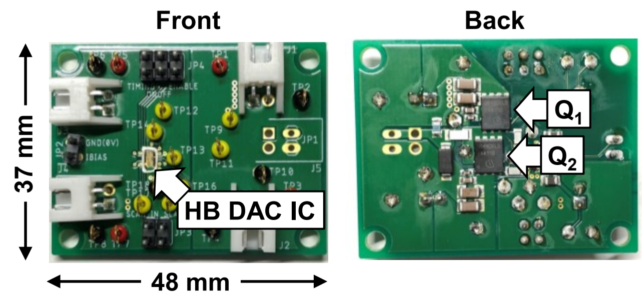

Fig. 6. Photo of PCB of DGD.

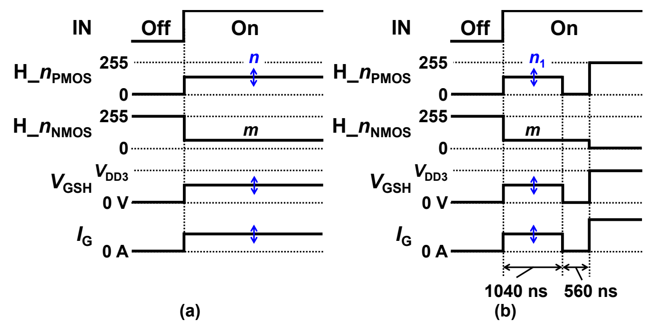

Fig. 7. Timing charts for turn-on measurement. (a) Conventional single-step gate driving (SGD). (b) Proposed active gate driving (AGD).

III. Measured Results

In this paper, only $I_{OVERSHOOT}$ at turn-on discussed and the collector-emitter voltage (V_{CE}) overshoot at turn-off is not discussed, because $I_{OVERSHOOT}$ is large, while the voltage overshoot is small, being less than 500 V.

Figs. 7 (a) and (b) show timing charts for the turn-on measurement of the conventional single-step gate driving (SGD) and the proposed active gate driving (AGD), respectively. AGD is based on the stop-and-go gate driving [9]. In AGD, only two periods (t_1 and t_2) out of four periods (t_1 to t_4) in Fig. 3 are used for simplicity. n is varied in SGD and n_1 is varied in AGD, where n and n_1 are integers between 0 and 255. m is common to SGD and AGD, where m is 60 or 100 in this paper.

Fig. 8 shows the measured n dependence V_{GSH} in SGD to demonstrate the successful operation of 8-bit DAC at V_{DD3} = V_{DD4} = 3.5 V and 4 V and m = 60 and 100. V_{GSH} is monotonically increasing with n, although DAC is nonlinear. The maximum output current of DAC is 100 mA. Fig. 9 shows the measured n dependence I_G in SGD to demonstrate the successful operation of 8-bit DGD at V_{DD3} = V_{DD4} = 3.5 V and 4 V and m = 60 and 100. To investigate the performance of DGD itself, a 100 μF capacitor is connected to the output of DGD and I_G is measured.

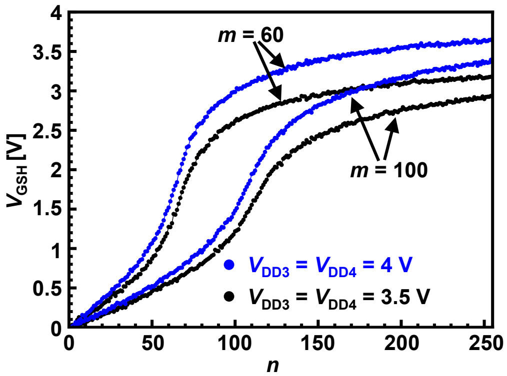

Fig. 8. Measured n dependence V_{GSH} in SGD to demonstrate operation of 8-bit DAC.

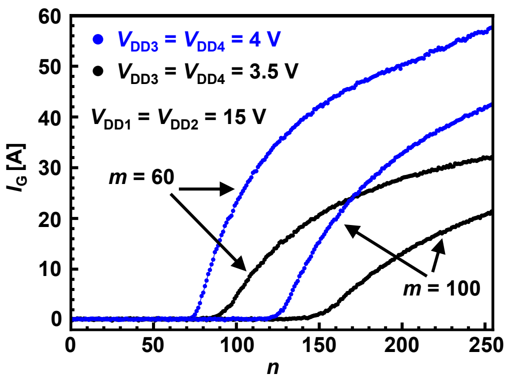

Fig. 9. Measured n dependence I_G in SGD to demonstrate operation of 8-bit DGD.

I_G is monotonically increasing with n, although it is nonlinear. The maximum I_G is 58 A.

Figs. 10 and 11 show a circuit schematic and a measurement setup of the double pulse test using DGD and two IGBT modules (Q_3 and Q_4 : CM1000HG-130XA, 6500 V, 1000 A) at 3000 V and 1000 A, respectively. Fig. 12 shows the measured E_{LOSS} vs. $I_{OVERSHOOT}$ at $V_{DD3} = V_{DD4} = 3.5$ V and $m = 100$. The black line shows the trade-off curve of the conventional SGD (Fig. 7 (a)) with varied n from 175 to 255. The red star shows the proposed AGD (Fig. 7 (b)) at $n_1 = 223$. Compared with SGD, the proposed AGD reduces E_{LOSS} from 6.9 J to 4.8 J by 30 % at the same $I_{OVERSHOOT}$ of 1.3 kA and reduces $I_{OVERSHOOT}$ from 1560 A to 1330 A by 15 % at the same E_{LOSS} of 5 J, which clearly shows the advantage of DGD for the 6500 V, 1000 A IGBT module.

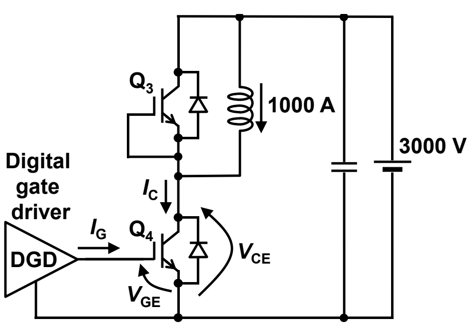

Fig. 10. Circuit schematic of double pulse test.

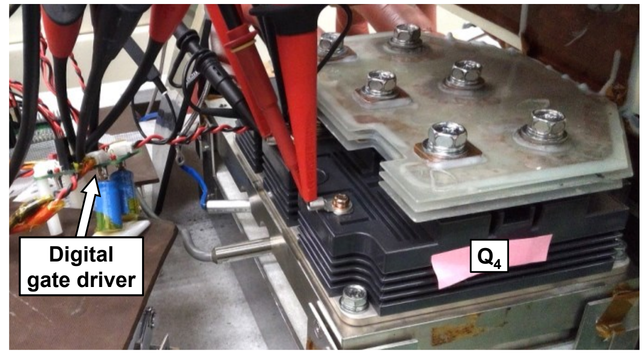

Fig. 11. Measurement setup of double pulse test.

Fig. 13 shows corresponding measured waveforms in Fig. 12. Fig. 13 (a) shows the measured waveforms of SGD at $n = 175$ with the smallest I_G, achieving the smallest $I_{OVERSHOOT}$ and the largest E_{LOSS}. In contrast, Fig. 13 (b) shows the measured waveforms of SGD at $n = 255$ with the largest I_G, achieving the smallest E_{LOSS} and the largest $I_{OVERSHOOT}$. The maximum measured I_G is 14 A. Fig. 13 (d) shows the measured waveforms of the proposed AGD. Figs. 13 (c) and (e) show the measured waveforms of SGD with the same $I_{OVERSHOOT}$ and E_{LOSS} as AGD, respectively. In Fig. 13 (d), AGD achieves low E_{LOSS} and $I_{OVERSHOOT}$ by setting I_G to zero just before the timing of $I_{OVERSHOOT}$. In Fig. 13 (d), the maximum measured I_G is 10 A.

Table I shows a comparison table of DGDs. The proposed DGD using HB DAC IC and two power MOSFETs achieves the largest V_{SWING} of 30 V and the largest I_G of 58 A in DGDs. This paper is the first to demonstrate the advantages of DGD in the high-voltage, large-current IGBT modules.

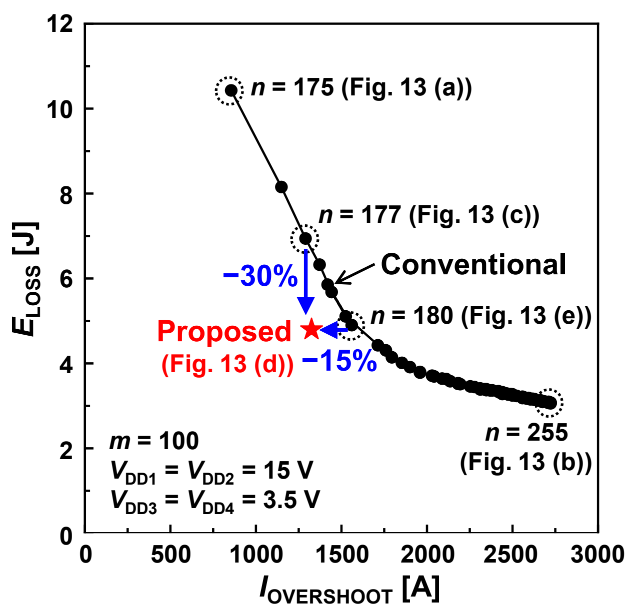

Fig. 12. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SGD and proposed AGD.

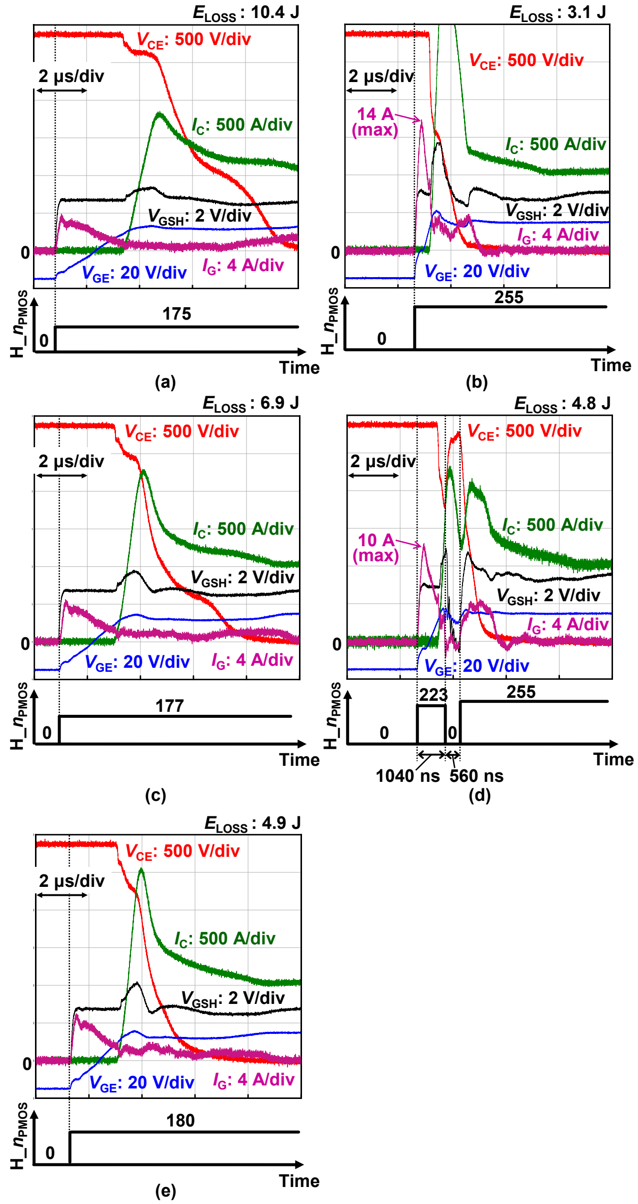

Fig. 13. Measured waveforms in Fig. 12. (a) Conventional SGD at n = 175. (b) Conventional SGD at n = 255. (c) Conventional SGD at n = 177. (d) Proposed AGD. (e) Conventional SGD at n = 180.

Table I. Comparison table of DGDs.

	TIA'17 [2]	ISPSD'20 [3]	ISPSD'21 [4]	TPEL'21 [5]	This work
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	Si IGBT
Process	180 nm BCD	180 nm BCD	180 nm BCD	180 nm HV CMOS	180 nm BCD
Chip area	6.25 mm²	1.97 mm²	4.32 mm²	5.0 mm²	2.5 mm²
Output voltage swing	15 V	3.3 V	5 V	5 V	30 V
Levels of I_G	6 bit	7 bit	6 bit	8 bit (coarse), 6 bit (fine)	8 bit
Max. I_G	5 A	3.3 V / 0.5 Ω = 6.6 A	5 A	5 V / 0.12 Ω = 42 A	58 A
Functions integrated into IC	1 driver	1 driver	1 driver	1 driver	2 DACs

IV. Conclusions

8-bit DGD using HB DAC IC and two power MOSFETs is proposed to enable V_{SWING} of ± 15 V and large I_G up to 58 A for the 6500 V, 1000 A IGBT modules. In the turn-on measurements of IGBT at 3000 V and 1000 A, compared with SGD, the proposed AGD reduces E_{LOSS} from 6.9 J to 4.8 J by 30 % at the same $I_{OVERSHOOT}$ of 1.3 kA and reduces $I_{OVERSHOOT}$ from 1560 A to 1330 A by 15 % at the same E_{LOSS} of 5 J, which clearly shows the advantage of DGD for the 6500 V, 1000 A IGBT module.

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