Sub-0.5 ns Step, 10-bit Time Domain Digital Gate Driver IC for Reducing Radiated EMI and Switching Loss of SiC MOSFETs

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***Abstract*— A sub-0.5 ns step, 10-bit time domain digital gate driver (TD DGD) IC is proposed for SiC MOSFETs to reduce both the radiated EMI and the switching loss (E_{LOSS}). Unlike the conventional current-domain DGDs, the proposed TD DGD has the advantage that the gate current is binary and only one period is digitally changed, making it easy to search for the optimal gate waveform that reduces both EMI and E_{LOSS}. Using TD DGD IC fabricated with 180-nm BCD process, the radiated EMI spectrums from 30 MHz to 100 MHz and E_{LOSS} are measured in the double pulse test of a full SiC module at 600 V and 300 A. The proposed active gate drive using TD DGD IC reduces E_{LOSS} by 50 % and 39 % compared with the conventional single-step gate drive while satisfying an EMI limit in turn-on and turn-off, respectively.**

Keywords—EMI, switching loss, gate driver, time domain

I. Introduction

Fast switching of SiC MOSFETs reduces the switching loss (E_{LOSS}), while the radiated EMI increases. Active gate driver [1–2] and digital gate driver (DGD) [3–8], which digitally controls the gate driving current of power devices during turn-on/off transients, are promising technologies to overcome the trade-off between EMI and E_{LOSS}. Addressing the radiated EMI using conventional DGDs, however, has problems.

Two methods of implementing DGD can be considered, a current-domain (CD) DGD and a time domain (TD) DGD. Fig. 1 (a) shows CD DGD, where the time step (Δt) is fixed and the gate current (I_{G}) is digitally n-bit controlled. All conventional DGDs [3–8] are CD DGDs. Fig. 1 (b) shows TD DGD, where I_{G} is binary and each time step is digitally n-bit controlled. Since the radiated EMI is generated at the moment when the SiC MOSFET switches, in order to control the radiated EMI using DGD, it is necessary to change I_{G} using DGD precisely targeting the moment of the switching. When the frequency range of the radiated EMI is from 30 MHz to 1 GHz, the range of time steps required for DGD is from 0.5 ns (= 1 / 1 GHz / 2) to 17 ns (= 1 / 30 MHz / 2). In the conventional CD DGDs, however, when Δt is reduced below 17 ns to control the radiated EMI, the number of steps (m) increases and the number of DGD parameter combinations explodes to $(2^n)^m$ as shown in Fig. 1 (a). For example, in DGD with n = 14 and m = 104 developed for

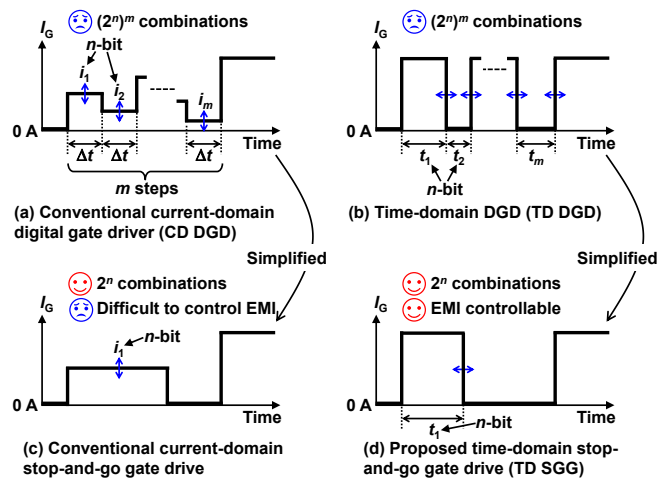

Fig. 1. Gate current (I_{G}) waveforms in digital gate drivers.

the radiated EMI in GaN [8], it is extremely difficult to find the optimal DGD parameters, because the number of DGD parameter combinations is $(2^{14})^{104}$. Therefore, in order to control the radiated EMI with reducing the number of DGD parameter combinations, TD DGD is better than CD DGD to change I_{G} precisely targeting the moment of the switching.

In addition, in order to reduce the number of DGD parameter combinations from $(2^n)^m$ to 2^n, a current-domain stop-and-go gate drive shown in Fig. 1 (c) is reported in [9, 10], while this is not suitable for the radiated EMI control, because the timing control is not possible. To solve the problems, a time-domain stop-and-go gate drive (TD SGG) shown in Fig. 1 (d) is proposed in this paper. By digitally controlling only t_1 in 10-bit, sub-0.5 ns steps, the proposed TD SGG reduces E_{LOSS} by 50 % and 39 % compared with the conventional single-step gate drive (SSG) while satisfying an EMI limit in turn-on and turn-off, respectively.

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II. Time Domain Digital Gate Driver (TD DGD) IC

Figs. 2 and 3 show a circuit schematic and a timing chart of the proposed TD DGD IC, respectively. The output voltage swing is 30 V to achieve V_{GS} from − 15 V to 15 V for SiC MOSFETs. In order to realize both the conventional SSG and the proposed TD SGG, which will be explained later in Figs. 8 and 9, using the same gate driver IC and compare them, both CD DGD and TD DGD functions are included in the developed TD DGD IC. TD DGD IC has a total of 26 control bits including T_1 [9:0], T_2 [3:0], I_1 [5:0], and I_2 [5:0]. By using the digitally controlled delay line (DCDL) in TD DGD IC, time of the first step (t_1) can be changed from 0 s to 470 ns in 10-bit, 459-ps steps using T_1 [9:0], and time of the second step (t_2) can be changed from 0 s to 90 ns in 4-bit, 6-ns steps using T_2 [3:0]. The circuit schematic of the 6-bit output stage in Fig. 2 is designed with reference to [7]. I_G can be digitally changed from 0 A to 22 A in 6-bit steps of 350 mA depending on I_1 [5:0] and I_2 [5:0]. n_{PMOS} is an integer from 0 to 63 indicating I_G at turn-on and $I_G = n_{PMOS} \times 350$ mA. Similarly, n_{NMOS} is an integer from 0 to 63 indicating I_G at turn-off.

Fig. 4 shows a die micrograph of TD DGD IC fabricated with 180-nm BCD process. The die size is 4.5 mm by 3.1 mm.

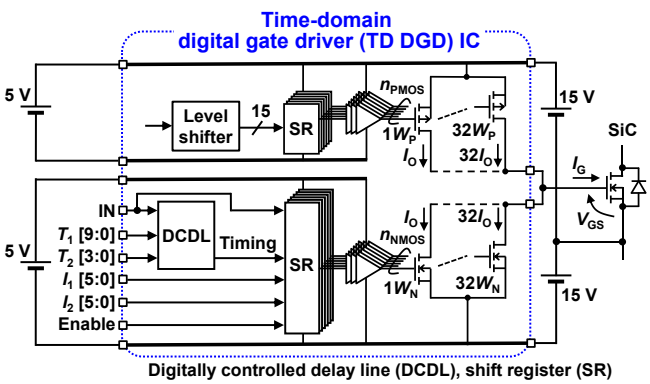


Fig. 2. Circuit schematic of proposed time domain digital gate driver (TD DGD) IC.

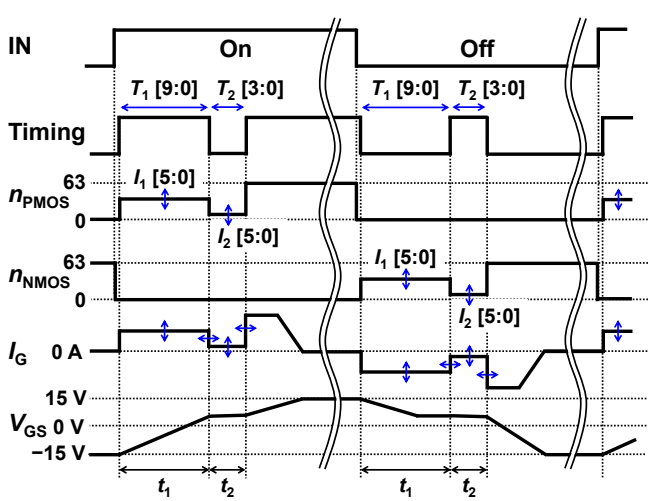


Fig. 3. Timing chart of proposed TD DGD IC.

Fig. 5 shows the measured t_1 vs. T_1 [9:0] to verify the time step and the linearity of DCDL. The 10-bit digital control of t_1 in sub-0.5 ns step from 0 s to 470 ns is successfully demonstrated. The measured time step is 459 ps (= 470 ns / 1023).

III. Measured Radiated EMI and Switching Loss of SiC MOSFETs

A. Measurement Setup

In order to show the advantage of the proposed TD SGG using TD DGD IC, the radiated EMI and E_{LOSS} are measured and compared with the conventional SSG. Figs. 6 and 7 show a circuit schematic and a measurement setup of the double pulse test using the developed TD DGD IC and a full SiC module (FMF400BX-24A, 1200 V, 400 A) at 25 °C, 600 V, and 300 A, respectively. In order to measure the radiated EMI, a magnetic field probe (RS H400–1, HZ–15, Rohde & Schwarz) is fixed just above the switching terminal of the SiC module and the probe output voltage (V_{EMI}) waveform at turn-on and turn-off is measured with a 1.25-GSa/s oscilloscope and Fourier transformed. Figs. 8 (a) and (b) show timing charts for the turn-

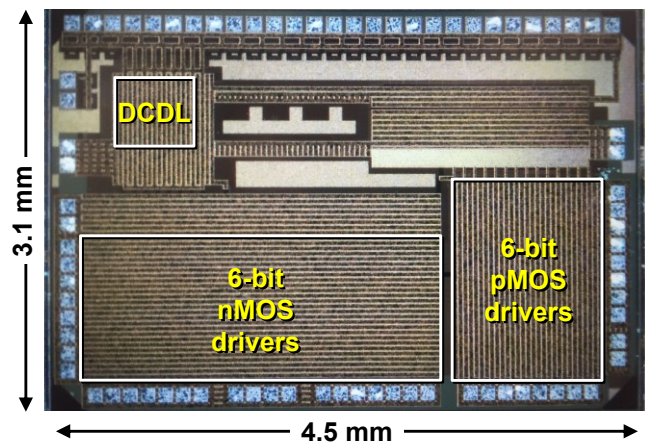


Fig. 4. Die micrograph of TD DGD IC fabricated with 180-nm BCD process.

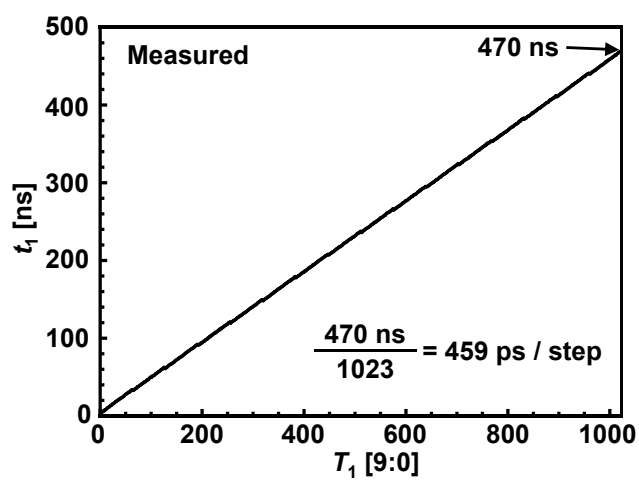


Fig. 5. Measured t_1 vs. T_1 [9:0] of digitally controlled delay line (DCDL) in TD DGD IC.

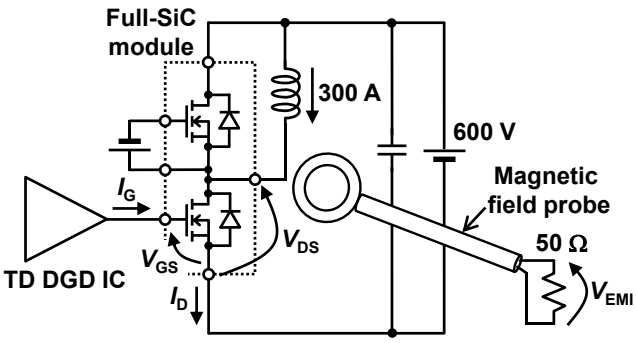


Fig. 6. Circuit schematic of double pulse test to measure radiated EMI.

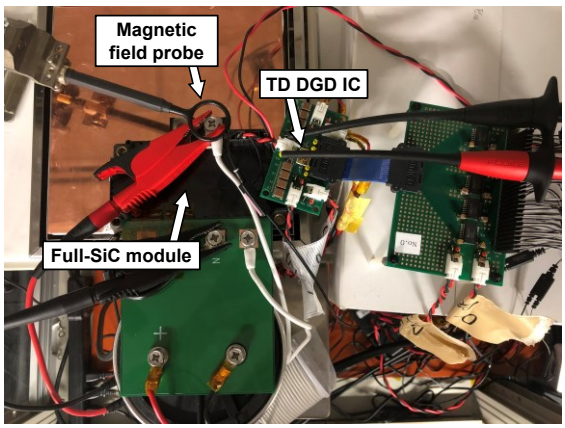


Fig. 7. Measurement setup using TD DGD IC and full SiC module to measure radiated EMI.

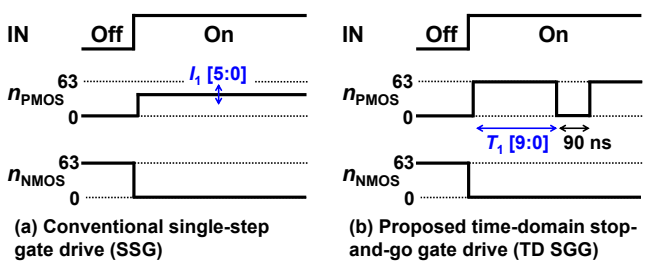


Fig. 8. Timing charts for turn-on measurements.

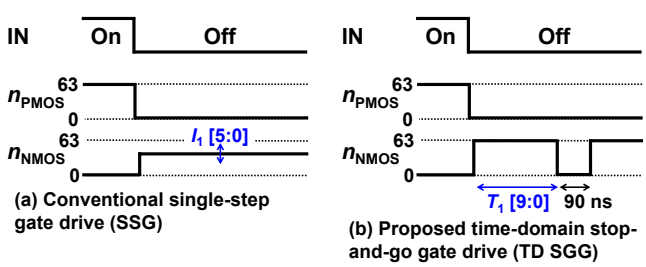


Fig. 9. Timing charts for turn-off measurements.

on measurement of the conventional SSG and the proposed TD SGG, respectively. Figs. 9 (a) and (b) show timing charts for the turn-off measurement of the conventional SSG and the proposed TD SGG, respectively. In SSG, I_1 [5:0] is varied, which emulates a conventional gate driver with varied gate resistance. In TD SGG, T_1 [9:0] is varied under the conditions of T_2 [3:0] = 15, corresponding to t_2 = 90 ns (= 6 ns × 15), I_1 [5:0] = 63, and I_2 [5:0] = 0.

B. Definition of EMI Evaluation Indicator

In order to quantitatively evaluate EMI, an excessive spectrum area (A_{EXCESS}), where the EMI spectrum exceeds an EMI limit, is defined as Eq. (1) [6].

$$A_{\mathrm{EXCESS}} = \int_{30\ \mathrm{MHz}}^{100\ \mathrm{MHz}} \left\{ \frac{\max(VA_{\mathrm{MEASURE}}, VA_{\mathrm{LIMIT}}) - VA_{\mathrm{LIMIT}}}{VA_{\mathrm{LIMIT}}} \right\} df \times 10^{-6} \quad (1)$$

where VA_{MEASURE} and VA_{LIMIT} are the measured relative voltage amplitude of V_{EMI} and the voltage amplitude of the EMI limit in units of dB, respectively, and f is the frequency. Since measurements of the radiated EMI are made using a magnetic field probe rather than a standard antenna, this paper discusses relative instead of absolute values of the radiated EMI. In this paper, A_{EXCESS} is defined in the range of 30 MHz to 100 MHz, because the developed TD DGD IC is effective for the radiated EMI from 30 MHz to 100 MHz. A_{EXCESS} of zero means that the measured EMI spectrum satisfies the EMI limit. In this paper, two types of VA_{LIMIT}'s are defined: "Limit 1" is VA_{LIMIT} = − 15 dB and "Limit 2" is VA_{LIMIT} = − 5 dB.

C. Turn-On Measurements

In this section, the measured radiated EMI and E_{LOSS} at turn-on are shown. Figs. 10 (a) and (b) show the measured E_{LOSS} vs. A_{EXCESS} in turn-on at Limit 1 and Limit 2, respectively. The conventional SSG and the proposed TD SGG are compared. In Fig. 10 (a), when I_1 [5:0] is increased from 8 to 63 in the conventional SSG, A_{EXCESS} is increased and E_{LOSS} is reduced, which clearly shows the trade-off relationship between EMI and E_{LOSS}. In Fig. 10 (a), when T_1 [9:0] is increased from 100 to 400 in the proposed TD SGG, the measurement results circled counterclockwise from the bottom right point and return to the bottom right point. In Fig. 10 (a), none of the measurement points achieved A_{EXCESS} = 0, while many measurement points achieved A_{EXCESS} = 0 in Fig. 10 (b), because Limit 1 is lower than Limit 2. Please note that optimization of t_1 with 459-ps step is very important because, depending on the value of T_1 [9:0], there are both cases where the proposed TD SGG has lower E_{LOSS} and A_{EXCESS} than the conventional SSG and cases where TD SGG has higher E_{LOSS} and A_{EXCESS} than SSG [10]. In this paper, the best gate drive is defined as the one that satisfies Limit 2 (A_{EXCESS} = 0) and has the lowest E_{LOSS} in Fig. 10 (b). In the following, three points including Point A, Point B, and Point C in Fig. 10 (b) will be focused on and are compared. Point A is the best gate drive in the conventional SSG with I_1 [5:0] = 27, Point B is the best gate drive in the proposed TD SGG with T_1 [9:0] = 367, corresponding to t_1 = 168 ns (= 459 ps × 367), and Point C is the highest drivability in the conventional SSG with I_1 [5:0] = 63. Compared with Point A, the proposed Point B reduces E_{LOSS} from 2.6 mJ to 1.3 mJ by 50 % at A_{EXCESS} = 0.

Fig. 11 shows the measured radiated EMI spectrums of Point A to Point C at turn-on. Point A and the proposed Point B satisfy Limit 2, while Point C violates Limit 2. Figs. 12 (a) to (c) show

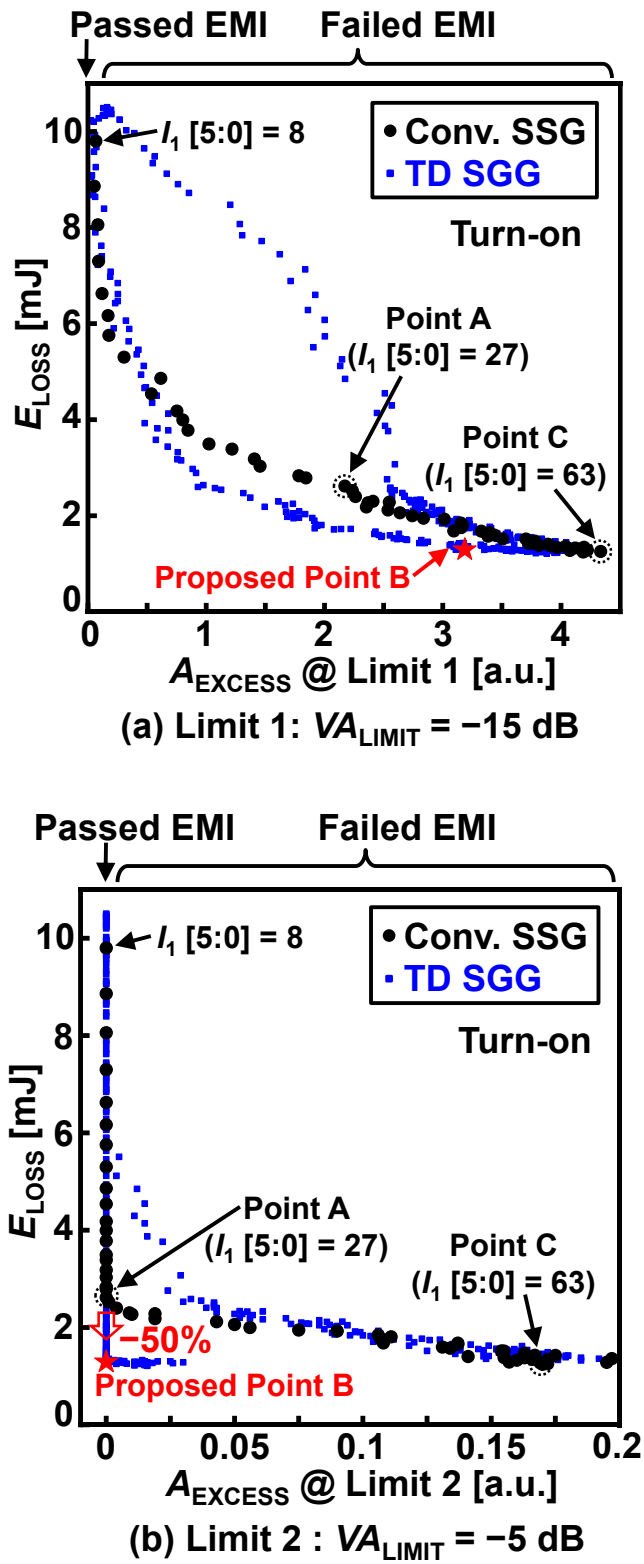


Fig. 10. Measured E_{LOSS} vs. A_{EXCESS} in turn-on at Limit 1 and Limit 2. The conventional SSG and the proposed TD SGG are compared.

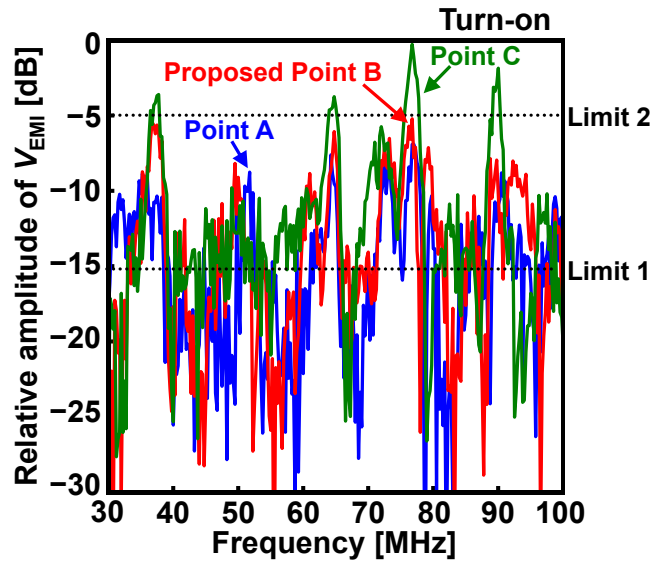


Fig. 11. Measured radiated EMI spectrums of Point A to Point C at turn-on.

the measured waveforms of V_{GS}, V_{DS}, I_D, and V_{EMI} and the timing chart of n_{PMOS} at turn-on in Point A, Point B, and Point C, respectively. First, Point A and Point B are compared. Looking at the waveforms of V_{DS} and I_D in Figs. 12 (a) and (b), it is clear that E_{LOSS} of Point B is smaller than that of Point A. Next, Point B and Point C are compared. The large ringing of V_{EMI} in Fig. 12 (c) is the cause of large EMI of Point C in Fig. 11. In Fig. 12 (b), a temporary drop in V_{GS} waveform caused by the proposed TD SGG can be clearly seen. In Point B, the temporary drop in V_{GS} waveform reduces the ringing of V_{EMI} in Fig. 12 (b), thereby reducing EMI in Fig. 11.

D. Turn-Off Measurements

In this section, the measured radiated EMI and E_{LOSS} at turn-off are shown. Almost similar results are obtained for turn-on and turn-off. Figs. 13 (a) and (b) show the measured E_{LOSS} vs. A_{EXCESS} in turn-off at Limit 1 and Limit 2, respectively. The conventional SSG and the proposed TD SGG are compared. In Fig. 13 (a), when I_1 [5:0] is increased from 8 to 63 in the conventional SSG, A_{EXCESS} is increased and E_{LOSS} is reduced, which clearly shows the trade-off relationship between EMI and E_{LOSS}. In Fig. 13 (a), when T_1 [9:0] is increased from 100 to 400 in the proposed TD SGG, the measurement results circled counterclockwise from the bottom right point and return to the bottom right point. In Fig. 13 (a), none of the measurement points achieved A_{EXCESS} = 0, while many measurement points achieved A_{EXCESS} = 0 in Fig. 13 (b), because Limit 1 is lower than Limit 2. In this paper, the best gate drive is defined as the one that satisfies Limit 2 (A_{EXCESS} = 0) and has the lowest E_{LOSS} in Fig. 13 (b). In the following, four points including Point D to Point G in Fig. 13 (b) will be focused on and are compared. Point D is the best gate drive in the conventional SSG with I_1 [5:0] = 11, Point E is the best gate drive in the proposed TD SGG with T_1 [9:0] = 273, corresponding to t_1 = 125 ns (= 459 ps × 273), and Point F is the highest drivability in the conventional SSG with I_1 [5:0] = 63. Point G is the worst gate drive in the proposed TD SGG with T_1 [9:0] = 222, corresponding to t_1 = 102 ns (=

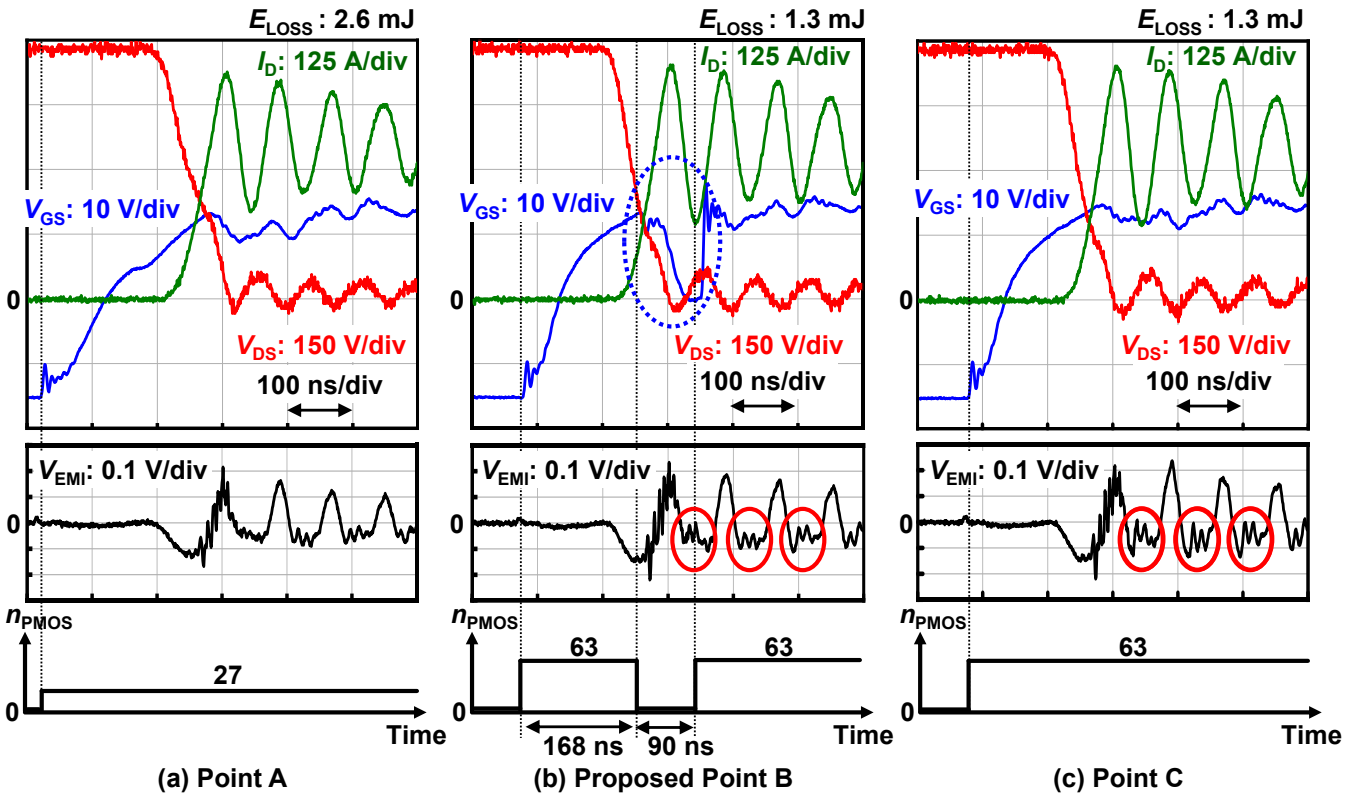


Fig. 12. Measured waveforms of V_{GS}, V_{DS}, I_D, and V_{EMI} and the timing chart of n_{PMOS} at turn-on in Point A to Point C.

459 ps × 222), which will be discussed later. Compared with Point D, the proposed Point E reduces E_{LOSS} from 12 mJ to 7.3 mJ by 39 % at $A_{EXCESS} = 0$.

Fig. 14 shows the measured radiated EMI spectrums of Point D to Point G at turn-off. Point D and the proposed Point E satisfy Limit 2, while Point F and Point G violate Limit 2. Figs. 15 (a) to (d) show the measured waveforms of V_{GS}, V_{DS}, I_D, and V_{EMI} and the timing chart of n_{NMOS} at turn-off in Point D to Point G, respectively. First, Point D and Point E are compared. Looking at the waveforms of V_{DS} and I_D in Figs. 15 (a) and (b), it is clear that E_{LOSS} of Point E is smaller than that of Point D. Next, Point E and Point F in Figs. 15 (b) and (c) are compared. In Fig. 15 (b), a temporary rise in V_{GS} waveform caused by the proposed TD SGG can be clearly seen, which reduces the ringing of V_{DS}, I_D, and V_{EMI}, thereby reducing EMI in Fig. 14.

Interesting Point G which is the worst gate drive in the proposed TD SGG is discussed here. Fig. 13 (b) shows that Point G is the very worst point because it has more E_{LOSS} than the point of the conventional SSG with I_1 [5:0] = 8, which has the largest E_{LOSS} in the conventional SSG, and more EMI than Point F, which has the largest EMI in the conventional SSG. The worst point is the same as the phenomenon observed in [10], which claims that "stop-and-go gate driving is a double-edged sword," and the discussion in [10] helps us understand the cause. As shown in Fig. 15 (d), when the first gate drive of the stop-and-go drive (102 ns in Fig. 15 (d)) is insufficient, a halfway turn-off occurs, resulting in increased E_{LOSS} because V_{DS} rises but I_D remains high during the 90-ns period. For practical use, the worst gate drive (Point G) should be avoided at all costs, making the optimization of t_1 very important in the proposed TD SGG.

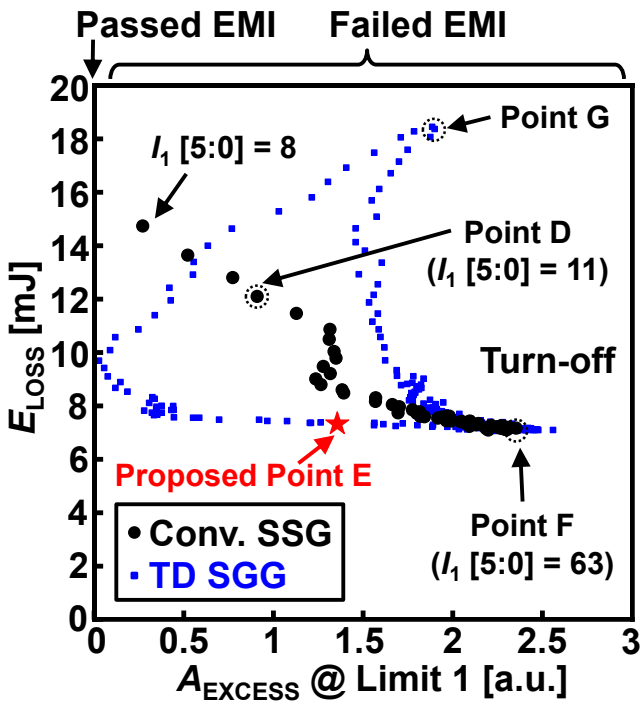
Comparing the turn-on V_{EMI} waveforms (Fig. 12) and the turn-off V_{EMI} waveforms (Fig. 15), the turn-on V_{EMI} waveforms contain high-frequency ringing, while the turn-off V_{EMI} waveforms do not, which results in a significant difference in the magnitude of the high-frequency components of the turn-on EMI spectrum (Fig. 11) and the turn-off EMI spectrum (Fig. 14). The reason for the difference is that the main circuit current loops are different for turn-on and turn-off. In the measurements at turn-on, the high-frequency ringing is observed in V_{EMI} due to the ESL of the main circuit capacitor in Fig. 6. As evidence, the high-frequency ringing in V_{EMI} disappeared when the main circuit capacitor was replaced with a capacitor with a smaller ESL.

E. Comparison with Previous Works

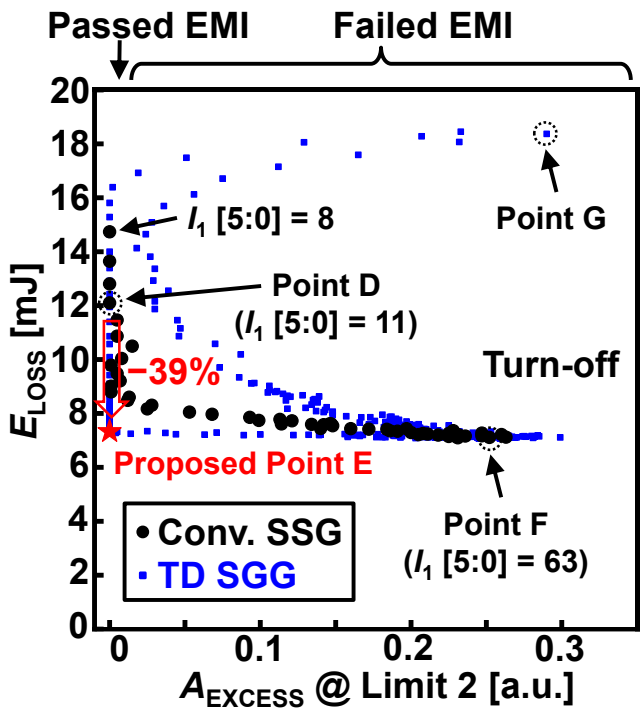
Table I shows a comparison table of DGD ICs. All conventional DGDs [4–5, 7–8] are CD DGDs, not TD DGD. This work is the first time-domain DGD achieving 459-ps step, 10-bit timing control. The output voltage swing of this work is the largest.

IV. Conclusions

This work is the first time-domain DGD achieving 459-ps step, 10-bit timing control. In the measurement of the radiated EMI spectrums from 30 MHz to 100 MHz in the full SiC module at 600 V and 300 A, the proposed TD SGG using TD



(a) Limit 1: VA_{LIMIT} = −15 dB



(b) Limit 2 : VA_{LIMIT} = −5 dB

Fig. 13. Measured E_{LOSS} vs. A_{EXCESS} in turn-off at Limit 1 and Limit 2. The conventional SSG and the proposed TD SGG are compared.

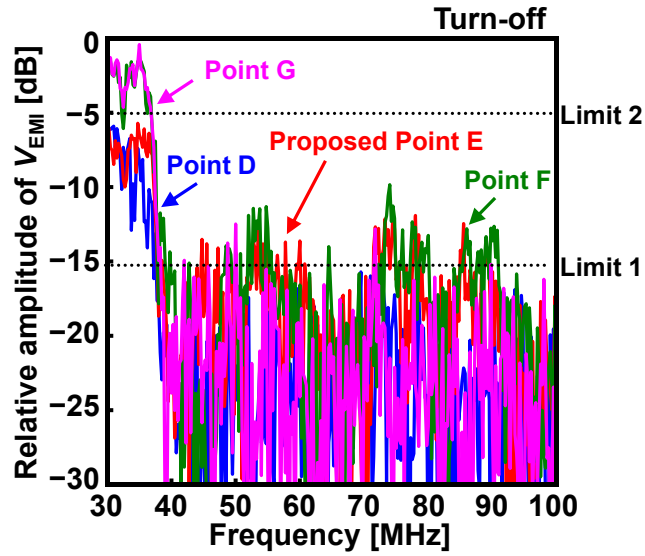


Fig. 14. Measured radiated EMI spectrums of Point D to Point G at turn-off.

Table I. Comparison table of DGD ICs.

	TIA'17 [4]	ISPSD'20 [5]	ISPSD'21 [7]	TPEL'21 [8]	This work
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	SiC MOSFET
Process	180 nm BCD	180 nm BCD	180 nm BCD	180 nm HV CMOS	180 nm BCD
Output voltage swing	15 V	3.3 V	5 V	5 V	30 V
Time-domain digital control	No	No	No	No	Yes
Time resolution	40 ns	0.3–3.0 ns	3.3 ns	1.25 ns (coarse), 100 ps (fine)	t_1: 459 ps × 10 bit t_2: 6 ns × 4 bit
Time steps	No limit	8	16	104	2
Levels of I_G	6 bit	7 bit	6 bit	8 bit (coarse), 6 bit (fine)	6 bit
Max. I_G	5 A	3.3 V / 0.5 Ω = 6.6 A	5 A	5 V / 0.12 Ω = 42 A	22 A

DGD IC fabricated with 180-nm BCD process reduces E_{LOSS} from 2.6 mJ to 1.3 mJ by 50 % and from 12 mJ to 7.3 mJ by 39 % compared with the conventional SSG while satisfying the EMI Limit 2 of − 5 dB in turn-on and turn-off, respectively.

References

[1] N. Oswald, P. Anthony, N. McNeill, and B. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2393–2407, Aug. 2013.

[2] X. Yang, Y. Yuan, X. Zhang, and P. Palmer, "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation," *IEEE Trans. on Industry Applications*, vol. 51, issue 2, pp. 1669–1677, March-April 2015.

[3] H. Dymond, J. Wang, D. Liu, J. Dalton, N. McNeill, D. Pamunuwa, S. Hollis, and B. Stark, "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. on Power Electronics*, vol. 33, no. 1, pp. 581–594, Mar. 2017.

[4] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, and T. Sakurai, "General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by

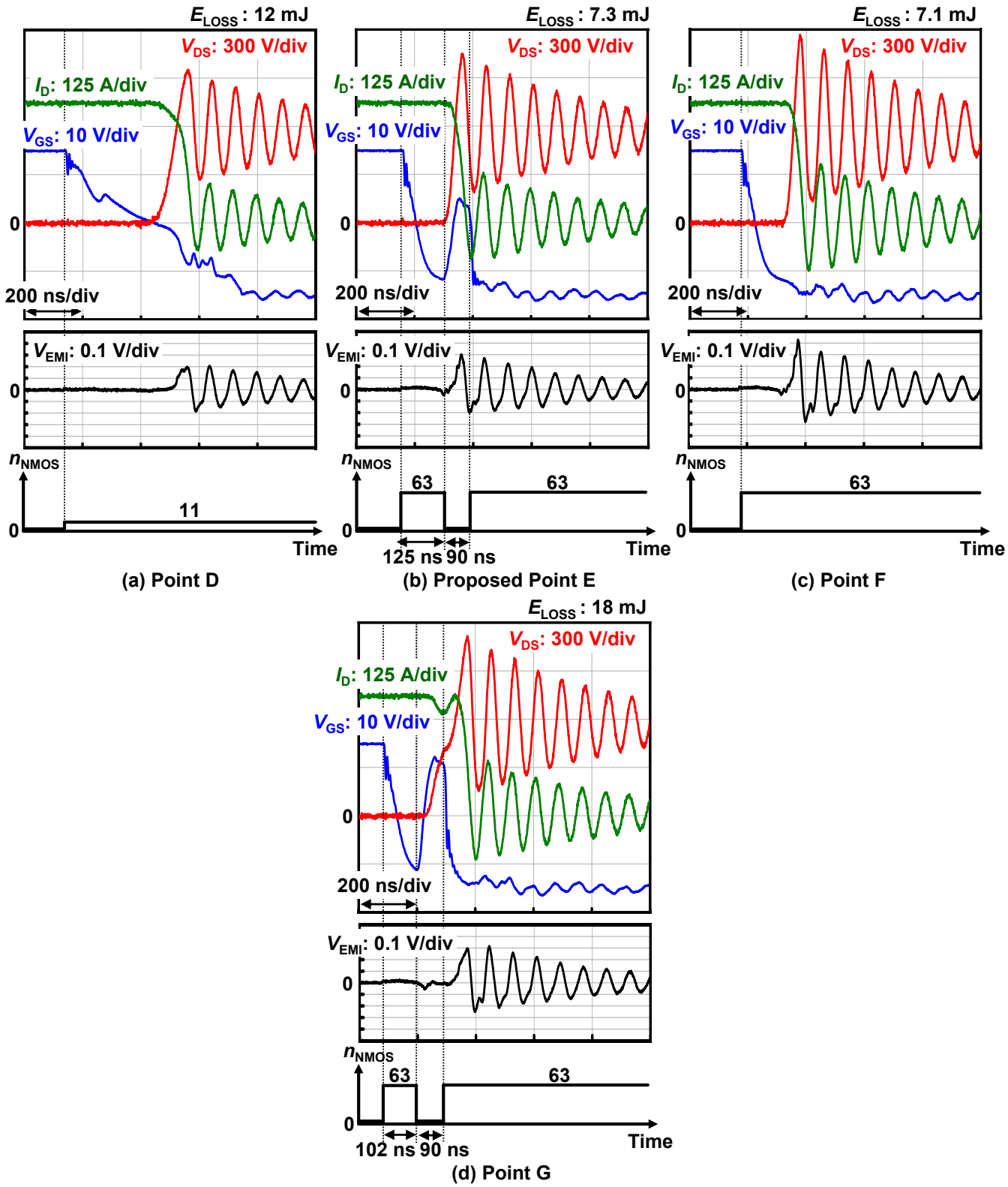


Fig. 15. Measured waveforms of V_{GS}, V_{DS}, I_D, and V_{EMI} and the timing chart of n_{NMOS} at turn-off in Point D to Point G.

vol. 53, issue 3, pp. 2350–2357, May-Jun. 2017.

[5] W. J. Zhang, J. Yu, Y. Leng, W. T. Cui, G. Q. Deng and W. T. Ng, “A segmented gate driver for E-mode GaN HEMTs with simple driving strength pattern control,” in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, Sep. 2020, pp. 102–105.

[6] R. Morikawa, T. Sai, K. Hata, and M. Takamiya, "Automatic generation of gate driving vectors for digital gate drivers to satisfy EMI regulations," in *Proc. IEEE Energy Conversion Congress & Exposition*, Oct. 2020, pp. 4931-4936.

[7] R. Katada, K. Hata, Y. Yamauchi, T. Wang, R. Morikawa, C. Wu, T. Sai, P. Chen, and M. Takamiya, “5 V, 300 MSa/s, 6-bit digital gate driver IC for GaN achieving 69 % reduction of switching loss and 60 % reduction of current overshoot’’, in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, May 2021, pp. 55–58.

[8] D. Liu, H. C. P. Dymond, S. J. Hollis, J. Wang, N. McNeill, D. Pamunuwa, and B. H. Stark, “Full custom design of an arbitrary waveform gate driver with 10-GHz waypoint rates for GaN FETs,” *IEEE Trans. on Power Electronics*, vol. 36, no. 7, pp. 8267–8279, July 2021.

[9] T. Sai, K. Miyazaki, H. Obara, T. Mannen, K. Wada, I. Omura, T. Sakurai, and M. Takamiya, “Stop-and-go gate drive minimizing test cost to find optimum gate driving vectors in digital gate drivers,” in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March 2020, pp. 3096-3101.

[10] R. Katada, K. Hata, Y. Yamauchi, T. -W. Wang, R. Morikawa, C. -H. Wu, T. Sai, P. -H. Chen, and M. Takamiya, "Digital gate driving (DGD) is double-edged sword: how to avoid huge voltage overshoots caused by DGD for GaN FETs," in Proc. IEEE Energy Conversion Congress & Exposition, Oct. 2021, pp. 5412-5416.