

# Large-Current Output Digital Gate Driver for 6500 V, 1000 A IGBT Module to Reduce Switching Loss and Collector Current Overshoot

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**Abstract**—An 8-bit digital gate driver (DGD) using a half-bridge digital-to-analog converter IC and two power MOSFETs is proposed to enable the output voltage swing of  $\pm 15$  V and the large gate current up to 28 A to reduce the switching loss ( $E_{LOSS}$ ) and the collector current overshoot ( $I_{OVERSHOOT}$ ) in a high-voltage, large-current IGBT module (HVIGBT) rated at 6500 V and 1000 A. By using the DGD to drive HVIGBT, the effectiveness of the active gate driving (AGD) is demonstrated for the first time in the world in the high-voltage and large-current range of 3.0–4.5 kV, 1000 A. The values of 1000 A, 4500 V, and  $\pm 15$  V are the world's highest records in AGD. For the purpose of investigating the optimum gate driving waveforms of AGD for HVIGBT, four different gate drive methods are compared in detail by measurements at 3.6 kV, 1000 A, and the stop-and-go gate driving is selected from a cost–performance perspective. Finally, a design guideline of AGD for HVIGBTs is clarified. The design guideline is to align the two peak heights of the collector current waveforms, thereby minimizing  $E_{LOSS}$  and  $I_{OVERSHOOT}$ .

**Index Terms**—Gate driver, IGBT, loss, overshoot.

## I. INTRODUCTION

THE needs for power electronics' applications in the high-voltage, large-current area, such as renewable energy and high-voltage dc transmission systems, are rapidly increasing to realize the carbon neutral society. Thus, it is very important to reduce the losses of the high-voltage, large-current power devices. Active gate drivers (AGDs), which control gate waveforms during the switching transient of power devices, and

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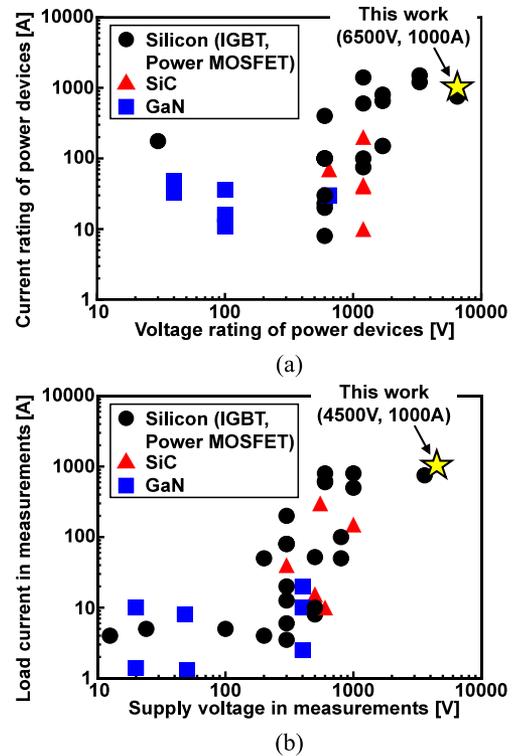


Fig. 1. (a) Voltage and current ratings of power devices and (b) supply voltage and load current of measurements in previous papers on AGDs [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36] by type of power devices.

digital gate drivers (DGDs), which digitize AGDs, have attracted attention as technologies that simultaneously reduce both the switching loss ( $E_{LOSS}$ ) and the switching noise.

Fig. 1(a) shows the voltage and current ratings of power devices used in previous papers on AGDs by type of power devices [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36]. There have been few reports on AGDs of power devices above 3000 V and 1000 A. Fig. 1(b) shows the supply voltage and the load current of measurements in previous papers on AGDs by type of power devices [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18],

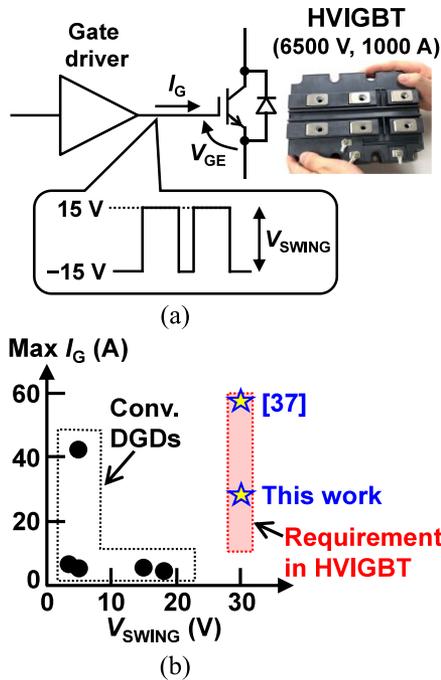


Fig. 2. (a) Definitions of gate current ( $I_G$ ) and gate swing voltage ( $V_{SWING}$ ). (b) Maximum  $I_G$  versus  $V_{SWING}$  of previously reported DGDs [11], [19], [24], [25], [26] and requirements in HVIGBT.

[19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36]. No measurements above 3600 V or 800 A are reported. Therefore, the effectiveness of AGDs in high-voltage, large-current regions above 3600 V and 800 A is unproven and unknown, even though the absolute value of  $E_{LOSS}$  increases in power electronics' applications in the high-voltage, large-current area, making the need for  $E_{LOSS}$  reduction by AGDs increasingly important.

To solve the problem, the research contributions of this article are the following two points.

- 1) This article is the first to demonstrate the advantages of AGDs in a double pulse test at the world's highest voltage (4.5 kV) and the largest load current (1000 A) using the 6500 V, 1000 A IGBT modules, defined as high-voltage IGBTs (HVIGBTs).
- 2) To enable the active gate driving in the 6500 V, 1000 A IGBT module, a new DGD with a maximum gate current ( $I_G$ ) of 28 A and the world's largest gate swing voltage ( $V_{SWING}$ ) of 30 V in DGDs is developed in this article.

Fig. 2(a) shows the definitions of  $I_G$  and  $V_{SWING}$ . Fig. 2(b) shows the maximum  $I_G$  versus  $V_{SWING}$  of the previously reported DGDs [11], [19], [24], [25], [26] and the requirements in HVIGBT. The 6500 V, 1000 A IGBT module (CM1000HG-130XA) used in this work requires a maximum  $I_G$  of at least 10 A and the gate-to-emitter voltage ( $V_{GE}$ ) of  $\pm 15$  V or  $V_{SWING} = 30$  V. As shown in Fig. 2(b), however, none of the previously reported DGDs satisfy the above required specifications. Therefore, in this article, a DGD that satisfies the required specifications is newly developed.

In addition, a new DGD circuit technology combining a half-bridge digital-to-analog converter (HB DAC) IC and two power

MOSFETs is proposed to solve the problem of cost increase due to the increased chip area of DGD ICs with large  $I_G$ . By using the proposed circuit technology, a DGD with large  $I_G$  has been successfully realized in the small chip area, namely at low cost.

This article is an extended version of the conference paper [37]. The two main additions to the conference paper [37] are described as follows.

- 1) The conference paper [37] compared  $E_{LOSS}$  and the collector current overshoot ( $I_{OVERSHOOT}$ ) reduction of two different gate drive methods, including the conventional single-step gate driving (SGD) and the stop-and-go gate driving (S&G) [20], which is a type of active gate driving. In contrast, in this article,  $E_{LOSS}$  and  $I_{OVERSHOOT}$  of four different gate drive methods, two-variable digital gate driving (2DG) with two slots, and four-variable digital gate driving (4DG) with four slots in addition to the above two are compared. The details of the four different gate drive methods are described later in Fig. 10. In addition, in this article, three types of active gate driving (S&G, 2DG, and 4DG) are compared in terms of  $E_{LOSS}$  and  $I_{OVERSHOOT}$  reduction performance and in terms of test cost to find the optimal gate driving parameters, and S&G is used in subsequent measurements from a cost-performance perspective. These details are explained in Section III.
- 2) In the conference paper [37], only the measured results of the double pulse tests under one condition of the power supply voltage ( $V_{CC}$ ) of 3.0 kV and the load current ( $I_L$ ) of 1000 A were shown because the proposed HB DAC IC was broken by overvoltage when  $V_{CC}$  was increased to 3.6 kV. In contrast, in this article, the measured results of the double pulse tests under four conditions of  $V_{CC} = 3.0$  kV, 3.6 kV, 4.0 kV, and 4.5 kV, and  $I_L = 1000$  A, suitable for the target 6500 V, 1000 A IGBT module, are successfully obtained because the proposed HB DAC IC is not broken by overvoltage by fully revising the PCB design of DGD. As a result,  $V_{CC}$  dependence of the  $E_{LOSS}$  reduction performance of the active gate driving, which is most important for the target 6500 V, 1000 A IGBT module, is clarified. In addition, a design guideline for the optimum gate driving parameters of the active gate driving for  $V_{CC}$  changes is clarified. These details are explained in Section IV.

## II. DESIGN OF DGD USING HB DAC IC AND TWO POWER MOSFETs

Fig. 3 shows a circuit schematic of the proposed DGD, including HB DAC IC and two power MOSFETs ( $Q_1$  and  $Q_2$ : IRLZ34NS, 55 V, 30 A). This DGD is a two-stage gate drive system: first the HB DAC IC drives the two power MOSFETs, and then the two power MOSFETs drive the IGBT. DGD is a current-source gate driver. HB DAC IC does not include the output stage to drive IGBTs. The two power MOSFETs ( $Q_1$  and  $Q_2$ ) work as the output stage. If the output stage that can output more than 20 A of  $I_G$ , which is the target of this article, is also integrated into the IC, the chip size will be huge and the cost will be high, which is unacceptable. Therefore, in this article, a DGD



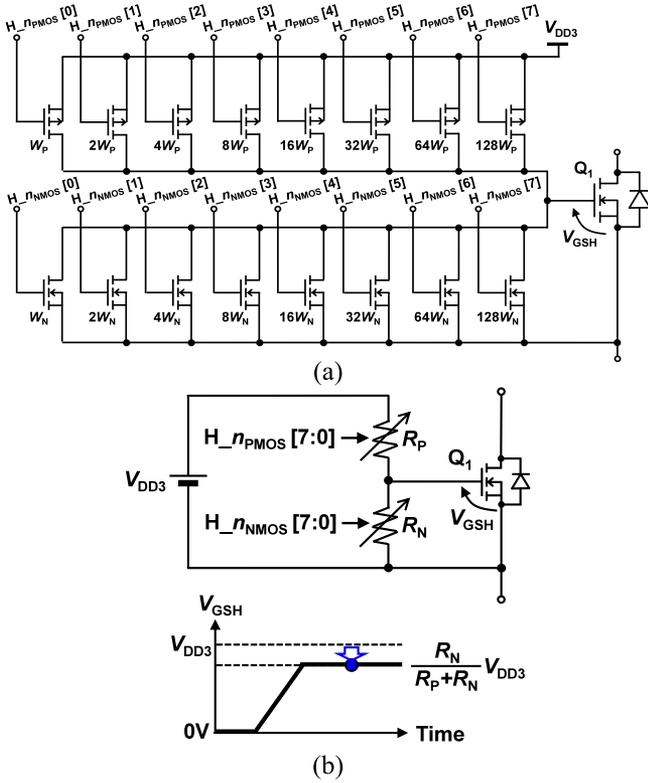


Fig. 6. (a) Circuit schematic and (b) equivalent circuit of 16-bit input DAC for  $Q_1$ .

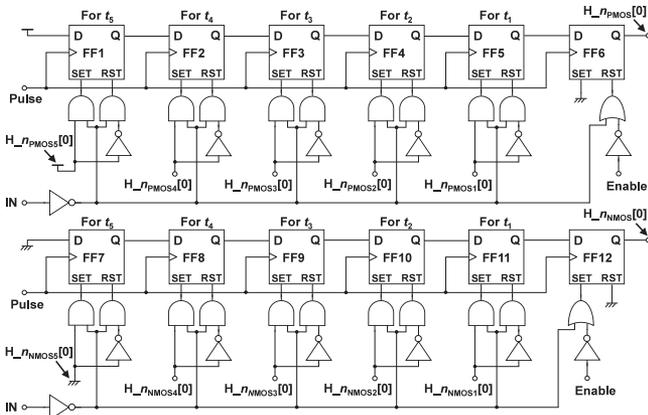


Fig. 7. Circuit schematic of high-side PISO for one bit ( $H\_nPMOS [0]$  and  $H\_nNMOS [0]$ ).

not properly set. Specifically, as shown in Fig. 7, when Enable is set to low, FF6 is reset and  $H\_nPMOS [0]$  is low, and FF12 is set and  $H\_nNMOS [0]$  is high. As a result,  $V_{GSH}$  is 0 V and IGBT is definitely turned OFF. In the subsequent operating mode (Enable = high), during the period of IN = low, i.e., IGBT is OFF, the control signals for the four slots from  $t_1$  to  $t_4$  ( $H\_nPMOS_1 [0]$  to  $H\_nPMOS_4 [0]$  and  $H\_nNMOS_1 [0]$  to  $H\_nNMOS_4 [0]$ ) given by SIPO are fed into FF2–FF5 and FF8–FF11. As shown in Fig. 7, in this article, during  $t_5$ ,  $H\_nPMOS_5 [0]$  is fixed to high and  $H\_nNMOS_5 [0]$  is fixed to low, resulting in  $H\_nPMOS$  being fixed to 255 and  $H\_nNMOS$  to 0. Then, when IN = high, each

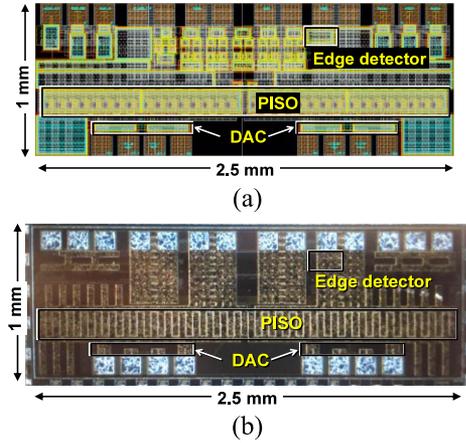


Fig. 8. (a) Layout and (b) die micrograph of HB DAC IC fabricated with 180-nm BCD process.

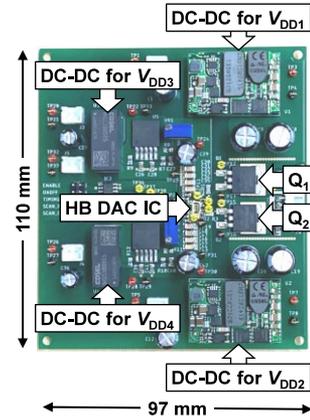


Fig. 9. Photograph of PCB of DGD.

time the pulse signal is received, the data in FFs are shifted one bit to the right to achieve five-slot  $I_G$  control. The circuit schematic of the low-side PISO is also similar to Fig. 7. When the two CMOS inverters with IN input are removed from Fig. 7, the circuit schematic of the low-side PISO is obtained.

Fig. 8(a) and (b) show a layout and a die micrograph of HB DAC IC fabricated with 180-nm BCD process, respectively. The die size is  $2.5 \text{ mm} \times 1.0 \text{ mm}$ . As explained in Fig. 3, note that the DAC area is small ( $0.014 \text{ mm}^2$ ) because the HB DAC IC does not include the output stage of DGD. As a result, the proposed HB DAC IC is low cost because of its small chip area, although the DGD can output the maximum  $I_G$  of 28 A.

Fig. 9 shows a photograph of PCB of DGD. As described in Section I, PCB of DGD in this article makes the following three design revisions to PCB of DGD in the conference paper [37].

- 1) Transient-voltage-suppression diodes are added to  $V_{GSH}$ ,  $V_{GSL}$ ,  $V_{DD3}$ , and  $V_{DD4}$  in Fig. 3 to prevent overvoltage breakdown of the proposed HB DAC IC.
- 2) The two power MOSFETs ( $Q_1$  and  $Q_2$ ) are changed from BSC094N06LS5 (60 V, 47 A) to IRLZ34NS (55 V, 30 A) because  $I_G$  of BSC094N06LS5 was too much for the output voltage of the HB DAC IC ( $V_{GSH}$ ,  $V_{GSL}$ ), specifically,

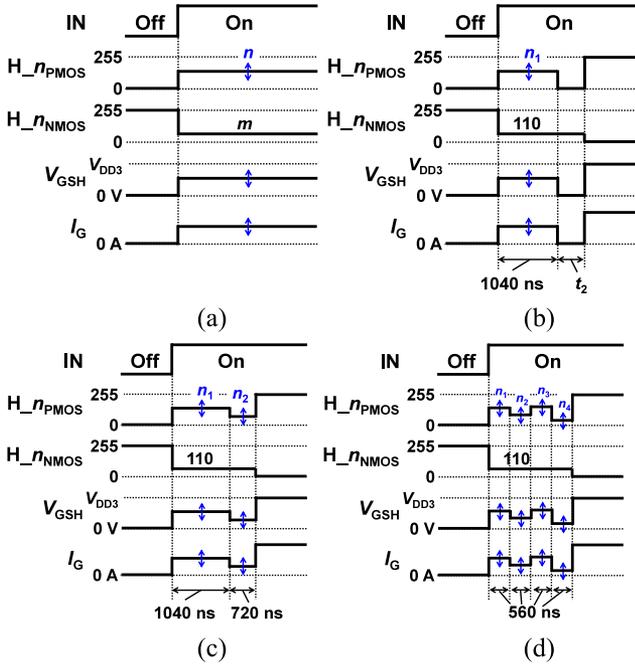


Fig. 10. Timing charts of turn-ON measurements for four different gate drive methods compared in this article. (a) Conventional SGD. (b) S&G gate driving. (c) Two-variable digital gate driving with two slots. (d) Four-variable digital gate driving with  $560 \text{ ns} \times 4$  slots.

$I_G$  is 15 A to 68 A at  $V_{GSH} = V_{GSL} = 3 \text{ V}$  to  $4 \text{ V}$  in BSC094N06LS5, while  $I_G$  is 6 A to 25 A at  $V_{GSH} = V_{GSL} = 3 \text{ V}$  to  $4 \text{ V}$  in IRLZ34NS.

- 3) Four isolated dc-dc converters for  $V_{DD1}$ – $V_{DD4}$  are mounted on the PCB to stabilize the power supply to DGD.

### III. COMPARISON OF FOUR DIFFERENT GATE DRIVE METHODS IN 6500 V, 1000 A IGBT MODULE

In this article, the comparison of four different gate drive methods in the 6500 V, 1000 A IGBT module is performed by measurements using the developed gate driver. In this article, only  $I_{\text{OVERSHOOT}}$  at turn-ON is discussed and the collector-emitter voltage ( $V_{CE}$ ) overshoot at turn-OFF is not discussed because  $I_{\text{OVERSHOOT}}$  is large, while the voltage overshoot is small, being less than 500 V.

#### A. Definition of Four Different Gate Drive Methods

Fig. 10(a)–(d) show the timing charts of the turn-ON measurements for the four different gate drive methods compared in this article, including the conventional SGD [see Fig. 10(a)], the S&G gate driving [20] [see Fig. 10(b)], 2DG with two slots [see Fig. 10(c)], and 4DG with  $560 \text{ ns} \times 4$  slots [see Fig. 10(d)].

The steps for determining the values of the slots ( $t_1$ – $t_4$ ) in the 4DG in Fig. 10(d) are explained below. As shown in Figs. 5 and 10(d), this DGD has a total of eight variables of freedom:  $t_1$ – $t_4$  and  $n_1$ – $n_4$ . However, since parameter optimization of eight variables is difficult to implement,  $t_1$ – $t_4$  were fixed and parameter optimization of four variables of  $n_1$ – $n_4$  was performed in this article.

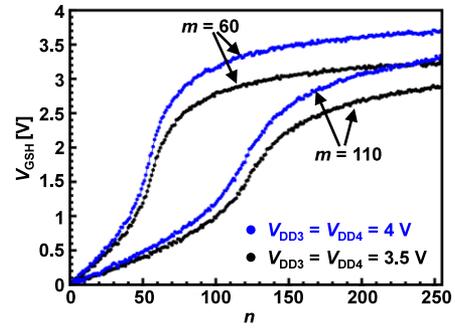


Fig. 11. Measured  $n$  dependence  $V_{GSH}$  in SGD to demonstrate the successful operation of 8-bit DAC at  $V_{DD3} = V_{DD4} = 3.5 \text{ V}$  and  $4 \text{ V}$  and  $m = 60$  and  $110$ .

- (Step 1) Examine the turn-ON delay ( $t_{d(\text{on})}$ ) and the turn-ON rise time ( $t_r$ ) shown in the datasheet of IGBT and determine  $t_{\text{TOTAL}}$  defined by the following:

$$t_{d(\text{on})} + t_r < t_1 + t_2 + t_3 + t_4 \equiv t_{\text{TOTAL}}. \quad (1)$$

$t_{\text{TOTAL}}$  is set to 2 ms because  $t_{d(\text{on})} = 1.2 \text{ ms}$  and  $t_r = 0.3 \text{ ms}$  for this HVIGBT.

- (Step 2) Determine  $t_1$ – $t_4$  by the following equation:

$$t_1 = t_2 = t_3 = t_4 = \frac{t_{\text{TOTAL}}}{4}. \quad (2)$$

The calculation results in  $t_1 = t_2 = t_3 = t_4 = 500 \text{ ns}$ . In the measurements, however, instead,  $t_1 = t_2 = t_3 = t_4 = 560 \text{ ns}$ , as shown in Fig. 10(d), because the lower limit of the time step of the signal generator that generates “Timing” signal in Fig. 5, which determines the values of  $t_1$ – $t_4$ , is 80 ns.

S&G, 2DG, and 4DG are a kind of active gate driving.  $n$  is varied in SGD,  $n_1$  is varied in S&G, ( $n_1$  and  $n_2$ ) are varied in 2DG, and ( $n_1, n_2, n_3$ , and  $n_4$ ) are varied in 4DG, where  $n$  and  $n_1$ – $n_4$  are integers between 0 and 255.  $m$  in SGD is 60 or 110 in this article. SGD with varied  $n$  emulates a conventional gate driver with varied gate resistance. 2DG and 4DG are based on the article presented in [11]. The optimal values of the variables ( $n_1$  and  $n_2$ ) in 2DG and ( $n_1, n_2, n_3$ , and  $n_4$ ) in 4DG (defined as gate vectors in this article) are searched by repeated measurements using the simulated annealing algorithm [11]. Details are explained later. S&G was proposed to reduce the effort of searching for the optimal gate vectors of 4DG [20]. As shown in Fig. 10(b), in S&G,  $I_G$  waveform of “medium–zero–strong” is used. The advantage of S&G is that it has only one variable ( $n_1$ ) while achieving almost the same performance as 4DG [20].

#### B. Measurements of Gate Driver

Fig. 11 shows the measured  $n$  dependence  $V_{GSH}$  in SGD to demonstrate the successful operation of 8-bit DAC at  $V_{DD3} = V_{DD4} = 3.5 \text{ V}$  and  $4 \text{ V}$  and  $m = 60$  and  $110$ .  $V_{GSH}$  is monotonically increasing with  $n$ , although DAC is nonlinear. The maximum output current of DAC is 100 mA. Fig. 12 shows the measured  $n$  dependence of  $I_G$  in SGD to demonstrate the successful operation of 8-bit DGD at  $V_{DD3} = V_{DD4} = 3.5 \text{ V}$  and  $4 \text{ V}$  and  $m = 60$  and  $110$ . To investigate the performance

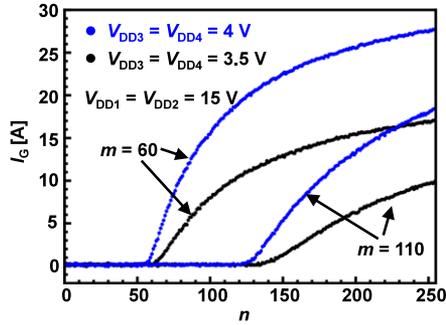


Fig. 12. Measured  $n$  dependence of  $I_G$  in SGD to demonstrate the successful operation of 8-bit DGD at  $V_{DD3} = V_{DD4} = 3.5$  V and 4 V and  $m = 60$  and 110.

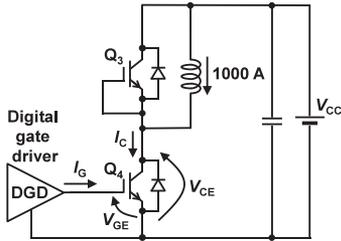


Fig. 13. Circuit schematic of double pulse test using DGD and two IGBT modules ( $Q_3$  and  $Q_4$  : CM1000HG-130XA, 6500 V, 1000 A).

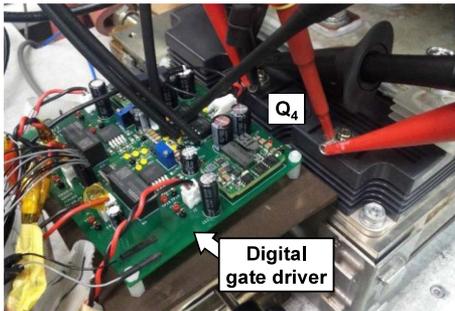
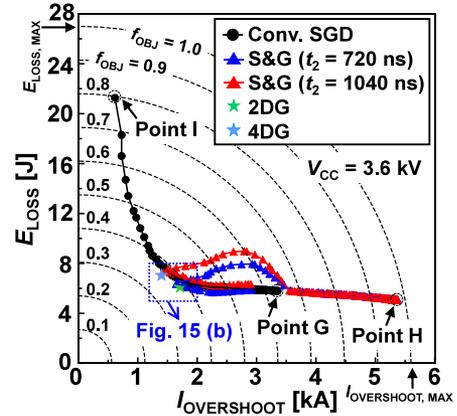


Fig. 14. Measurement setup of double pulse test using DGD and IGBT modules.

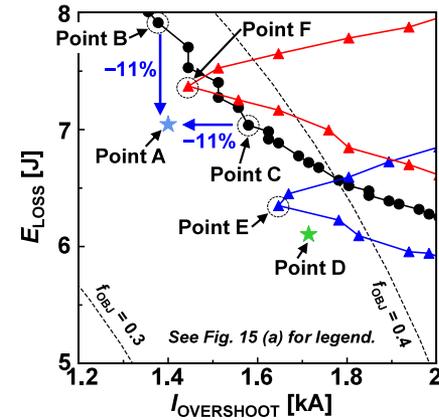
of DGD itself, a 100  $\mu$ F capacitor is connected to the output of DGD and  $I_G$  is measured.  $I_G$  is monotonically increasing with  $n$ , although it is nonlinear. The maximum  $I_G$  is 28 A. In all following measurements in this article, measurements are performed under condition of  $V_{DD3} = V_{DD4} = 3.5$  V and  $m = 110$ , with the maximum  $I_G$  of 10 A because 10 A is enough to actively drive the target IGBT.

### C. Measurements of $E_{LOSS}$ Versus $I_{OVERSHOOT}$ in 6500 V, 1000 A IGBT Module

Figs. 13 and 14 show a circuit schematic and a measurement setup of the double pulse test using DGD and two IGBT modules ( $Q_3$  and  $Q_4$  : CM1000HG-130XA, 6500 V, 1000 A), respectively. In the measurement, as shown in Fig. 13, the proposed DGD is isolated by the four isolated dc-dc converters, as shown in Fig. 9 (CHS1202412 for  $V_{DD1}$  and  $V_{DD2}$  and MGS100505 for  $V_{DD3}$  and  $V_{DD4}$ ) and the signal isolator IC (IL260-3E).



(a)



(b)

Fig. 15. (a) Overall view of the measured  $E_{LOSS}$  versus  $I_{OVERSHOOT}$  of four different gate drive methods for comparison at  $V_{CC} = 3.6$  kV. (b) Enlarged view of (a).

In this experiment, the signal isolator IC was used to simplify the measurement setup. Optical isolators, however, have been originally used in the HVIGBTs. Therefore, if the signal isolator IC is replaced with the optical isolator, the proposed DGD will be able to drive the high-side IGBT ( $Q_3$ ), as shown in Fig. 13, normally without causing CMRR-induced malfunctions.

The measurement conditions are room temperature and  $I_L$  of 1000 A. The power supply voltage ( $V_{CC}$ ) of the main circuit in Section III is 3.6 kV.

Fig. 15(a) and (b) show the overall view of the measured  $E_{LOSS}$  versus  $I_{OVERSHOOT}$  of four different gate drive methods for comparison at  $V_{CC} = 3.6$  kV and an enlarged view of Fig. 15(a), respectively. This article discusses the switching at turn-ON and does not discuss the switching at turn-OFF because  $I_{OVERSHOOT}$  is large,  $V_{CE}$  overshoot at turn-OFF is small, being less than 500 V in the HVIGBT. The definition of  $E_{LOSS}$  at turn-ON is given as follows:

$$E_{LOSS} = \int_{t_0}^{t_1} I_C V_{CE} dt \quad (3)$$

where  $t_0$  is the time when  $I_C$  reaches 10% of  $I_L$ , and  $t_1$  is the time when  $V_{CE}$  reaches 10% of  $V_{CC}$ .

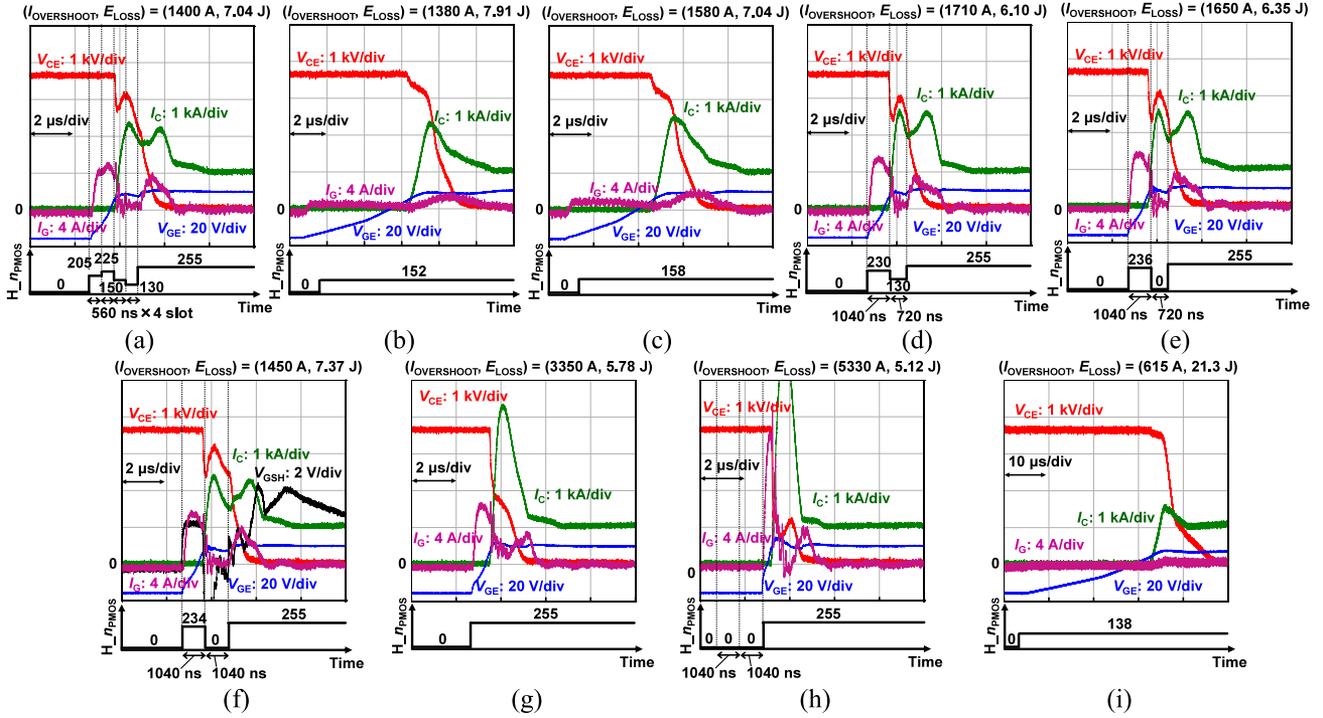


Fig. 16. Gate vectors and measured waveforms from point A to point I in Fig. 15. (a) Point A (4DG). (b) Point B (SGD). (c) Point C (SGD). (d) Point D (2DG). (e) Point E (S&G). (f) Point F (S&G). (g) Point G (SGD). (h) Point H (S&G). (i) Point I (SGD).

TABLE I  
RANKING OF  $f_{OBJ}$  OF POINT A TO POINT I IN FIG. 15 AND DETAILS OF EACH POINT

	Gate driving method	Gate vectors	$E_{LOSS}$ [J]	$I_{OVERSHOOT}$ [A]	$f_{OBJ}$	Ranking of $f_{OBJ}$
Point A	Best point in 4DG	$(n_1, n_2, n_3, n_4) = (205, 225, 150, 130)$	7.04	1400	0.361	1st
Point B	SGD	$n = 152$	7.91	1380	0.383	5th
Point C	SGD	$n = 158$	7.04	1580	0.384	6th
Point D	Best point in 2DG	$(n_1, n_2) = (230, 130)$	6.10	1710	0.381	4th
Point E	Best point in S&G ( $t_2 = 720$ ns)	$n_1 = 236$	6.35	1650	0.377	3rd
Point F	Best point in S&G ( $t_2 = 1040$ ns)	$n_1 = 234$	7.37	1450	0.376	2nd
Point G	SGD	$n = 255$	5.78	3350	0.636	7th
Point H	S&G ( $t_2 = 1040$ ns)	$n_1 = 0$	5.12	5330	0.970	9th
Point I	SGD	$n = 138$	21.3	615	0.795	8th

For S&G, the measured results at two different  $t_2$  are shown because  $t_2$  is the second most important parameter after  $n_1$  in S&G. To quantitatively compare the different gate drive methods, an evaluation function ( $f_{OBJ}$ ) in (4) is defined as a performance index of gate driving [11], and it is discussed that a gate driving with small  $f_{OBJ}$  is an excellent gate driving

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,MAX}}\right)^2 + \left(\frac{I_{OVERSHOOT}}{I_{OVERSHOOT,MAX}}\right)^2} \quad (4)$$

where  $E_{LOSS,MAX}$  is 27 J and  $I_{OVERSHOOT,MAX}$  is 5600 A in this article. The dashed concentric curves in Fig. 15(a) and (b) show the contour of  $f_{OBJ}$  from 0.1 to 1.0. Table I presents

the ranking of  $f_{OBJ}$  of Point A to Point I, the representative points in Fig. 15(a) and (b), and the details of each point. Fig. 16 shows the gate vectors and measured waveforms from Point A to Point I.

A way to estimate IGBT switching characteristics, such as  $dV_{CE}/dt$ ,  $dI_C/dt$ ,  $E_{LOSS}$ , and  $I_{OVERSHOOT}$ , and the controllable performance range when applying this DGD to unknown IGBTs will be explained. The DGD is the current-source gate driver, as described in Fig. 3. Actually, as the measured waveform of  $I_C$  in Fig. 16(c) shows,  $I_C$  is almost constant from  $V_{GE}$  of  $-15$  V to the threshold voltage of IGBT. Therefore, by modeling the DGD as a constant current source and performing SPICE simulations to drive IGBTs, the switching characteristics of IGBTs can be estimated. Furthermore, the controllable performance range of the switching characteristics can be estimated by varying the value of the constant current source in the  $I_C$  range of DGD, as shown in Fig. 12.

1) *Conventional SGD*: The black lines in Fig. 15(a) and (b) show the tradeoff curves of the conventional SGD [see Fig. 10(a)] with varied  $n$  from 138 to 255. The tradeoff curves emulate the conventional gate driving with varied gate resistance, and this study aims to achieve a performance lower left than this tradeoff curve, i.e., low  $E_{LOSS}$  and low  $I_{OVERSHOOT}$ , by active gate driving. Fig. 16(g) and (i) show the measured waveforms at Point G and Point I, where  $I_C$  is maximum and minimum in SGD, respectively.

2) *S&G Gate Driving*: The blue and red lines in Fig. 15(a) and (b) show the measured results of S&G [see Fig. 10(b)] with varied  $n_1$  from 0 to 255 at  $t_2 = 720$  ns and 1040 ns, respectively. Fig. 17(a)–(c) show the measured  $n_1$  dependence of  $E_{LOSS}$ ,

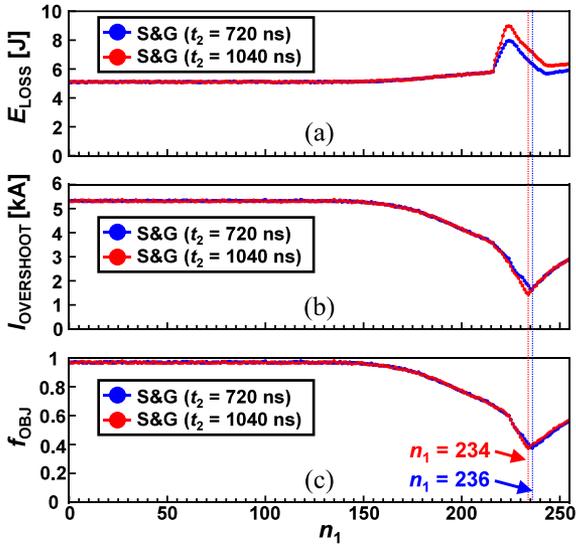


Fig. 17. Measured  $n_1$  dependence of (a)  $E_{\text{LOSS}}$ , (b)  $I_{\text{OVERSHOOT}}$ , and (c)  $f_{\text{OBJ}}$  in S&G.

$I_{\text{OVERSHOOT}}$ , and  $f_{\text{OBJ}}$  in S&G, respectively. When  $n_1$  is varied from 0 to 255,  $E_{\text{LOSS}}$  has the maximum value,  $I_{\text{OVERSHOOT}}$  has the minimum value, and  $f_{\text{OBJ}}$  has the minimum value. By changing the input data given to “Scan In” terminal in Fig. 4 from an external signal generator, the value of  $n_1$  was changed from 0 to 255, and the measurement was repeated 256 times to obtain the results, as shown in Fig. 17.

In S&G at  $t_2 = 720$  ns, the measured point at  $n_1 = 236$  is the best point where  $f_{\text{OBJ}}$  is the minimum, which is Point E in Fig. 15(b). The measured waveforms at Point E are shown in Fig. 16(e). Similarly, in S&G at  $t_2 = 1040$  ns, the measured point at  $n_1 = 234$  is the best point where  $f_{\text{OBJ}}$  is the minimum, which is Point F in Fig. 15(b). The measured waveforms at Point F are shown in Fig. 16(f). As shown in Fig. 17(b),  $I_{\text{OVERSHOOT}}$  is minimum at  $n_1 = 234$ , so  $f_{\text{OBJ}}$  is also minimum at  $n_1 = 234$ . The reason why  $I_{\text{OVERSHOOT}}$  is minimum at  $n_1 = 234$  is explained below. When  $n_1$  is decreased from 234,  $I_{\text{OVERSHOOT}}$  increases because the first peak of  $I_C$  in Fig. 16(f) decreases and the second peak of  $I_C$  increases; thus,  $I_{\text{OVERSHOOT}}$  determined by the second peak increases. In contrast, increasing  $n_1$  from 234 also increases  $I_{\text{OVERSHOOT}}$  because the first peak of  $I_C$  in Fig. 16(f) increases and the second peak of  $I_C$  decreases, thus increasing  $I_{\text{OVERSHOOT}}$  determined by the first peak. Therefore, as shown in Fig. 16(e) and (f), by adjusting  $n_1$  to align the two peak heights of  $I_C$  waveforms,  $E_{\text{LOSS}}$  and  $I_{\text{OVERSHOOT}}$  are reduced and the best point with the smallest  $f_{\text{OBJ}}$  is achieved in S&G. When  $t_2$  is increased in S&G from 720 ns (Point E) to 1040 ns (Point F), as shown in Fig. 15(b) and Table I,  $I_{\text{OVERSHOOT}}$  decreases from 1650 to 1450 A as the optimum  $n_1$  decreases from 236 to 234, while  $E_{\text{LOSS}}$  increases from 6.35 to 7.37 J. On the other hand, as shown in Table I,  $f_{\text{OBJ}}$  at Points E and F are almost the same, and therefore, it can be said that S&G can tune  $E_{\text{LOSS}}$  and  $I_{\text{OVERSHOOT}}$  of the best point by varying  $t_2$  and  $n_1$ .

At Point H, as shown in Fig. 15(a),  $I_{\text{OVERSHOOT}}$  is at a maximum of 5330 A, as shown in Fig. 16(h), because, as shown

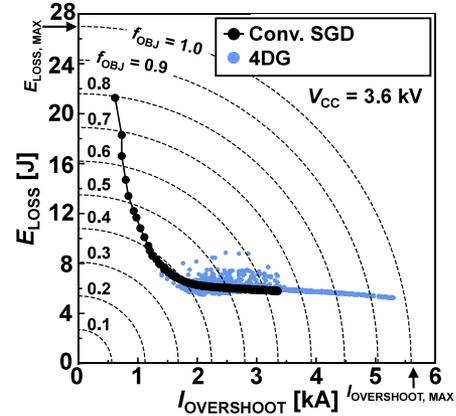


Fig. 18.  $E_{\text{LOSS}}$  versus  $I_{\text{OVERSHOOT}}$  for all 2745 measured points in search process in 4DG at  $V_{\text{CC}} = 3.6$  kV.

TABLE II  
DETAILS OF TOP TEN RANKING OF  $f_{\text{OBJ}}$  IN 2745 MEASURED RESULTS OF 4DG

Ranking of $f_{\text{OBJ}}$	$n_1$	$n_2$	$n_3$	$n_4$	$E_{\text{LOSS}}$ [J]	$I_{\text{OVERSHOOT}}$ [A]	$f_{\text{OBJ}}$
1	205	225	150	130	7.04	1400	0.361
2	204	235	133	147	6.76	1490	0.365
3	230	201	150	130	7.22	1400	0.366
4	255	191	146	157	6.43	1602	0.372
5	206	226	156	171	6.17	1669	0.376
6	191	249	141	130	6.92	1557	0.378
7	239	209	130	205	6.03	1736	0.382
8	187	239	151	154	6.87	1602	0.383
9	255	197	131	204	6.21	1714	0.383
10	222	222	130	179	6.15	1736	0.385

in Fig. 10(b), at the moment  $H_{\text{nPMOS}}$  changes from 0 to 255,  $H_{\text{nNMOS}}$  also changes from 110 to 0, resulting in the maximum  $I_C$  of 14 A in Fig. 16(h).

3) 2DG and 4DG: Points D and A in Fig. 15(a) and (b) are the best points where the smallest  $f_{\text{OBJ}}$  is achieved by repeatedly measuring and searching for  $n_1$  to  $n_2$  and  $n_1$  to  $n_4$  using the simulated annealing algorithm [11] for 2DG [see Fig. 10(c)] and 4DG [see Fig. 10(d)], respectively. In the following, the details of the best point search method in 4DG will be explained, and the exact same method is used for 2DG. In 4DG, using the method of Miyazaki et al. [11], the simulated annealing algorithm was applied to repeatedly perform switching measurements while varying the gate vectors ( $n_1, n_2, n_3$ , and  $n_4$ ), measure  $E_{\text{LOSS}}$  and  $I_{\text{OVERSHOOT}}$ , calculate  $f_{\text{OBJ}}$ , and search for the gate vector that minimizes  $f_{\text{OBJ}}$ .

Fig. 18 shows  $E_{\text{LOSS}}$  versus  $I_{\text{OVERSHOOT}}$  for all 2745 measured points in the search process in 4DG at  $V_{\text{CC}} = 3.6$  kV. Fig. 18 also shows the tradeoff curve of the conventional SGD for comparison. 4DG has many measurement points to the lower left of the tradeoff curve of SGD. Fig. 19 shows the time series of gate vectors,  $E_{\text{LOSS}}$ ,  $I_{\text{OVERSHOOT}}$ , and  $f_{\text{OBJ}}$  for 2745 search measurements in 4DG. The simulated annealing algorithm is used to search the gate vectors ( $n_1, n_2, n_3$ , and  $n_4$ ). It can be seen that  $f_{\text{OBJ}}$  varies greatly at the beginning of the search, while at the end of the search,  $f_{\text{OBJ}}$  converges to a constant value, indicating that the search has been completed. Table II presents the details

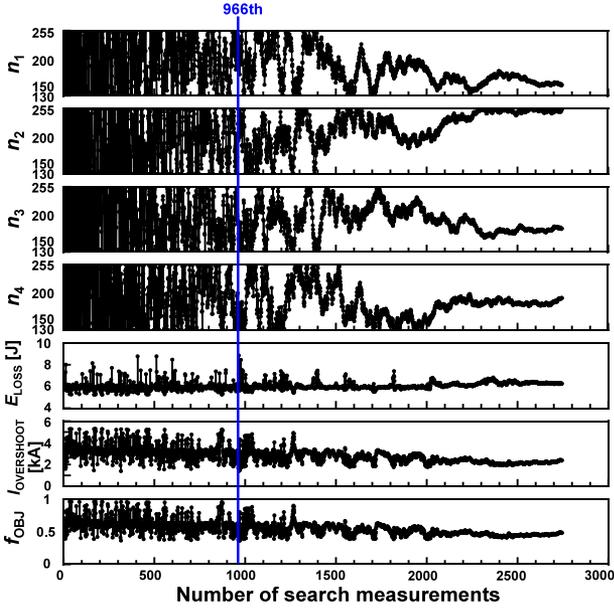


Fig. 19. Time series of gate vectors,  $E_{LOSS}$ ,  $I_{OVERSHOOT}$ , and  $f_{OBJ}$  for 2745 search measurements in 4DG.

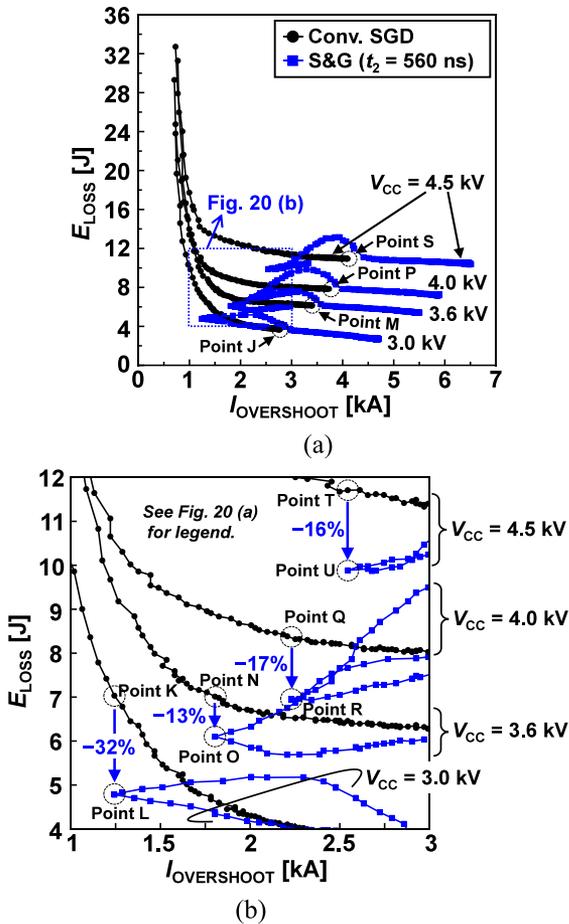


Fig. 20. (a) Overall view of the measured  $V_{CC}$  dependence of  $E_{LOSS}$  versus  $I_{OVERSHOOT}$  of the conventional SGD and S&G at  $t_2 = 560$  ns at room temperature and the load current of 1000 A. (b) Enlarged view of (a).

of the top ten ranking of  $f_{OBJ}$  in all 2745 measured results of 4DG. The top ten  $f_{OBJ}$ 's occur near the 1000th search, not at the end of the search. Therefore, in this article, the 966th measured point that achieved the smallest  $f_{OBJ}$  is adopted as the best point in 4DG (Point A) in this study. The measured waveforms of the best points (Point A and Point D) of 4DG and 2DG are shown in Fig. 16(a) and (d), respectively.

#### D. Comparison of Four Different Gate Drive Methods

The four different gate drive methods for the 6500 V, 1000 A IGBT module are compared. As shown in Table I,  $f_{OBJ}$  ranks Point A (best point in 4DG) in first place, Point F (best point in S&G with  $t_2 = 1040$  ns) in second place, Point E (best point in S&G with  $t_2 = 720$  ns) in third place, and Point D (best point in 2DG) in fourth place, with 4DG showing the best performance. As shown in Fig. 15(b), all four points are lower left than the tradeoff curve of SGD, resulting in lower  $E_{LOSS}$  and  $I_{OVERSHOOT}$  than SGD by the active gate driving. As shown in Fig. 15(b), Table I, and Fig. 16(a)–(c), compared with Point B of SGD, Point A (best point in 4DG) reduces  $E_{LOSS}$  from 7.91 to 7.04 J by 11% under  $I_{OVERSHOOT}$ -aligned condition. Compared with Point C of SGD, Point A (best point in 4DG) reduces  $I_{OVERSHOOT}$  from 1580 to 1400 A by 11% under  $E_{LOSS}$ -aligned condition.

Here, the similarities among 4DG, 2DG, and S&G are discussed. Interestingly, comparing the best waveforms of 4DG, 2DG, and S&G in Fig. 16(a) and (d)–(f), the gate vectors are different, while  $V_{GE}$  and  $I_G$  waveforms are similar, and  $I_C$  waveforms have two peaks with equal peak height. Therefore, aligning the two peak heights of  $I_C$  waveforms in the target IGBT is a common design guideline for active gate driving that minimize  $f_{OBJ}$ . Also, comparing Fig. 16(a) and (d)–(f), IG waveforms are “medium–(almost) zero–strong” in common. As shown in Fig. 12, IGs of gate vectors  $n_3 = 150$  and  $n_4 = 130$  in Point A (best point in 4DG) and  $n_2 = 130$  in Point D (best point in 2DG) are almost zero. The same is true for the top ten ranking of  $f_{OBJ}$  of 4DG in Table II, where  $I_G$  waveforms are “medium ( $n_1$  and  $n_2$ )–(almost) zero ( $n_3$  and  $n_4$ )–strong.” Therefore, as shown in Fig. 10(b)–(d), although 4DG, 2DG, and S&G have different gate driving waveform constraints, the derived optimal gate driving waveforms are all “medium–(almost) zero–strong” in common, and their  $f_{OBJ}$ 's are not significantly different, as shown in Table I. Here, the physical reasons why AGD with  $I_G$  waveforms of “medium–(almost) zero–strong” perform better than the conventional SGD are explained. AGD achieves smaller  $f_{OBJ}$  than the conventional SGD by shortening the turn-ON delay in the first medium drive, reducing  $I_{OVERSHOOT}$  in the next (almost) zero drive and reducing  $E_{LOSS}$  in the last strong drive.

On the other hand, the test cost to find the optimum gate vectors for 4DG, 2DG, and S&G is very different. The number of combinations in gate vector for 4DG, 2DG, and S&G is  $(2^8)^4$  ( $>10^9$ ),  $(2^8)^2$  ( $>10^4$ ), and  $2^8$  ( $=256$ ), respectively. In this article, as shown in Fig. 19, the optimization of  $(2^8)^4$  gate vectors of 4DG is successfully performed in only 2745 iterations using the simulated annealing algorithm. The test cost for 4DG is still high

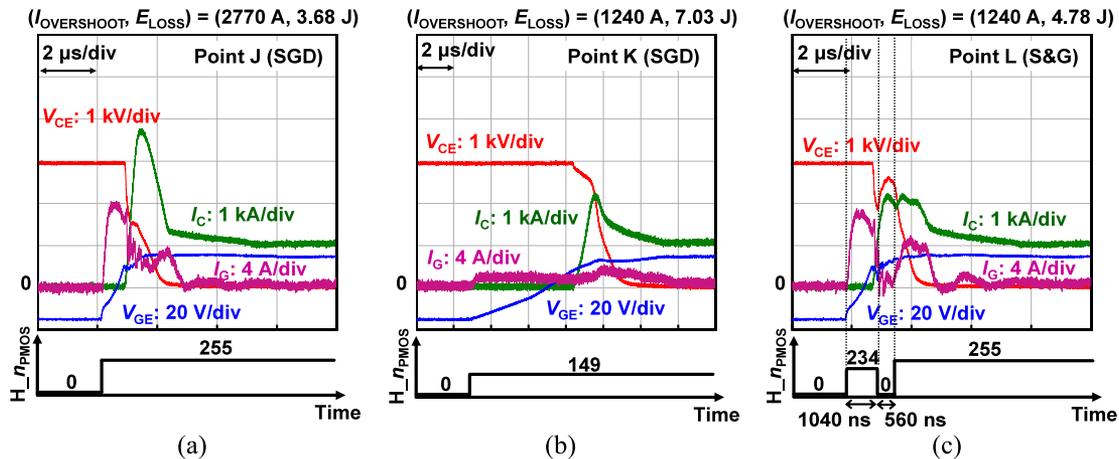


Fig. 21. Gate vectors and measured waveforms from Point J to Point L in Fig. 20 at  $V_{CC} = 3.0$  kV.

because 2745 measurements in 4DG are more than ten times higher than 256 measurements in S&G. As shown in Table I,  $f_{OBJ}$  of Point A (best point in 4DG) is 0.361, while  $f_{OBJ}$  of Point E (best point in S&G with  $t_2 = 720$  ns) is 0.377, and that of Point F (best point in S&G with  $t_2 = 1040$  ns) is 0.376, showing only a small difference. Therefore, in this article, S&G will be used in subsequent measurements from a cost–performance perspective. Adopting S&G eliminates the need for the four slots ( $t_3$ ,  $t_4$ ,  $t_8$ , and  $t_9$ ) in Fig. 5 and, thus, has the advantage of reducing the circuit size of the HB DAC IC, as shown in Fig. 4.

#### IV. $V_{CC}$ DEPENDENCE OF ACTIVE GATE DRIVE IN 6500 V, 1000 A IGBT MODULE

In the target 6500 V, 1000 A IGBT module, the  $V_{CC}$  dependence of  $E_{LOSS}$  reduction effect of the active gate driving is very important yet unknown. For low-voltage, small-current IGBTs (rated 600 V, 100 A), the load current dependence and the temperature dependence of  $E_{LOSS}$  reduction effects of the active gate drive (4DG and S&G) over the conventional SGD have been quantitatively investigated in [16], while the  $V_{CC}$  dependence has not been reported. Therefore, in this article, the  $V_{CC}$  dependence of  $E_{LOSS}$  reduction effect of the active gate driving over the conventional SGD in the 6500 V, 1000 A IGBT module is investigated in detail by measurements.

Fig. 20(a) and (b) show the overall view of the measured  $V_{CC}$  dependence of  $E_{LOSS}$  versus  $I_{OVERSHOOT}$  of the conventional SGD and S&G at  $t_2 = 560$  ns at room temperature and  $I_L$  of 1000 A and an enlarged view of Fig. 20(a), respectively. Note that since the IGBT samples are different in Figs. 15 and 20, the measured results of the two do not match. As shown in Fig. 20(a), when  $V_{CC}$  increases from 3.0 to 4.5 kV, both  $E_{LOSS}$  and  $I_{OVERSHOOT}$  increase, as expected. The points of interest, Point J to Point U, are defined in Fig. 20(a) and (b). The points of maximum  $I_G$  ( $n = 255$ ) of SGD at  $V_{CC} = 3.0$  kV, 3.6 kV, 4.0 kV, and 4.5 kV are defined as Point J, Point M, Point P, and Point S, respectively. The best points with the smallest  $f_{OBJ}$  of S&G at  $V_{CC} = 3.0$  kV, 3.6 kV, 4.0 kV, and 4.5 kV are defined as Point L, Point O, Point R, and Point U, respectively. These four points

are lower left than the tradeoff curve for the conventional SGD, indicating that the S&G advantage is maintained even when  $V_{CC}$  varies from 3.0 to 4.5 kV. The points of SGD with the same  $I_{OVERSHOOT}$  as the best point of S&G at  $V_{CC} = 3.0$  kV, 3.6 kV, 4.0 kV, and 4.5 kV are defined as Point K, Point N, Point Q, and Point T, respectively.

Figs. 21–24 show the gate vectors and the measured waveforms from Point J to Point U at  $V_{CC} = 3.0$  kV, 3.6 kV, 4.0 kV, and 4.5 kV, respectively. As shown in Figs. 21(a), 22(a), 23(a), and 24(a), the maximum  $I_G$  is 8 A. At  $V_{CC} = 3.0$  kV, as shown in Figs. 20 and 21, compared with Point K of the conventional SGD, Point L (best point in S&G) reduces  $E_{LOSS}$  from 7.03 to 4.78 J by 32% under  $I_{OVERSHOOT}$ -aligned condition. At  $V_{CC} = 3.6$  kV, as shown in Figs. 20 and 22, compared with Point N of the conventional SGD, Point O (best point in S&G) reduces  $E_{LOSS}$  from 7.01 to 6.10 J by 13% under  $I_{OVERSHOOT}$ -aligned condition. At  $V_{CC} = 4.0$  kV, as shown in Figs. 20 and 23, compared with Point Q of the conventional SGD, Point R (best point in S&G) reduces  $E_{LOSS}$  from 8.38 to 6.94 J by 17% under  $I_{OVERSHOOT}$ -aligned condition. At  $V_{CC} = 4.5$  kV, as shown in Figs. 20 and 24, compared with Point T of the conventional SGD, Point U (best point in S&G) reduces  $E_{LOSS}$  from 11.7 to 9.88 J by 16% under  $I_{OVERSHOOT}$ -aligned condition.

In summary, in  $V_{CC}$  range from 3.0 to 4.5 kV, the proposed S&G reduces  $E_{LOSS}$  by 13%–32% compared with the conventional SGD under  $I_{OVERSHOOT}$ -aligned condition. This result indicates that applying the proposed S&G to high-voltage converter/inverter systems using the HVIGBTs would reduce  $E_{LOSS}$  by 13%–32%; thus, the benefit of the proposed AGD to high-voltage applications is significant. Interestingly, similar to Section III, comparing the best waveforms of S&G in Figs. 21(c), 22(c), 23(c), and 24(c), IC waveforms have two peaks with equal peak height by tuning  $n_1$  regardless of  $V_{CC}$ . Table III presents  $V_{CC}$  dependence of the optimum  $n_1$  in S&G, as shown in Figs. 21(c), 22(c), 23(c), and 24(c). The common design guideline, as described in Section III, for active gate driving that minimize  $f_{OBJ}$ , aligning the two peak heights of  $I_C$  waveforms, is successfully achieved by increasing  $n_1$  from 234 to 242 as  $V_{CC}$  increases from 3.0 to 4.5 kV.

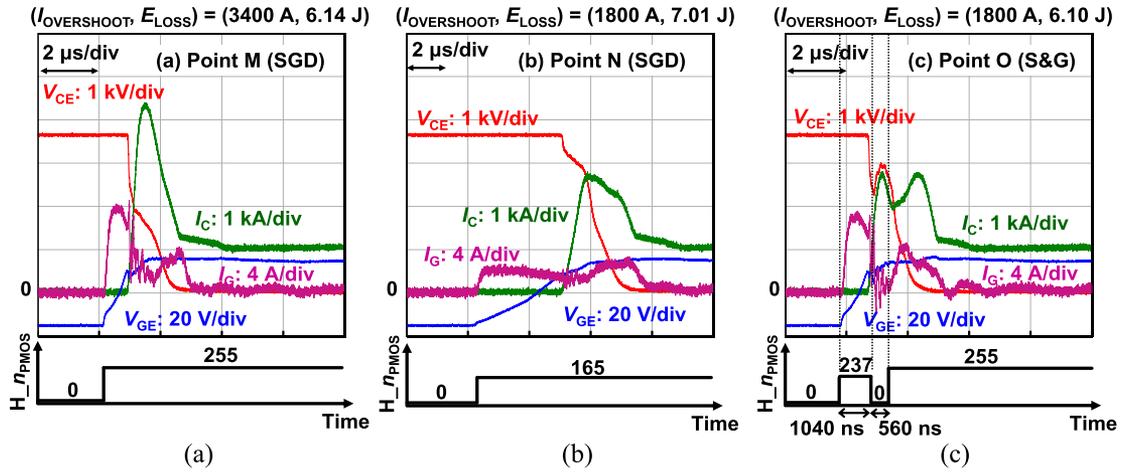


Fig. 22. Gate vectors and measured waveforms from Point M to Point O in Fig. 20 at  $V_{CC} = 3.6$  kV.

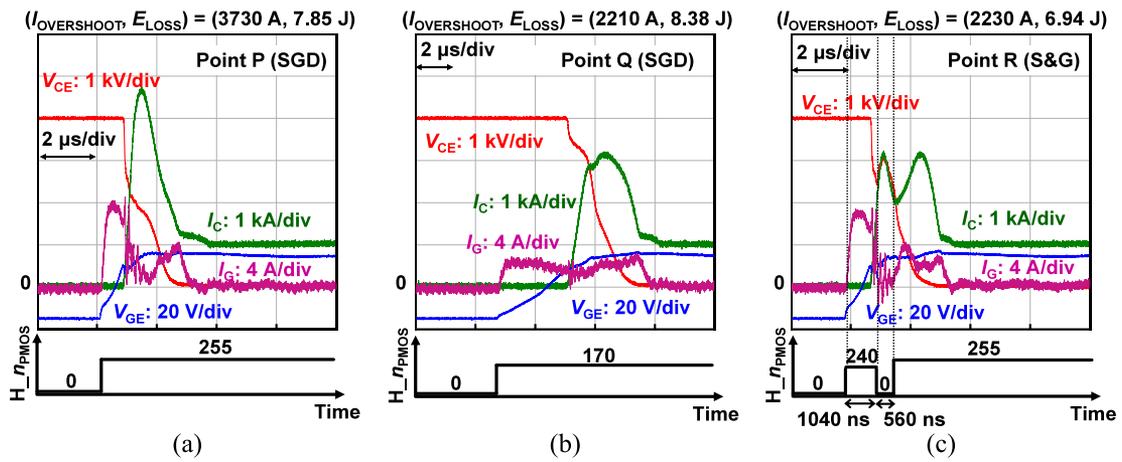


Fig. 23. Gate vectors and measured waveforms from Point P to Point R in Fig. 20 at  $V_{CC} = 4.0$  kV.

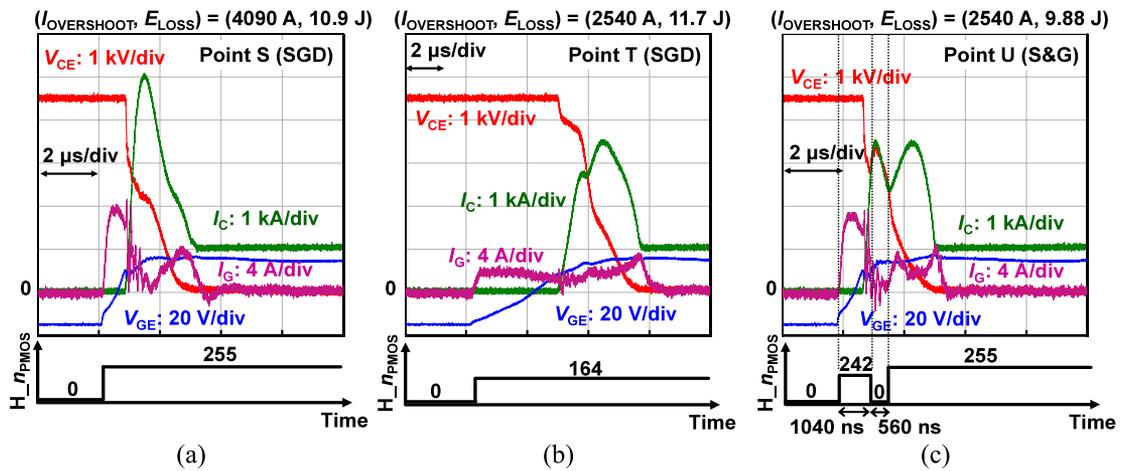


Fig. 24. Gate vectors and measured waveforms from Point S to Point U in Fig. 20 at  $V_{CC} = 4.5$  kV.

TABLE III  
 $V_{CC}$  DEPENDENCE OF OPTIMUM  $n_1$  IN S&G

$V_{CC}$	Optimum $n_1$ in S&G
3.0 kV	234
3.6 kV	237
4.0 kV	240
4.5 kV	242

TABLE IV  
 COMPARISON TABLE OF DGDs

	TIA'17 [11]	ISPSD'20 [19]	ISPSD'21 [24]	TPEL'21 [25]	This work
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	Si IGBT
Process	180 nm BCD	180 nm BCD	180 nm BCD	180 nm HV CMOS	180 nm BCD
Chip area	6.25 mm <sup>2</sup>	1.97 mm <sup>2</sup>	4.32 mm <sup>2</sup>	5.0 mm <sup>2</sup>	2.5 mm <sup>2</sup>
Output voltage swing	15 V	3.3 V	5 V	5 V	30 V
Levels of $I_G$	6 bit	7 bit	6 bit	8 bit (coarse), 6 bit (fine)	8 bit
Max. $I_G$	5 A	3.3 V / 0.5 $\Omega$ = 6.6 A	5 A	5 V / 0.12 $\Omega$ = 42 A	28 A
Functions integrated into IC	1 driver	1 driver	1 driver	1 driver	2 DACs

Table IV presents a comparison table of DGDs. The proposed DGD using HB DAC IC and two power MOSFETs achieves the largest  $V_{SWING}$  of 30 V and the second largest  $I_G$  of 28 A in DGDs. This article is the first to demonstrate the advantages of DGD in HVIGBT.

## V. CONCLUSION

This article is the first to demonstrate the advantages of AGDs in the double pulse test at the world's highest voltage (4.5 kV) and the largest load current (1000 A) using the 6500 V, 1000 A IGBT modules. To enable the active gate driving in the 6500 V, 1000 A IGBT module, a new DGD circuit technology combining HB DAC IC and two power MOSFETs is proposed to realize a DGD that can output large  $I_G$  up to 28 A with a low-cost small-area IC. The four different gate drive methods, including SGD, S&G, 2DG, and 4DG, are compared by measurements at 3.6 kV, 1000 A in terms of  $E_{LOSS}$  and  $I_{OVERSHOOT}$  reduction performance and in terms of test cost to find the optimal gate driving parameters, and S&G is selected from a cost-performance perspective.  $V_{CC}$  dependence of the  $E_{LOSS}$  reduction performance of the active gate driving, which is most important for the target 6500 V, 1000 A IGBT module, is also clarified. In  $V_{CC}$  range from 3.0 to 4.5 kV, the proposed S&G reduces  $E_{LOSS}$  by 13%–32% compared with the conventional SGD under  $I_{OVERSHOOT}$ -aligned condition. In this article, advantages of various gate drive methods in turn-ON are discussed, while the gate drive methods presented in this article are also effective in turn-OFF. The reoptimization of gate vectors in turn-OFF, however, is required because the physics of switching is different between turn-ON and turn-OFF.

Finally, the design guideline of the active gate driving for HVIGBT is clarified. Aligning the two peak heights of  $I_C$  waveforms is the design guideline for active gate driving that

minimize  $f_{OBJ}$ . The high-speed operating limit of the developed DGD, i.e., the minimum value of time slot ( $t_1-t_4$  and  $t_6-t_9$ ), is determined by the rise time and fall time of  $V_{GSH}$  and  $V_{GSL}$  in Fig. 5. The minimum value of time slot is estimated to be about 150 ns because the rise time of  $V_{GSH}$  is 110 ns and the fall time of  $V_{GSH}$  is 40 ns, as shown in the measured  $V_{GSH}$  waveform in Fig. 16(f). Therefore, this DGD with a minimum time step of 150 ns would be applicable to silicon power devices (IGBTs and power MOSFETs) but not to WBG devices (SiC and GaN) because the WBG devices require the time step of 100 ns or less. The time step, however, can be shortened by modifying the HB DAC IC output driving force to be stronger. Although this article focused on  $I_{OVERSHOOT}$  as an evaluation index of switching noise, it is also possible to reduce electromagnetic interference (EMI) with DGD. Articles [21], [38], and [39] report the measurement results of minimizing  $E_{LOSS}$  while meeting EMI regulations by optimizing gate vectors using DGD. It is possible to achieve the similar EMI countermeasures as above using the proposed DGD in this article.

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