Bond Wire Lift-off Sensor Circuit for Power Devices Integrated in Gate Driver IC

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***Abstract*-- To achieve low-cost detection of bond wire lift-off for power devices without sensor circuits made of discrete components on PCB, the world's first fully integrated bond wire lift-off sensor (BWLS) compatible with existing gate driver IC is proposed. When several bond wires in the emitter of an IGBT lift off, the increased parasitic inductance leads to a higher induced voltage, which raises the transient-state turn-on gate-to-emitter voltage (V_{GE}). The proposed BWLS detects bond wire lift-off by tracking and holding the variating transient-state turn-on V_{GE}. The BWLS is designed to automatically find the optimal capturing timing because the maximum sensitivity is achieved if the V_{GE} is held when collector current varies the most. For function verification, a gate driver IC with integrated BWLS is fabricated with 180 nm BCD process. Double pulse test results at 20 A and 80 A show that the proposed circuit successfully detects the reduction in the number of bond wires from the initial value of six to one in an IGBT module and achieves an average sensitivity of 54 mV per wire.**

***Index Terms*-- Bond wire, lift-off detection, gate-emitter voltage, track-and-hold.**

I. Introduction

In power devices, die-to-die and die-to-pin connections are built using bond wires. Therefore, the bond wire lift-off detection for power devices is an important technology to realize reliable power electronic systems [1-15]. The target of this work is to develop a bond wire lift-off sensor (BWLS) that (1) can be fully integrated into a gate driver IC without external components for low cost and low area consumption, and (2) does not require the power device to be under special voltage or current conditions for bond wire lift-off sensing. Table I shows a summary of previous works. Methods for detecting bond wire lift-off from on-state voltage drop [11], bond wire parasitic inductance [12], collector-emitter resistance [13], short circuit current [14], and reverse body diode voltage drop [15] have been proposed. However, collector current (I_C) measurement requires a current sensor, and collector-emitter voltage (V_{CE}) measurement requires a high-voltage diode, which are not suitable for integration into ICs. In addition, [11, 14, 15] require special voltage or current conditions, such as auxiliary power supplies, for bond wire lift-off sensing, which is a problem because it can interfere with the original operation of the power converters. Since there is no existing study that has achieved the above targets, the BWLS that fulfills both targets is proposed in this paper.

TABLE I. Comparison Table of Bond Wire Lift-off Detection Methods

Reference	[11]	[12]	[13]	[14]	[15]	This work
Target power device	IGBT	IGBT	IGBT	IGBT	SiC MOSFET	IGBT
Physical quantity that changes	R_{WIRE}	L_{WIRE}	R_{WIRE}	R_{WIRE}	R_{WIRE}	L_{WIRE}
Measured value	$V_{CE(ON)}$, V_F	V_{GE}	$V_{CE(ON)}$, I_C, V_{TH}	I_{SC}	V_{SD}	V_{GE}, V_{eE}
Special voltage or current conditions	YES	NO	NO	YES	YES	NO
Implementation	Discrete	Discrete	Discrete	Discrete	Discrete	Fully integrated
Sensitivity	53 mV/wire	2.8 mV/wire	0.32 mΩ/wire	0.38 A/wire	3.5 mV/wire	54 mV/wire

II. Proposed Fully Integrated Bond Wire Lift-off Sensor

In this paper, the lift-off of bond wires from the IGBT's emitter is discussed. Fig. 1 shows a simplified schematic illustration of the bond wire lift-off detection. When bond wire lifts off from metal pad, the gate-to-emitter voltage (V_{GE}) waveform varies accordingly due to the parasitic signal path between gate and emitter. Therefore, it is possible to design a circuit that senses the V_{GE} variation and then detects bond wire lift-off. Fig. 2 shows the overall schematic of the proposed IC with integrated BWLS. A gate driver (GD) is included for driving the IGBT module and the BWLS senses the voltage difference (V_{GSS}) between gate terminal of IGBT and IC ground, which is 15 V higher than V_{GE}, and outputs a voltage signal (Sensor_out) that is related to the number of lifted off bond wire. Since V_{GSS} rises rapidly during turn-on, a circuit that tracks and holds V_{GSS} is needed. The track-and-hold circuit should track V_{GSS} when a turn-on signal arrives and hold the sensor output at the moment that V_{GSS} varies the most due to bond wire lift-off.

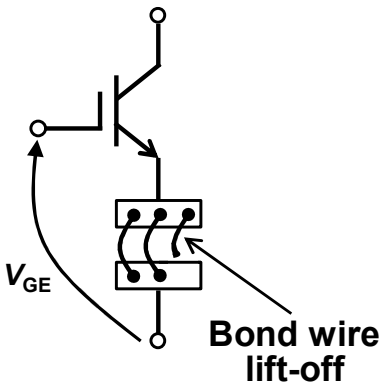

Fig. 1. Schematic illustration of bond wire lift-off.

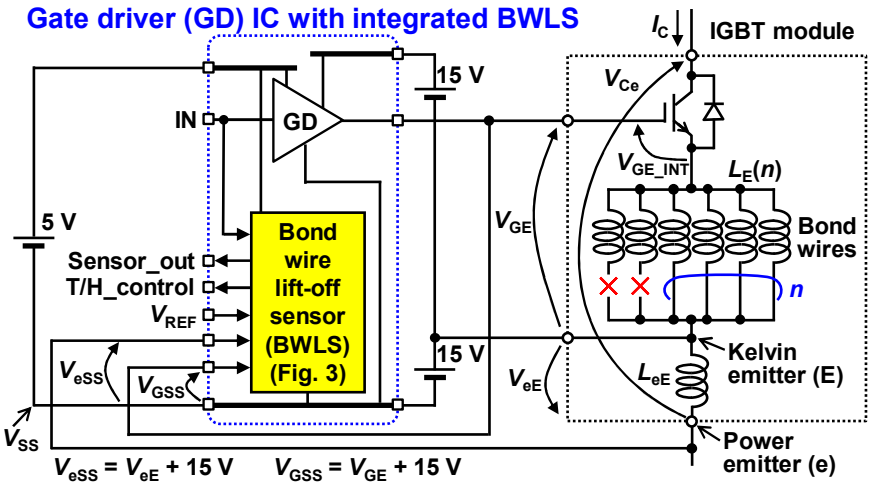

Fig. 2. Overall schematic of gate driver IC with integrated BWLS.

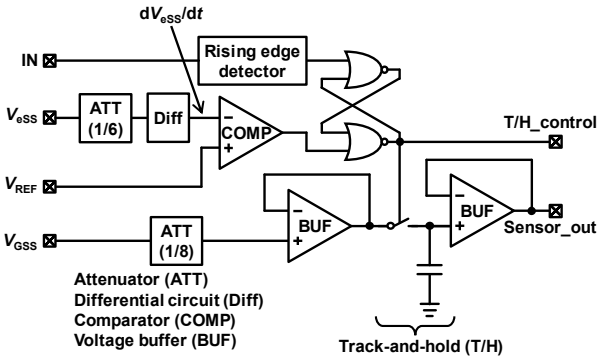

Fig. 3. Circuit schematic of proposed BWLS.

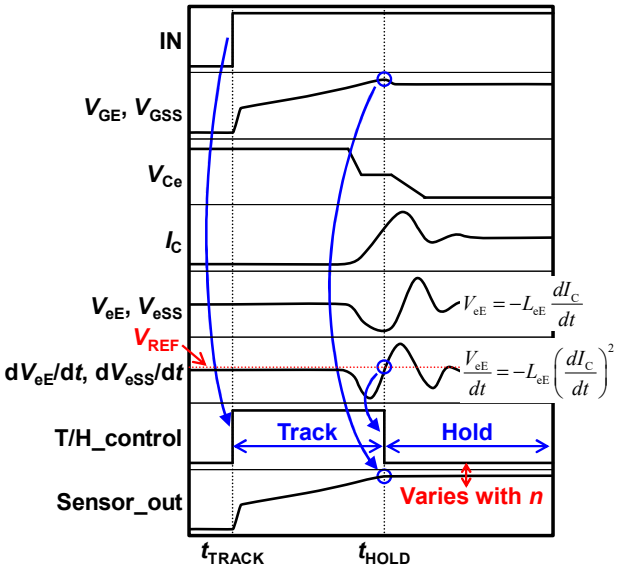

Fig. 4. Timing chart of proposed BWLS.

Figs. 3 and 4 show the detailed circuit schematic and timing chart of the proposed BWLS, respectively. The principle of operation of BWLS is explained below.

Eq. (1) describes the relationship between the V_{GSS} and the number of remaining bond wires (n).

$$V_{GSS} = V_{GE\_INT} + L_E(n)\frac{dI_C}{dt} + 15, \qquad (1)$$

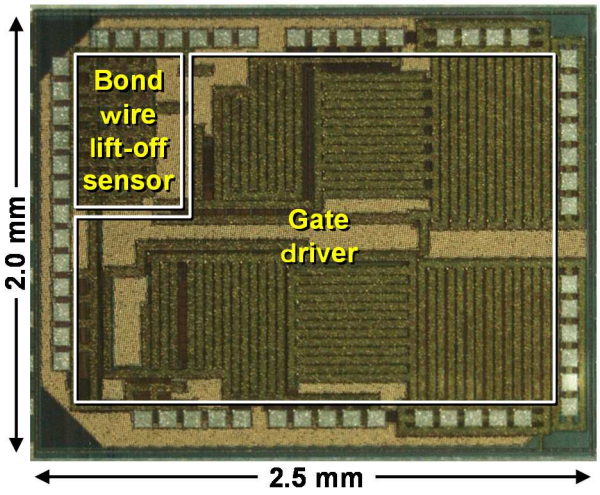

Fig. 5. Gate driver IC with integrated BWLS.

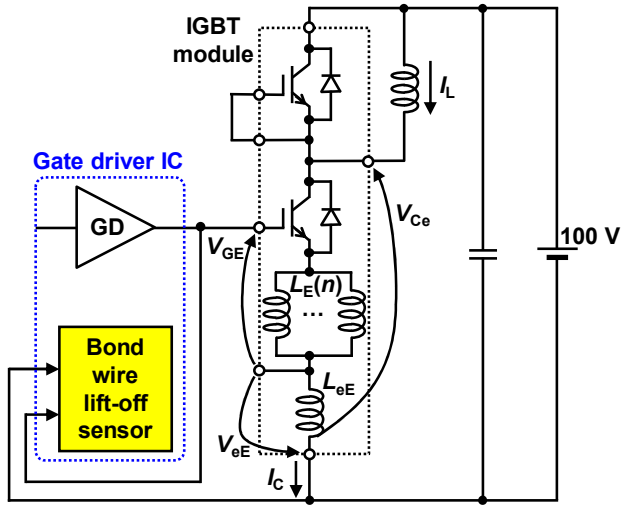

Fig. 6. Circuit schematic of double pulse test.

where V_{GE_INT} is the internal gate-emitter voltage, which is not measurable, $L_E(n)$ is the parasitic inductance of bond wires, which is a function of the remaining bond wires' number n, and t is the time variable. A 15 V is added because BWLS senses voltage between IGBT's gate terminal and IC ground.

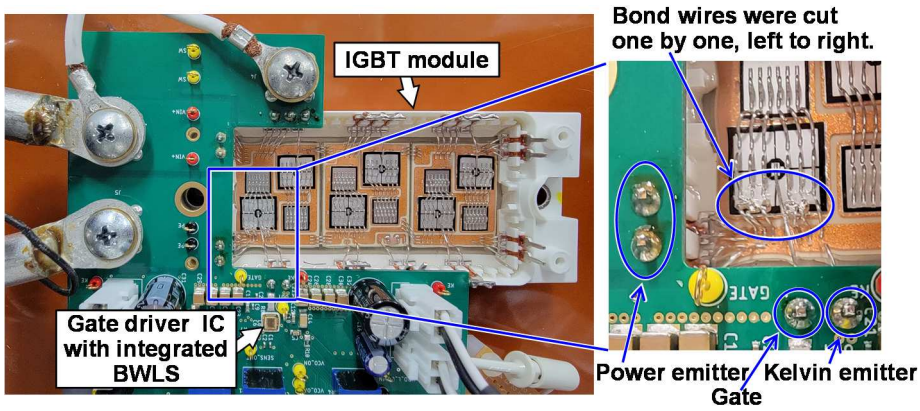

Fig. 7. Measurement setup.

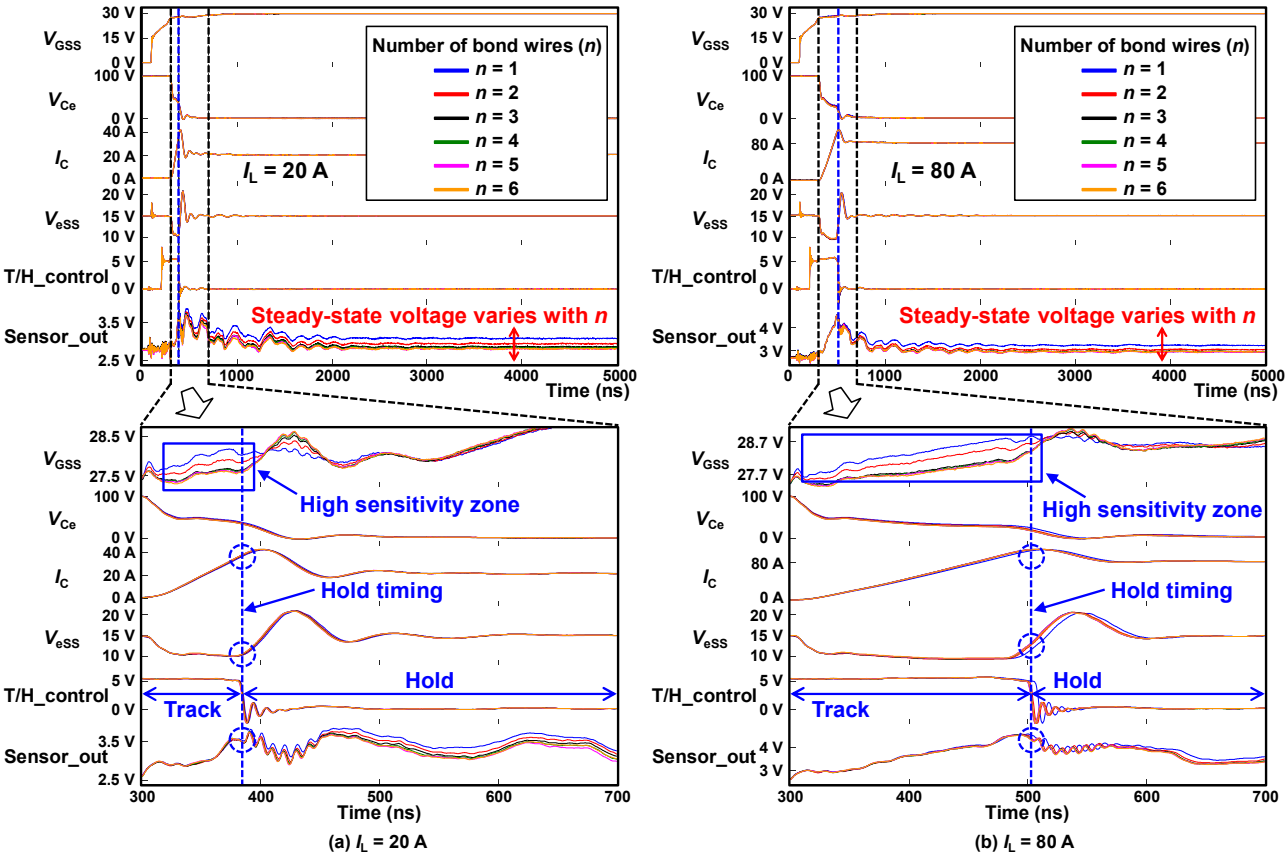

Fig. 8. Measured turn-on waveforms of BWLS with varied n from 6 to 1.

BWLS holds the transient-state turn-on V_{GSS} that varies with the change of $L_E(n)$, then n can be estimated from the variation of the steady-state track-and-hold output named Sensor_out. According to Eq. (1), the BWLS is designed to hold V_{GSS} when dI_C/dt is maximum for the theoretically best sensitivity.

V_{eE} is the voltage difference between Power emitter and Kelvin emitter and V_{eSS} is that between Power emitter and IC ground. Instead of V_{eE}, the proposed circuit takes V_{eSS} as a trigger for holding output, as shown in Figs. 3 and 4. According to the equations in Fig. 4, the moment when dI_C/dt achieves maximum is the same as that when $dV_{eSS}/dt = 0$, which is detected by a comparator. Then the falling edge of T/H_control signal is triggered, and the attenuated V_{GSS} is held. The proposed circuit is compatible with most of the gate driver IC. In this work, the proposed circuit is combined with our previous work [16]. For function verification, a gate driver IC integrated BWLS is fabricated with 180-nm BCD process, and the die photo is shown in Fig. 5. The die size is 2.0 mm by 2.5 mm.

III. Measured Results

Fig.6 shows the circuit schematic of the double pulse test measurement setup. The voltage supply of the power loop is 100 V. Fig. 7 shows the photo of the measurement setup. An IGBT module (FS100R12N2T4P, 1200 V, 100 A) is selected as the test object and is mounted on a specially designed PCB. The internal structure of the IGBT is exposed for easier handling. The load current (I_L) is measured by the Rogowski coil.

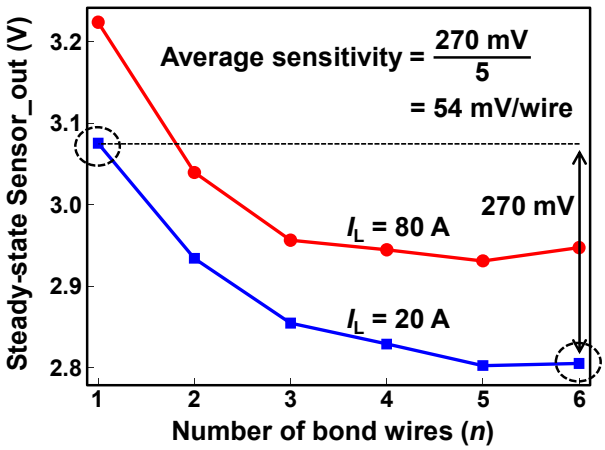

Fig. 9. Measured n dependence of steady-state Sensor_out.

To demonstrate the functionality, BWLS is measured in double pulse test with the I_L of 20 A and 80 A. The initial value of n is 6, and n is changed by manually cutting off the bond wires one by one to emulate the gradual bond wire lift-off failure.

Fig. 8 (a) and (b) shows the measured turn-on waveforms of BWLS with varied n from 6 to 1 at I_L = 20 A and 80 A, respectively. The gate driver uses 15 V for turning on and -15 V for turning off the IGBT module and the proposed circuit senses the V_{GSS} between gate of IGBT and IC ground, which is 15 V higher than V_{GE}. The V_{GSS} waveforms almost overlap together except for the I_C rising phase, which verifies that the induced voltage across the parasitic inductance $L_E(n)$ appears on the V_{GSS}. When zooming in the time scale and vertical scale of V_{GSS}, the n dependence of V_{GSS} is clearly observed in the area named high sensitivity zone, where I_C is rising. The blue V_{GSS} curve, for example, shows the V_{GSS} waveform when there is only one bond wire left (n = 1).

Although BWLS output varies during turn-on phase because of the transient noise and interference, the steady state Sensor_out clearly shows the waveform dependency on n, which tells that the BWLS achieves the goal of bond wire detection in a single IC. Comparing the measured V_{GSS} waveforms at I_L = 20 A and 80 A, it can be seen that I_L takes more time to climb to 80 A. Except for the extension of high sensitivity zone, the circuit's operation is the same for both I_L = 20 A and 80 A.

Obviously, as predicted by Eq. (1), the high sensitivity zone is observed where dI_C/dt is approaching maximum value and V_{eSS} is close to the minimum value at I_L = 20 A and I_L = 80 A. The BWLS is designed to achieve high sensitivity by detecting the maximum dI_C/dt, which is theoretically the optimal timing for holding V_{GSS}. As shown in Figs. 3 and 4, the BWLS takes V_{eSS} as input, and then obtains dV_{eE}/dt (equal to dV_{eSS}/dt), which corresponds to I_C's second derivative with respect to time, from the attenuated V_{eSS}. Then the maximum dI_C/dt is detected according to the zero-crossing point of dV_{eE}/dt. The falling edge of T/H_control is triggered and indicates the hold timing, which is depicted as a blue dashed line in Fig. 8 (a) and (b).

Although the noisy transient-state Sensor_out occurs immediately after the output holding, n can be estimated from the steady-state Sensor_out. Fig. 9 shows the measured n dependence of steady-state Sensor_out at I_L = 20 A and 80 A. Sensor_out increases when n decreases, and the voltage swing of Sensor_out for both I_L conditions is almost the same. With larger I_L, Sensor_out tends to be higher. Therefore, n can be estimated more efficiently from Sensor_out by recording the initial value with n of six and comparing the measured Sensor_out with the initial record.

Because of the parallel nature of inductors, the total inductance does not change much when the first few bonding wires are cut off. Therefore, the Sensor_out changes slightly, even the measurement error and noise could be larger than the voltage difference of Sensor_out. In this paper, the ratio between the swing of Sensor_out (270 mV) and the number of cut-off bond wires (n = 5) is defined as the average sensitivity (54 mV/wire) of the bond wire lift-off detection method. Table I shows the comparison of existing bond wire lift-off detection methods. This work is the first one that achieves the fully integrated bond wire lift-off detection in a single IC that does not require discrete components and special voltage or current conditions for bond wire lift-off sensing.

IV. Conclusions

The fully integrated BWLS, which can detect bond wire lift-off from the V_{GSS} waveform and does not require special voltage or current conditions, is proposed. The functionality of BWLS is shown by the double pulse test with the voltage of 100 V and the current of I_L = 20 A and 80 A. To increase the sensitivity of BWLS, the turn-on V_{GSS} waveform is tracked and automatically captured when V_{eSS} is minimum, concurrently with dI_C/dt reaching its maximum value. The captured V_{GSS} is a DC signal, which is convenient for read-out.

Acknowledgment

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