Natural Active Gate Driving for Breaking Trade-off Between Switching Loss and Current Overshoot Using Ordinary Gate Driver

Yaogan Liang
The University of Tokyo
Tokyo, Japan

Haoxi Zhou
The University of Tokyo
Tokyo, Japan

Dibo Zhang
The University of Tokyo
Tokyo, Japan

Katsuhiro Hata
The University of Tokyo
Now with Shibaura Institute of Technology
Tokyo, Japan

Makoto Takamiya
The University of Tokyo
Tokyo, Japan
mtaka@iis.u-tokyo.ac.jp

***Abstract*— Natural active gate driving (NAGD) using an ordinary gate driver is proposed to reduce both loss and noise during switching transients of power devices. In NAGD, in a 4-pin IGBT or SiC MOSFET, the ground pin of an ordinary gate driver is connected to the power emitter (PE) in IGBT or power source (PS) in SiC MOSFET instead of the Kelvin emitter (KE) or Kelvin source (KS). Active gate driving is naturally achieved because the internal gate-to-emitter or gate-to-source voltage temporarily drops during power device turn-on due to an induced voltage caused by the parasitic inductance between the KE and PE in IGBT or the KS and PS in SiC MOSFET. The 600 V double pulse tests are conducted using IGBT module at load current (I_L) of 20 A, 50 A, and 80 A, and using SiC module at I_L of 70 A. The switching loss (E_{LOSS}) and collector or drain current overshoot ($I_{OVERSHOOT}$) of the conventional gate driving (CGD) and the proposed NAGD are compared, and the results is shown on tradeoff curves. In measurement of IGBT module, where I_L equals 80 A, compared with the CGD, the proposed NAGD reduces E_{LOSS} by 49 % under $I_{OVERSHOOT}$-aligned condition and $I_{OVERSHOOT}$ by 33 % under E_{LOSS}-aligned condition. In measurement of SiC module, the NAGD achieves a 26 % reduction in E_{LOSS} and a 25 % reduction in $I_{OVERSHOOT}$ under conditions align with $I_{OVERSHOOT}$ and E_{LOSS}.**

Keywords—switching loss, current overshoot, emitter and source inductance, active gate driving, trade-off curve

I. Introduction

Active gate driving (AGD), which changes the gate driving strength multiple times in fine time slots during the switching period of power devices, is attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching. AGD, however, is not yet widely used, because it requires a complex and special active gate driver, which is expensive to implement. Specifically, to control the gate waveform for AGD, open-loop active gate drivers [1-2] require many input pins, while closed-loop active gate drivers [3-8] require sensors and controllers. To solve the problem, in this paper, natural active gate driving (NAGD) is proposed to realize AGD using an ordinary gate driver. With the parasitic emitter inductance in IGBT or source inductance in SiC MOSFET, negative feedback is achieved naturally because of emitter or source degeneration when the load current (I_L) goes through power devices. Therefore, the control circuits are not required.

II. Proposed Natural Active Gate Driving (NAGD)

Figs. 1 and 2 show circuit schematics of the conventional gate driving (CGD) and the proposed NAGD when using IGBT and SiC MOSFET, respectively. In a 4-pin power device, the ground pin of an ordinary gate driver is connected to the Kelvin emitter (KE) or Kelvin source (KS) in CGD,

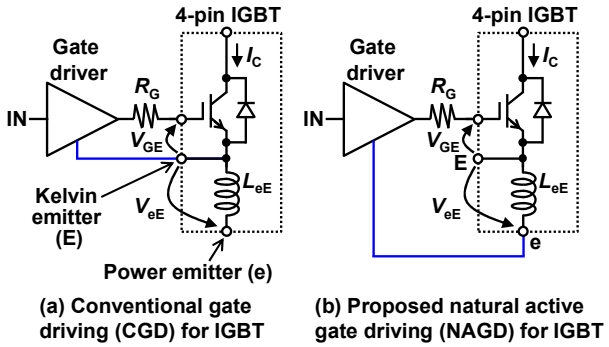

Fig. 1. Schematic of CGD and NAGD for IGBT.

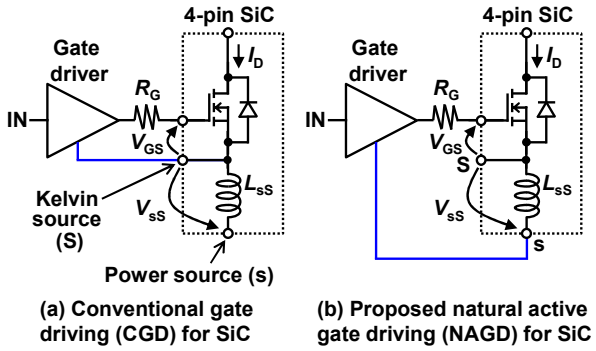

Fig. 2. Schematic of CGD and NAGD for SiC.

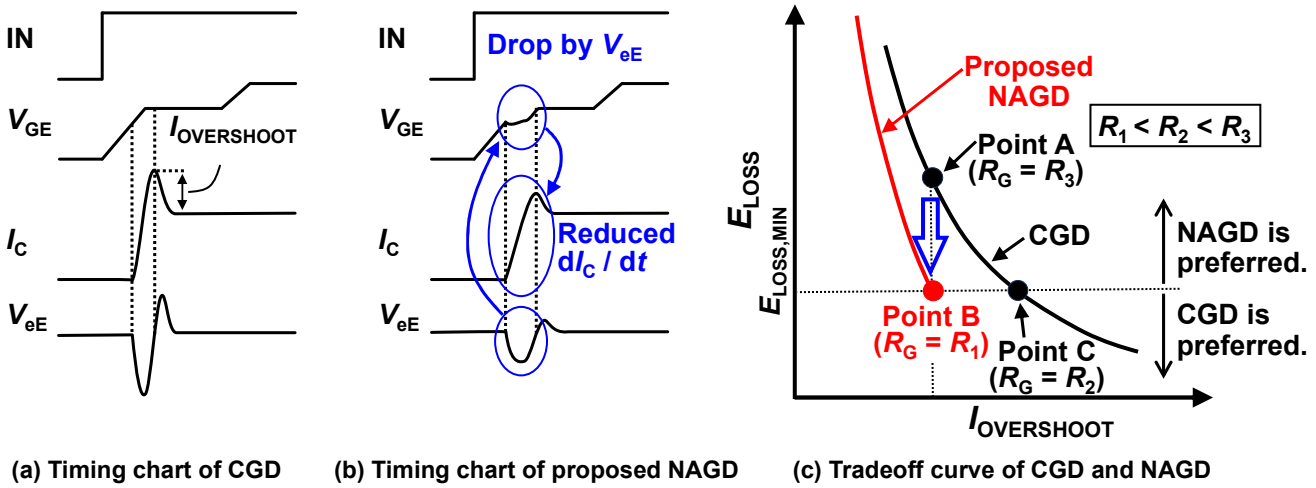

Fig. 3. Timing charts and tradeoff curve of CGD and NAGD. (a) Timing chart of CGD. (b) Timing chart of NAGD. (c) E_{LOSS} and $I_{OVERSHOOT}$ trade-off curves for CGD and NAGD at turn-on, where R_G is varied.

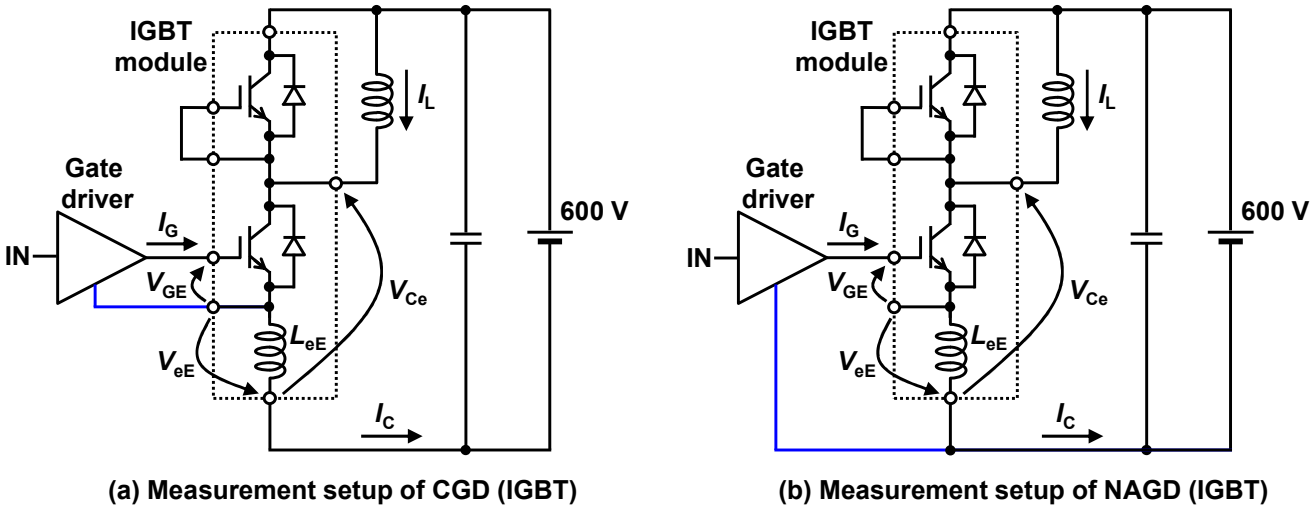

Fig. 4. Circuit schematics of double-pulse test using IGBT module. (a) CGD. (b) NAGD

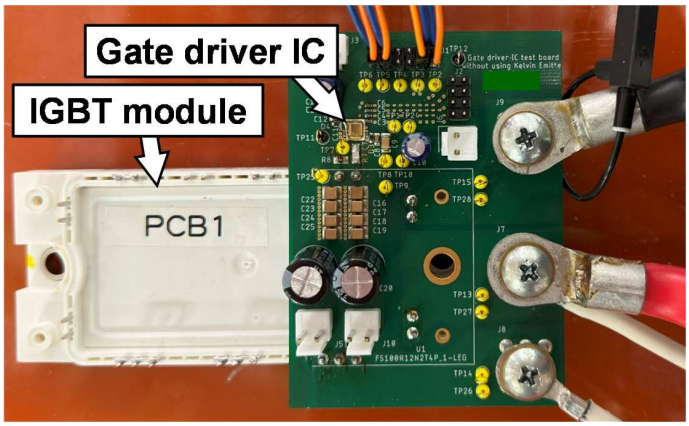

Fig. 5. Measurement setup of IGBT module.

while it is connected to the power emitter (PE) or power source (PS) in NAGD. Figs. 1 (a), (b) and Figs. 2 (a), (b) can be said to be the comparisons between 4-pin and a 3-pin power device, since the connection of NAGD is the same as for a 3-pin IGBT or SiC MOSFET without the KE or KS. Since the mechanism of NAGD is the same in IGBT and SiC

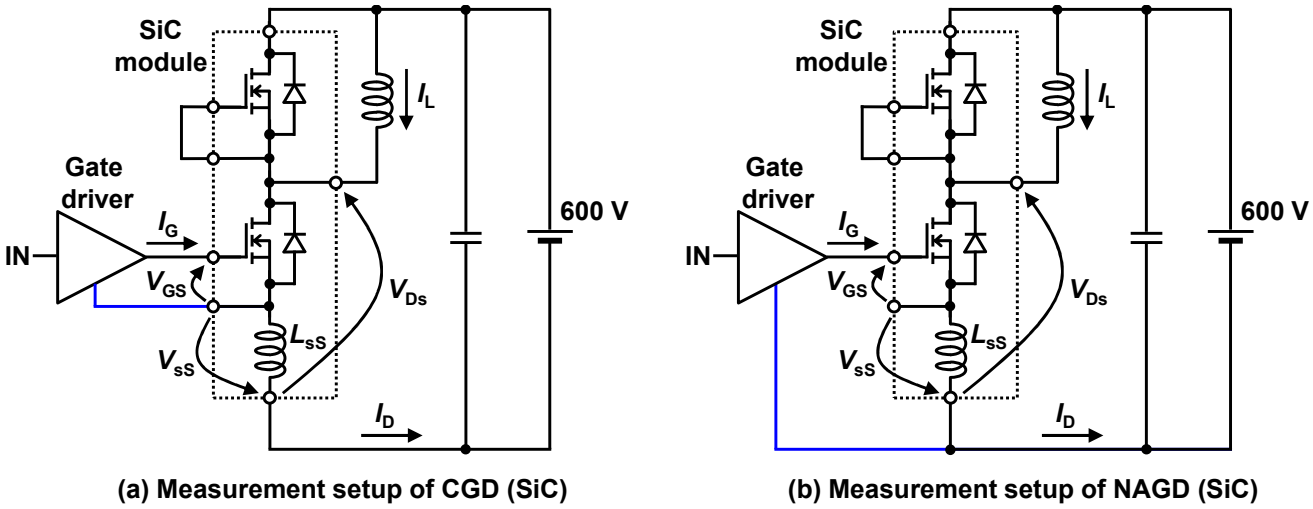

Fig. 6. Circuit schematics of double-pulse test using SiC module. (a) CGD. (b) NAGD.

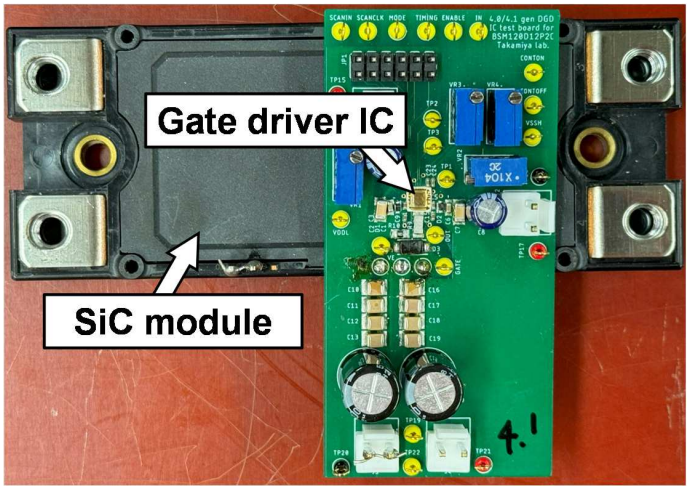

Fig. 7. Measurement setup of SiC module.

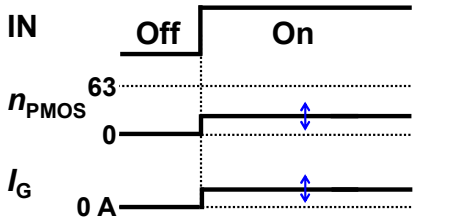

Fig. 8. Timing chart at turn-on.

MOSFET, for simplicity, Figs. 3 (a) and (b) only show the timing charts of CGD and NAGD at turn-on of IGBT. When the IGBT or SiC MOSFET turns on and the collector current (I_C) or drain current (I_D) changes, transient voltage between the KE and the PE (V_{eE}) or voltage between KS and PS (V_{sS}) is induced as shown in Eq. (1) and (2).

$$V_{eE} = -L_{eE}\frac{dI_C}{dt} \quad (1)$$

$$V_{sS} = -L_{sS}\frac{dI_D}{dt} \quad (2)$$

where L_{eE} and L_{sS} is the parasitic inductance between the KE and the PE in IGBT, KS and PS in SiC MOSFET, and t is time. In CGD in Fig. 1 (a), Fig. 2 (a) and Fig. 3 (a), V_{eE} and V_{sS} are outside the gate loop, making the gate-to-emitter voltage (V_{GE}) and gate-to-source voltage (V_{GS}) unaffected by V_{eE} and V_{sS} changes, while in NAGD in Fig. 1 (b), Fig. 2 (b) and Fig. 3 (b), V_{eE} and V_{sS} is inside the gate loop, making the V_{GE} and V_{GS} affected by V_{eE} and V_{sS} changes [9-11]. In NAGD in Fig. 3 (b), AGD is naturally achieved by negative feedback effect of L_{eE}, because V_{GE} transiently drops during the period of increasing I_C due to the transient increase in $|V_{eE}|$, resulting in a decrease in dI_C / dt, an increase in the switching loss (E_{LOSS}), and a decrease in the collector current overshoot ($I_{OVERSHOOT}$, same for drain current overshoot) [9-

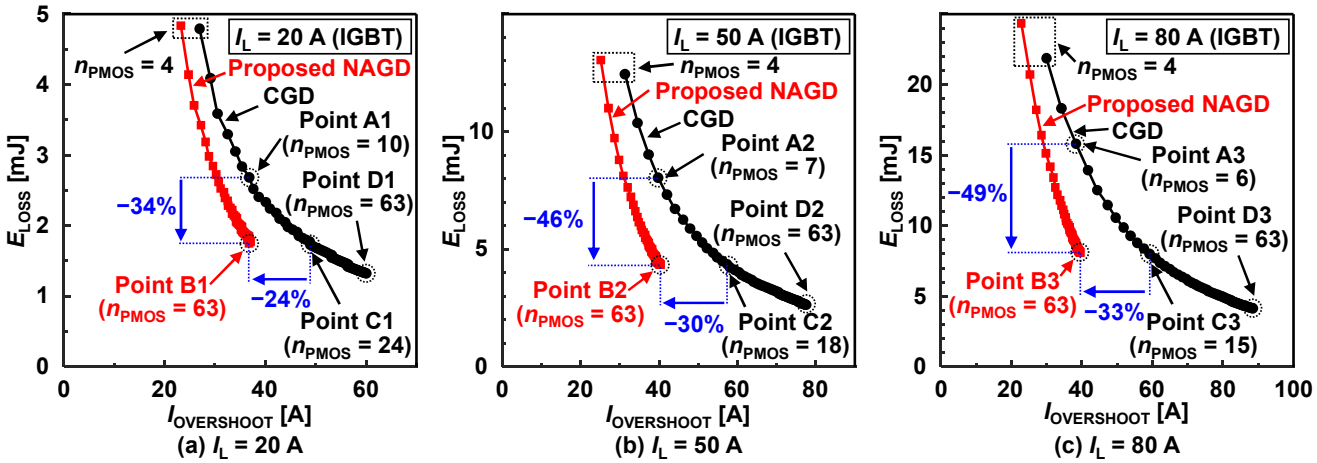

Fig. 9. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of CGD and NAGD using IGBT module.

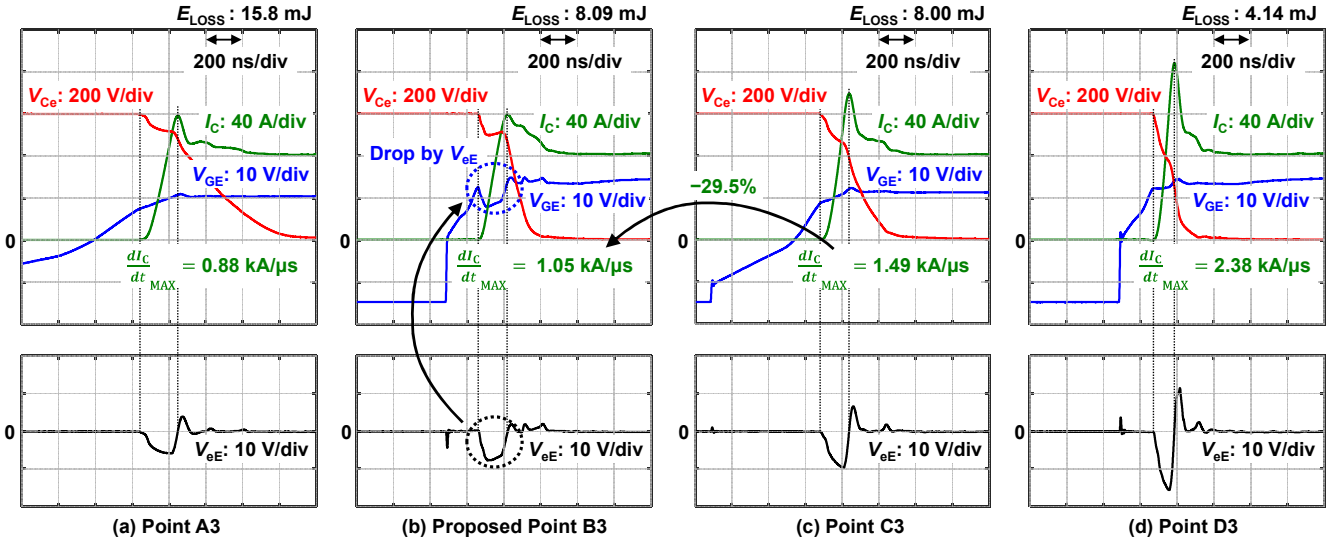

Fig. 10. Measured waveforms of Points A3 to D3 in Fig. 9 (c).

12], compared to CGD. The V_{GE} waveform of NAGD is very similar to that of the previously proposed stop-and-go AGD [5, 13], which reduces driving current in the rising phase of I_C. Fig. 3 (c) shows a schematic of the E_{LOSS} and $I_{OVERSHOOT}$ trade-off curves for CGD and NAGD at turn-on, where the gate resistance (R_G) in Figs. 1 and 2 is varied. In this paper, it is clarified for the first time in the world that the trade-off curve of NAGD is on the lower left side compared to the trade-off curve of CGD. For example, Point B (NAGD, $R_G = R_1$) has reduced $I_{OVERSHOOT}$ at the same E_{LOSS} compared to Point C (CGD, $R_G = R_2$, $R_1 < R_2$). On the other hand, Point B (NAGD, $R_G = R_1$) reduces E_{LOSS} compared to Point A (CGD, $R_G = R_3$, $R_1 < R_3$) under $I_{OVERSHOOT}$-aligned conditions. The following explains how to choose CGD and NAGD depending on the situation. $E_{LOSS,MIN}$ is defined as the minimum value of E_{LOSS} that can be realized by NAGD. When the required E_{LOSS} is smaller than $E_{LOSS,MIN}$, CGD should be used, tolerating large $I_{OVERSHOOT}$. In contrast, when the required E_{LOSS} is larger than $E_{LOSS,MIN}$, NAGD with smaller $I_{OVERSHOOT}$ than CGD should be used.

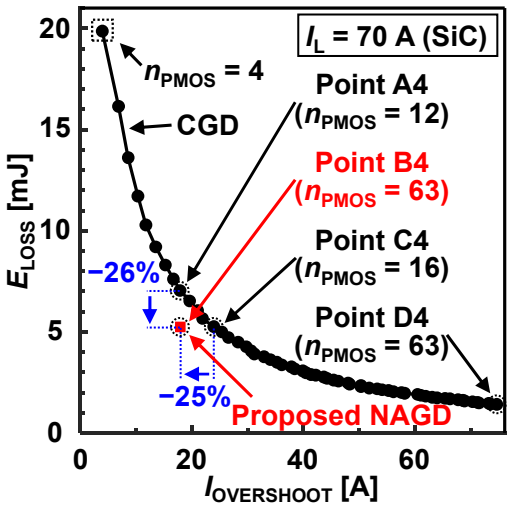

Fig. 11. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of CGD and NAGD using SiC module.

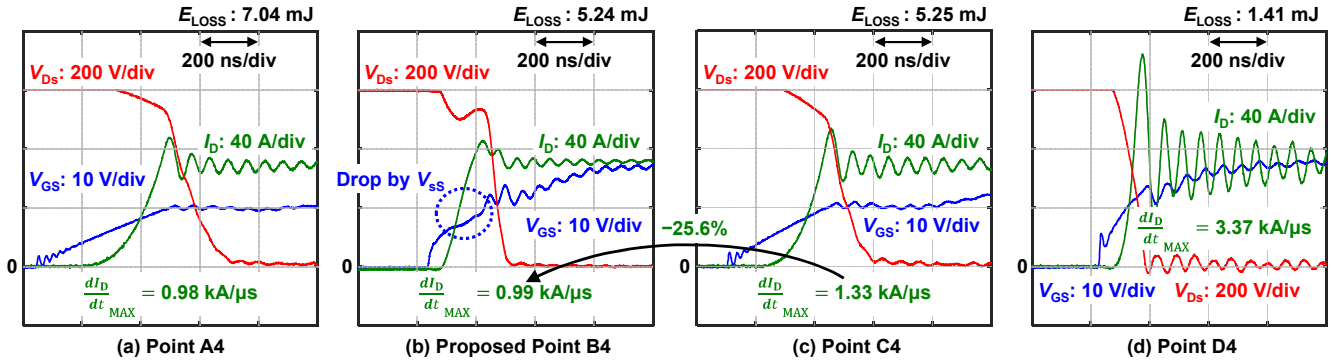

Fig. 12. Measured waveforms of Points A4 to D4 in Fig. 11.

III. Measured Results

Figs. 4 (a) and (b) show the circuit schematics of the double pulse test at 600 V for CGD and NAGD using IGBT module, respectively, where R_G = 0 Ω. Fig. 5 shows the measurement setup with an IGBT module (FS100R12N2T4P, 1200 V, 100 A rating). To minimize any unwanted effect, two highly similar gate driver PCBs, for CGD and NAGD, are fabricated, and Fig. 5 only shows the latter. The double pulse test schematic for CGD and NAGD using SiC module (BSM180D12P2C101, 1200 V, 204 A rating) is shown in Figs. 6 (a) and (b). Fig. 7 only shows the NAGD measurement setup of SiC module for simplicity. Fig. 8 shows a timing chart at turn-on. To efficiently perform the trade-off curve measurements in Fig. 3 (c) without the need to change R_G, the gate current (I_G) of a current-source type 6-bit digital gate driver IC [5] is varied by digital control, where n_{PMOS} is a parameter that determines I_G as shown in Fig. 8.

A. IGBT module

Figs. 9 (a) to (c) show the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of CGD and NAGD using IGBT module at the I_L of 20 A, 50 A, and 80 A, respectively. The black and red curves show the trade-off curves for CGD and NAGD, respectively, with varied n_{PMOS} from 4 to 63. Fig. 9 clearly shows that the trade-off curve of NAGD is on the lower left side compared to the trade-off curve of CGD. Points A1 to A3, Points B1 to B3, Point C1 to C3 and Points D1 to D3 are defined for I_L = 20 A, 50 A, and 80 A, respectively, where Points "B"s are the proposed NAGD, Point "A"s are CGD with closest $I_{OVERSHOOT}$ comparing to Points "B"s, and Point "C"s are CGD with the closest E_{LOSS} comparing to Points "B"s. Comparing Point "A"s and Point "B"s, the proposed NAGD reduces E_{LOSS} by 34 %, 46 %, and 49 % under $I_{OVERSHOOT}$-aligned condition at I_L = 20 A, 50 A, and 80 A, respectively. Comparing Point "C"s and Point "B"s, the proposed NAGD reduces $I_{OVERSHOOT}$ by 24 %, 30 %, and 33 % under E_{LOSS}-aligned condition at I_L = 20 A, 50 A, and 80 A, respectively. Figs. 10 (a) to (d) show the measured waveforms of Points A3 to D3 in Fig. 9 (c), respectively. In the proposed Point B3 in Fig. 10 (b), the transient V_{GE} drop during the period of increasing I_C is clearly observed, which is the evidence of NAGD. Comparing E_{LOSS}-aligned Points B3 and C3, NAGD reduced $I_{OVERSHOOT}$ by 33 % from 59 A to 40 A and the maximum dI_C / dt by 29.5 % from 1.49 kA / μs to 1.05 kA / μs. In Fig. 9, with maximum I_G, CGD achieves fast switching but with larger $I_{OVERSHOOT}$, which can cause damage to power device, as shown in Point "D"s. On the other hand, because the negative feedback from emitter inductance becomes greater as dI_C / dt increase, although Point "B"s and "D"s have the same driving strength, the dI_C / dt of NAGD is lower than CGD, resulting in high E_{LOSS} and slow switching, as shown in Fig. 9. Therefore, CGD can be chosen when the allowable E_{LOSS} is smaller than $E_{LOSS,MIN}$, and NAGD is preferred when low $I_{OVERSHOOT}$ is necessary, as shown and discussed in Fig. 3 (c).

B. SiC module

Fig. 11 shows the measured trade-off curve in double-pulse test at 600 V and 70 A using SiC module. Similar to the IGBT measurements, the I_G is varied by digitally sweeping n_{PMOS} from 4 to 63. Points A4 to D4 are defined. The NAGD with maximum I_G (Point B4) is located in the lower left side of the CGD trade-off curve, which achieves a 26 % reduction in E_{LOSS}, comparing to Point A4, under $I_{OVERSHOOT}$-aligned condition and a 25 % reduction in $I_{OVERSHOOT}$, comparing to Point C4, under E_{LOSS}-aligned condition. Figs. 12 (a) to (d) show the measured waveforms of Points A4 to D4 in Fig. 11, respectively. In Fig. 12 (b), similar to V_{GE} in IGBT, the V_{GS} is reduced due to the induced V_{SS} when I_D is ramping up. Compared to Point A4 and Point C4, I_D of Point B4 has a faster rising edge when I_D is zero, therefore the turn-on delay is smaller. The dI_D / dt is then automatically reduced when I_D is close to I_L of 70 A by NAGD. In contrast, driven by KS, the slope of I_D become steeper when the gate is further charged in Point A4 and C4, leading to a larger $I_{OVERSHOOT}$. As a result, the maximum dI_D / dt is reduced by 25.6 % from 1.33 kA / μs to 0.99 kA / μs, comparing Point C4 to Point B4. In Fig. 12 (d), driven by maximum I_G, ringing occurs on the waveforms of I_D and V_{DS}, which is harmful to power modules. Instead, in Fig. 12 (b), the ringing is suppressed better than Point A4 with less E_{LOSS} and turn-on delay. Therefore, it is possible to address ringing issue by simply changing the gate drive loop from CGD to NAGD.

IV. Conclusions

NAGD is proposed to realize AGD using an ordinary gate driver instead of a complex and special active gate driver. In

the double pulse tests using IGBT module at 600 V, 80 A, compared with CGD, the proposed NAGD reduces E_{LOSS} by 49 % under $I_{OVERSHOOT}$-aligned condition. Besides, 33 % reduction in $I_{OVERSHOOT}$, and 29.5 % reduction in maximum dI_C / dt is achieved under E_{LOSS}-aligned condition. NAGD also works in the double pulse tests of SiC module at 600 V, 70 A. The E_{LOSS} and $I_{OVERSHOOT}$ is reduced by 26 % and 25 % under $I_{OVERSHOOT}$-aligned and E_{LOSS}-aligned condition. The maximum dI_D / dt is reduced by 25.6 %.

ACKNOWLEDGMENT

This work was partly supported by NEDO (JPNP21009).

REFERENCES

[1] D. Liu, H. C. P. Dymond, S. J. Hollis, J. Wang, N. McNeill, D. Pamunuwa, and B. H. Stark, "Full custom design of an arbitrary waveform gate driver with 10-GHz waypoint rates for GaN FETs," *IEEE Trans. on Power Electron.*, vol. 36, no. 7, pp. 8267-8279, July 2021.

[2] W. J. Zhang, J. Yu, W. T. Cui, Y. Leng, J. Liang, Y.-T. Hsieh, H.-H. Tsai, Y.-Z. Juang, W.-K. Yeh, and W. T. Ng, "A smart gate driver IC for GaN power HEMTs with dynamic ringing suppression," *IEEE Trans. on Power Electron.*, vol. 36, no. 12, pp. 14119-14132, Dec. 2021.

[3] S. Kawai, T. Ueno, and K. Onizuka, "A 4.5V/ns active slew-rate-controlling gate driver with robust discrete-time feedback technique for 600V superjunction MOSFETs," *in Proc. IEEE International Solid-State Circuits Conf.*, Feb. 2019, pp. 252-254.

[4] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. on Power Electron.*, vol. 36, no. 2, pp. 1491-1505, Feb. 2021.

[5] D. Zhang, K. Horii, K. Hata, and M. Takamiya, "Digital gate driver IC with real-time gate current change by sensing drain current to cope with operating condition variations of SiC MOSFET," *in Proc. IEEE Int. Conf. on Power Electronics and ECCE Asia*, May 2023, pp. 374-380.

[6] R. Wang, L. Liang, Y.Chen, Y. Pan, J. Li, L. Han and G. Tan, "Self-adaptive active gate driver for IGBT switching performance optimization based on status monitoring," *IEEE Trans. on Power Electron.*, vol. 35, no. 6, pp. 6362-6372, Jun. 2020.

[7] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," *IEEE Trans. on Power Electron.*, vol. 30, no. 6, pp. 3402-3417, Jun. 2015.

[8] S. Zhao, A. Dearien, Y. Wu, C. Farnell, A. U. Rashid, F. Luo and H. A. Mantooth, "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Trans. on Power Electron.*, vol. 35, no. 2, pp. 1882-1898, Feb. 2020.

[9] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," *in Proc. Int. Power Electronics Conf. and ECCE Asia*, Jun. 2010, pp. 164-169.

[10] Y. Li, Y. Zhang, Y. Gao, S. Du and J. Liu, "Switching characteristic analysis and application assessment of SiC MOSFET with common source inductance and kelvin source connection," *IEEE Trans. on Power Electron.*, vol. 37, no. 7, pp. 7941-7951, Jul. 2022.

[11] M. Mandal, S. K. Roy and K. Basu, "Analytical switching transient model of TO-247-4 packaged SiC MOSFETs and comparison with TO-247-3 devices," *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2022, pp. 1-8.

[12] P. Xue and P. Davari, "The trade-off of switching losses and EMI generation for SiC MOSFET with common source and Kelvin source configurations," *in Proc. European Conf. on Power Electronics and Applications*, Sep. 2023, pp. 1-8.

[13] T. Sai, K. Miyazaki, H. Obara, T. Mannen, K. Wada, I. Omura, T. Sakurai, and M. Takamiya, "Stop-and-go gate drive minimizing test cost to find optimum gate driving vectors in digital gate drivers," *in Proc. IEEE Applied Power Electronics Conf. and Expo.*, Mar. 2020, pp. 3096-3101.