Method for Determining Optimum Time in Time-Domain Stop-and-Go Active Gate Driving

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***Abstract*— A method for determining the optimum time in time-domain stop-and-go active gate driving (TD AGD), which changes the gate driving strength three times from "strong to high-Z to strong", is proposed. In the double pulse tests of IGBT at 600 V, compared with the conventional gate driving, the proposed TD AGD reduces the switching loss by 25% and 18% at load currents of 50 A and 100 A, respectively, under collector current overshoot-aligned conditions.**

Keywords*— *active gate driving, switching loss, current overshoot, time domain

I. INTRODUCTION

Active gate driving (AGD), which changes the gate driving strength multiple times in fine time slots during the switching period of power devices, is attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching. A time-domain stop-and-go active gate driving (TD AGD) [1-16] is an AGD that changes the gate driving strength three times from "strong to high-Z to strong" or "strong to weak to strong", and in this paper, the time for the first and next drives are defined as t_1 and t_2, respectively. TD AGD can cope with variations in operating conditions such as load current (I_L) and junction temperature by adaptively changing t_1 and t_2 [1-16]. As shown in Fig. 1, where V_{GE} is the gate-to-emitter voltage and I_C is the collector current of IGBTs, various t_1 and t_2 decision methods have been proposed, however, it is not clear which decision method is the best to always solve the trade-off problem even if the operating conditions vary. Therefore, in this paper, a new method shown in Fig. 1 for determining t_1 and t_2 in TD AGD is proposed and the validity of the proposed method is proved by measured results with both t_1 and t_2 varied in two dimensions.

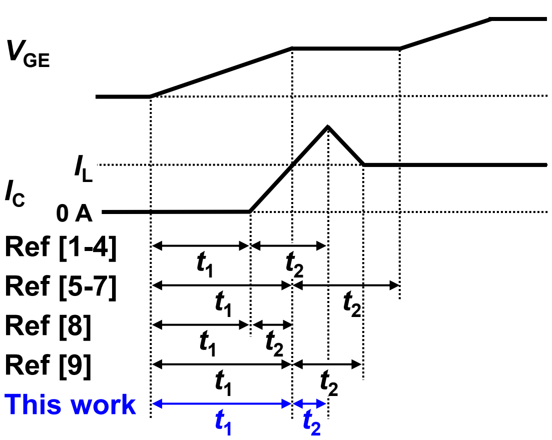
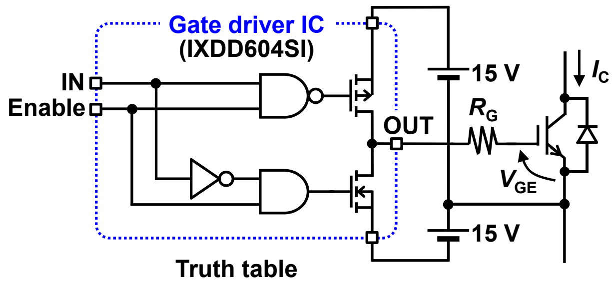


Fig. 1. Various t_1 and t_2 decision methods in TD AGD.

II. PROPOSED METHOD FOR DETERMING OPTIMUN TIME IN TIME-DOMAIN STOP-AND-GO ACTIVE GATE DRIVING

Figs. 2 and 3 show a circuit schematic and a timing chart of TD AGD in this paper, respectively. Using a gate driver IC (IXDD604SI) with an Enable input, t_1 and t_2 are controlled by controlling the timing of Enable. In this paper, only AGD at turn-on is discussed, because the trade-off relationship between switching losses and collector-to-emitter voltage (V_{CE}) overshoot at turn-off was not observed for the IGBT measured in this study. Fig. 4 shows the proposed method for determining the optimum t_1 and t_2 ($t_{1,OPT}$ and $t_{2,OPT}$). $t_{1,OPT}$ and $t_{2,OPT}$ are determined from the measured V_{GE} and I_C waveforms



Truth table

IN	Enable	OUT
0	0	High-Z
1	0	High-Z
0	1	0
1	1	1

Fig. 2. Circuit schematic of TD AGD.

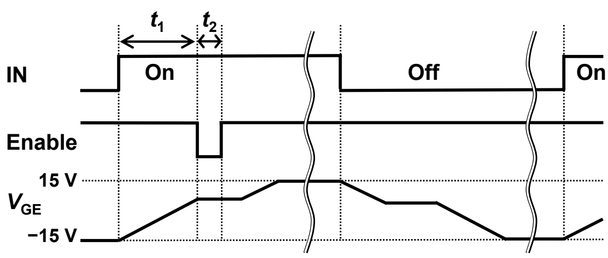


Fig. 3. Timing chart of TD AGD.

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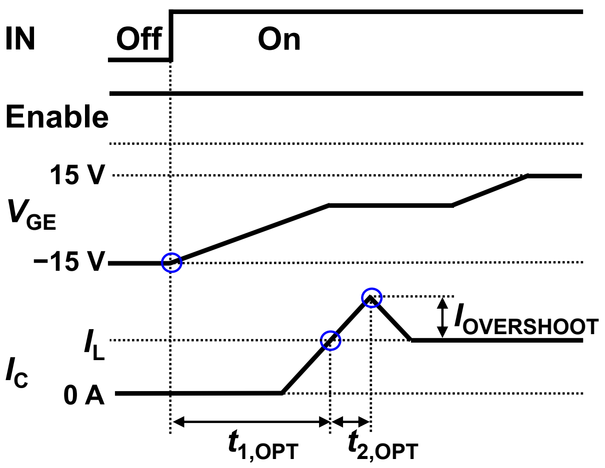

Fig. 4. Proposed method for determining $t_{1,OPT}$ and $t_{2,OPT}$.

at each operating condition such as I_L and junction temperature using conventional gate driving with the gate resistance (R_G) recommended in the datasheet of IGBTs. $t_{1,OPT}$ is the time from the rise edge of V_{GE} to $I_C = I_L$. $t_{2,OPT}$ is the time from $I_C = I_L$ to the peak of I_C. From the device physics point of view, $t_{1,OPT}$ is the time for the gate voltage to charge from −15 V to the Miller plateau voltage, and $t_{2,OPT}$ is the time for the reverse recovery current of the high-side diode to reach its peak value from 0 A. When operating conditions change, $t_{1,OPT}$ and $t_{2,OPT}$ also change, making it necessary to measure waveforms for each operating condition to determine $t_{1,OPT}$ and $t_{2,OPT}$.

III. Measured Results

Fig. 5 shows a PCB of the gate driver for TD AGD. The gate driver PCB includes a signal isolator and an isolated DC-DC converter. Figs. 6 and 7 show a circuit schematic and a measurement setup of the double pulse test using the gate driver and IGBT (CM100DY-24T, 1200 V, 100 A rating) at 600 V, respectively. Figs. 8 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and AGD at turn-on for comparison, respectively. In SGD, R_G is varied from 2.2 Ω to 33 Ω. In AGD, R_G is fixed at 3.9 Ω as recommended in the datasheet.

Figs. 9 (a) and (b) show the measured switching loss (E_{LOSS}) vs. collector current overshoot ($I_{OVERSHOOT}$) of the conventional SGD and AGD at I_L = 50 A and 100 A, respectively. The black curves show the trade-off curves for SGD with varying R_G. Figs. 10 and 11 show the measured t_1 and t_2 dependence of E_{LOSS}, $I_{OVERSHOOT}$, and the relative loss

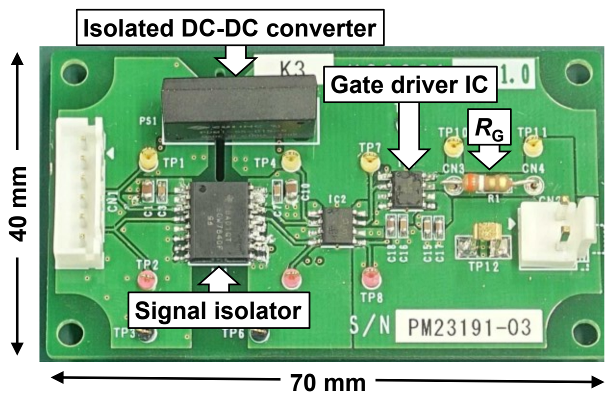

Fig. 5. PCB of gate driver for TD AGD.

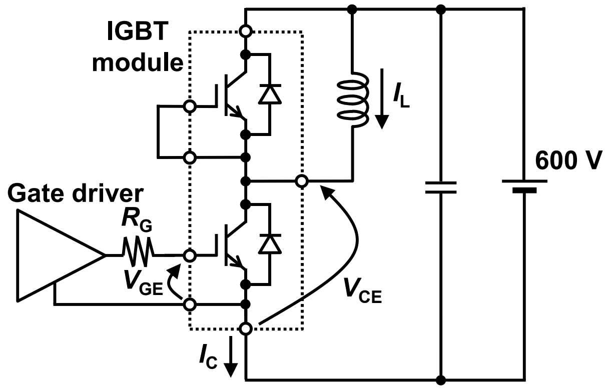

Fig. 6. Circuit schematic of double pulse.

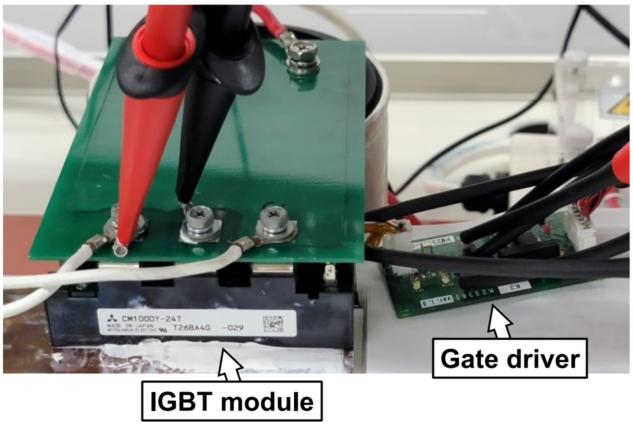

Fig. 7. Measurement setup of double pulse test.

increase (RLI) of AGD at I_L = 50 A and 100 A, respectively. The definition of RLI is as follows:

$$\mathrm{RLI} = \frac{E_{LOSS,AGD} - E_{LOSS,SGD}}{E_{LOSS,SGD}} \times 100 \qquad (1)$$

where $E_{LOSS,AGD}$ is E_{LOSS} of AGD and $E_{LOSS,SGD}$ is E_{LOSS} of SGD, which has the same $I_{OVERSHOOT}$ as AGD. $E_{LOSS,SGD}$ is calculated using a curve that is a curve approximation of the trade-off curve in Fig. 9, instead of the measured points of SGD in Fig. 9. Two types of t_1 and t_2 dependence of E_{LOSS}, $I_{OVERSHOOT}$, and RLI, global and local, are measured. In global t_1 and t_2 sweep measurements to compare the conventional and proposed methods, t_1 is varied in 50 ways from 100 ns to 590 ns in 10 ns steps, and t_2 is varied in 49 ways from 20 ns to 500 ns in 10 ns steps, for a total of 2450 combinations. In local t_1 and t_2 sweep measurements to validate the proposed method, t_1 is varied in 50 ways from 200 ns to 298 ns in 2 ns steps, and t_2 is varied in 48 ways from 14 ns to 108 ns in 2 ns steps, for a total of 2400 combinations. In this paper, the lower limit of t_2

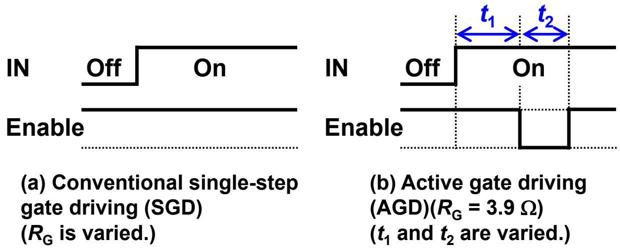

Fig. 8. Timing charts at turn-on for comparison. (a) Conventional single-step gate driving (SGD). (b) Active gate driving (AGD).

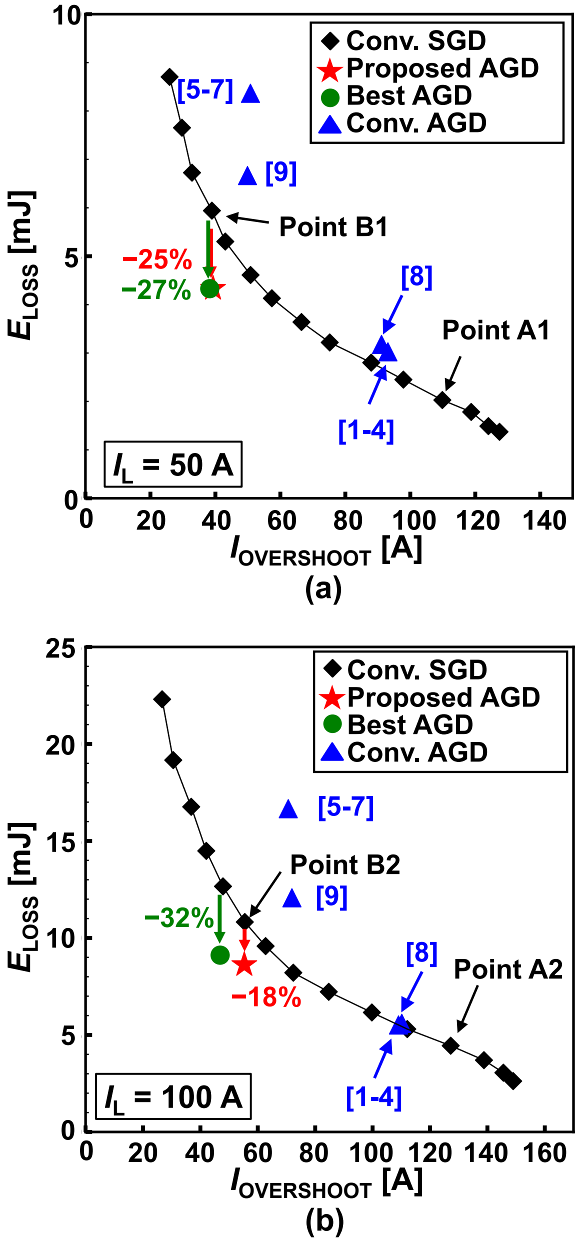

Fig. 9. Measured switching loss (E_{LOSS}) vs. collector current overshoot ($I_{OVERSHOOT}$) of conventional SGD and AGD. (a) I_L = 50 A. (b) I_L = 100 A.

was 14 ns, because when t_2 is set below 12 ns, the gate driver IC in Fig. 2 cannot be enabled for a short pulse, and the high-Z period is lost. Comparing Figs. 10 (a) and (b), and Figs. 11 (a) and (b), E_{LOSS} and $I_{OVERSHOOT}$ have a trade-off relationship. $t_{1,OPT}$ and $t_{2,OPT}$ in Figs. 10 and 11 are determined from the measured waveforms in Fig. 12 (a) and Fig. 13 (a) shown later, and AGD using them is defined as "Proposed AGD". The measurement point with the lowest RLI in all measurement points is defined as "Best AGD". If t_1 and t_2 of Proposed AGD agree with t_1 and t_2 of Best AGD, it is experimental evidence that the proposed method for determining $t_{1,OPT}$ and $t_{2,OPT}$ is correct. The optimization of t_1 is very important to reduce RLI and increase the benefit of AGD over SGD, because as shown in Figs. 10 (c) and 11 (c), the t_1 dependence of RLI is sensitive, while the t_2 dependence is insensitive. As shown in Figs. 10 (c) and 11 (c), RLI is almost minimum at $t_1 = t_{1,OPT}$ and $t_2 = t_{2,OPT}$, which supports the validity of the proposed method for determining $t_{1,OPT}$ and $t_{2,OPT}$.

To compare the conventional and proposed methods, the measured results of the conventional method [1-9] shown in Fig. 1 are also shown in Figs. 9 to 11. Table I shows a summary of RLI of the conventional methods, Proposed AGD, and Best AGD extracted from Fig. 10 (c) and Fig. 11 (c). RLI's of the conventional method [1-9] are large, while RLI of Proposed AGD is small and is fairly close to RLI of Best AGD. Specifically, at I_L = 50 A, Proposed AGD using $t_1 = t_{1,OPT}$ = 218 ns, $t_2 = t_{2,OPT}$ = 40 ns achieves RLI of − 25%. At I_L = 100 A, Proposed AGD using $t_1 = t_{1,OPT}$ = 236 ns, $t_2 = t_{2,OPT}$ = 42 ns achieves RLI of − 18%. Since t_1 and t_2 in Proposed AGD are quite close to t_1 and t_2 in Best AGD, the proposed method for determining $t_{1,OPT}$ and $t_{2,OPT}$ is experimentally proven to be correct.

Fig. 12 shows measured waveforms of Point A1, Proposed AGD, Point B1, and Best AGD in Fig. 9 (a) at I_L = 50 A. Point A1 shown in Fig. 12 (a) is the measurement point for determining $t_{1,OPT}$ and $t_{2,OPT}$ as shown in Fig. 4, where $t_{1,OPT}$ = 218 ns, $t_{2,OPT}$ = 40 ns. Point B1 shown in Fig. 12 (c) is the SGD measurement point where $I_{OVERSHOOT}$ is almost the same as Proposed AGD. Comparing Proposed AGD with R_G = 3.9 Ω in Fig. 12 (b) and Point B1 with R_G = 18 Ω, Proposed AGD reduces E_{LOSS} from 5.9 mJ to 4.3 mJ under $I_{OVERSHOOT}$ -aligned conditions by setting high-Z just before the timing of $I_{OVERSHOOT}$ and driving more strongly than Point B1 for all periods except t_2.

Fig. 13 shows measured waveforms of Point A2, Proposed AGD, Point B2, and Best AGD in Fig. 9 (b) at I_L = 100 A. Point A2 shown in Fig. 13 (a) is the measurement point for determining $t_{1,OPT}$ and $t_{2,OPT}$ as shown in Fig. 4, where $t_{1,OPT}$ = 236 ns, $t_{2,OPT}$ = 42 ns. Point B2 shown in Fig. 13 (c) is the SGD measurement point where $I_{OVERSHOOT}$ is almost the same as Proposed AGD. Comparing Proposed AGD with R_G = 3.9 Ω in Fig. 13 (b) and Point B2 with R_G = 12 Ω, Proposed AGD reduces E_{LOSS} from 10.7 mJ to 8.6 mJ under $I_{OVERSHOOT}$ -aligned conditions.

IV. Conclusions

A new method for determining $t_{1,OPT}$ and $t_{2,OPT}$ to minimize RLI in TD AGD is proposed and the validity of the proposed method is proved by measured results with both t_1 and t_2 varied in two dimensions. $t_{1,OPT}$ is the time from the rise edge of V_{GE} to $I_C = I_L$. $t_{2,OPT}$ is the time from $I_C = I_L$ to the peak of I_C. At I_L = 50 A, Proposed AGD using $t_1 = t_{1,OPT}$ = 218 ns, $t_2 = t_{2,OPT}$ = 40 ns achieves RLI of − 25%. At I_L = 100 A, Proposed AGD using $t_1 = t_{1,OPT}$ = 236 ns, $t_2 = t_{2,OPT}$ = 42 ns achieves RLI of − 18%.

TABLE I. Summary of RLI of Conventional Methods, Proposed AGD, and Best AGD

	I_L = 50 A	I_L = 100 A
Ref [1-4]	**20%**	**−0.17%**
Ref [5-7]	**84%**	**95%**
Ref [8]	**17%**	**2.6%**
Ref [9]	**43%**	**45%**
Proposed AGD	**−25% (t_1 = 218 ns, t_2 = 40 ns)**	**−18% (t_1 = 236 ns, t_2 = 42 ns)**
Best AGD	**−27% (t_1 = 218 ns, t_2 = 28 ns)**	**−32% (t_1 = 232 ns, t_2 = 22 ns)**

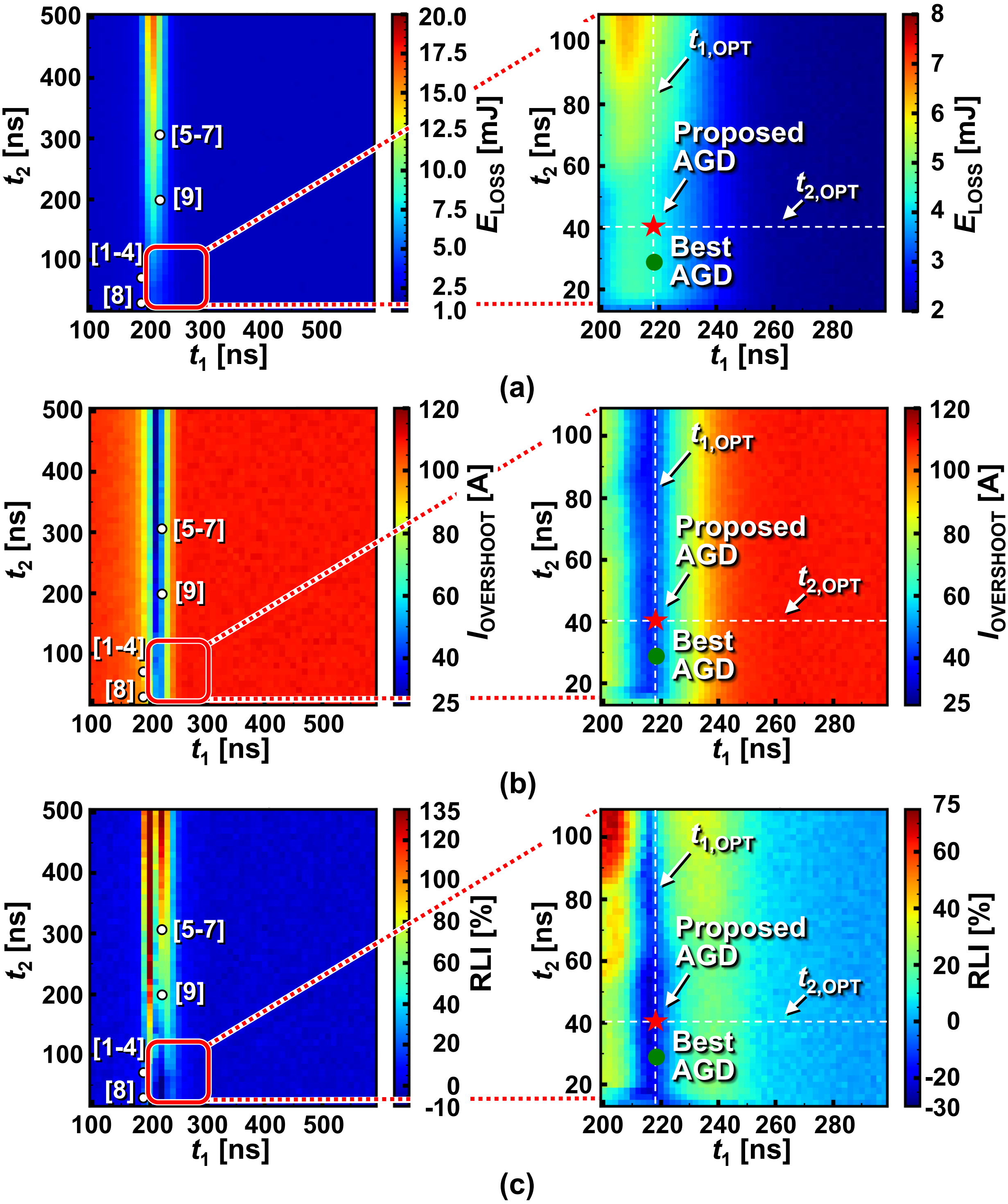

Fig. 10. Measured t_1 and t_2 dependence of (a) E_{LOSS}, (b) $I_{\mathrm{OVERSHOOT}}$, (c) relative loss increase (RLI) of AGD at I_{L} = 50 A.

REFERENCES

[1] V. John, B.-S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1108–1117, Sep-Oct 1999.

[2] S. Takizawa, S. Igarashi, and K. Kuroki, "A new di/dt control gate drive circuit for IGBTs to reduce EMI noise and switching losses," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference*, 2002, vol. 2, pp. 1443–1449 vol.2.

[3] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "Advanced active gate drive for switching performance improvement and overvoltage protection of high-power IGBTs," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3802–3815, 2018.

[4] Y. Ling, Z. Zhao, and Y. Zhu, "A self-regulating gate driver for high-power IGBTs," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3450–3461, 2021.

[5] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A novel active gate driver for improving SiC MOSFET switching trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, 2017.

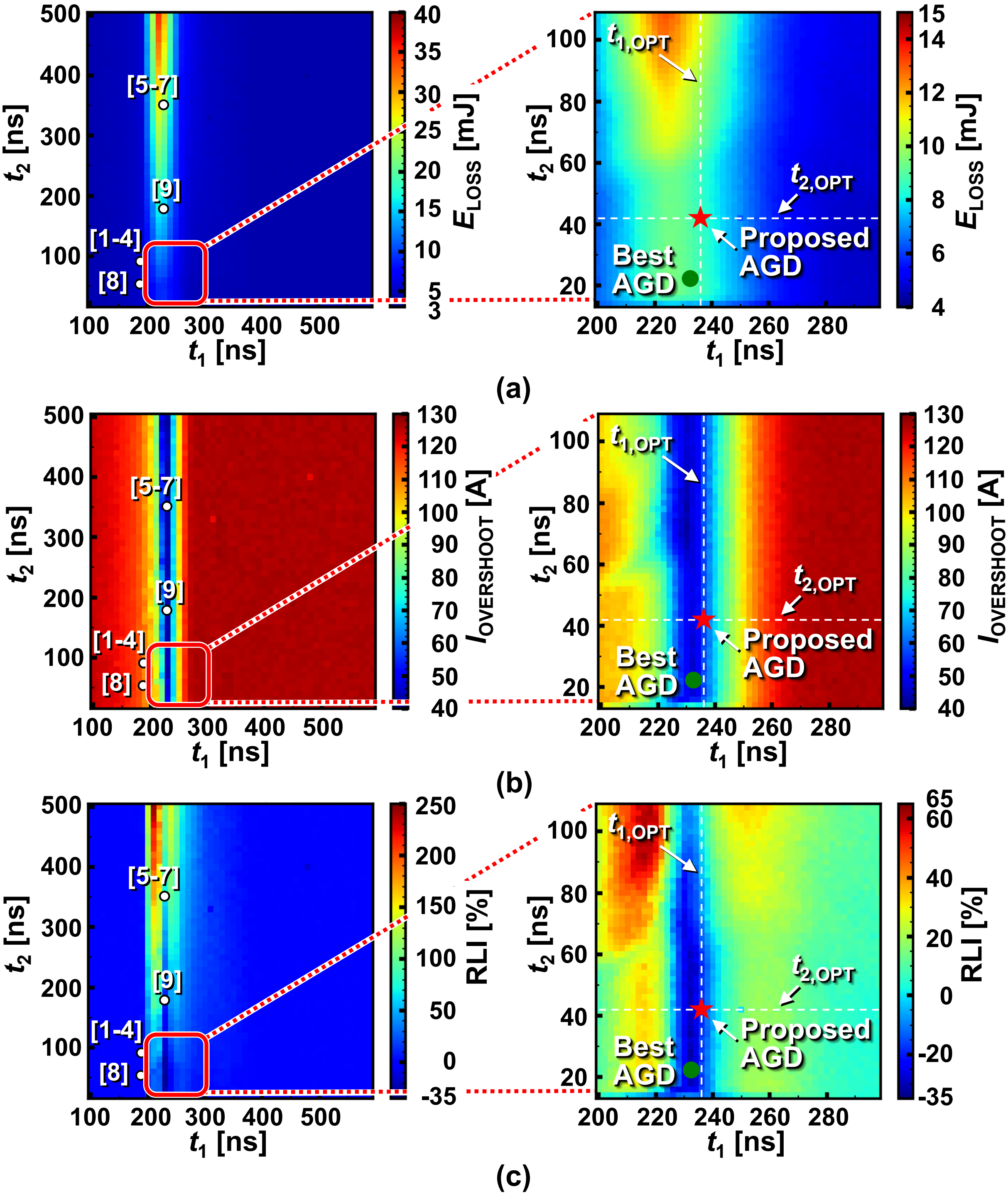

Fig. 11. Measured t_1 and t_2 dependence of (a) E_{LOSS}, (b) $I_{\mathrm{OVERSHOOT}}$, (c) relative loss increase (RLI) of AGD at I_{L} = 100 A.

[6] J. Zhu, D. Yan, S. Yu, W. Sun, G. Shi, S. Liu, and S. Zhang, "A 600V GaN active gate driver with dynamic feedback delay compensation technique achieving 22.5% turn-on energy saving," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, vol. 64, pp. 462–464.

[7] S. Yu, Q. Zhou, G. Shi, T. Wu, J. Zhu, L. Zhang, W. Sun, S. Zhang, N. He, and Y. Li, "A 400-V half bridge gate driver for normally-off GaN HEMTs with effective *dv/dt* control and high *dv/dt* immunity," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 741–751, 2023.

[8] Y. Sun, L. Sun, A. Esmaeli, and K. Zhao, "A Novel Three Stage Drive Circuit for IGBT," in *2006 1ST IEEE Conference on Industrial Electronics and Applications*, 2006, pp. 1–6.

[9] M. Riefer, J. Winkler, S. Strache, and I. Kallfass, "Implementation of current-source gate driver with open-loop slope shaping for SiC-MOSFETs," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[10] S. Kawai, T. Ueno, and K. Onizuka, "15.8 A 4.5V/ns active slew-rate-controlling gate driver with robust discrete-time feedback technique for

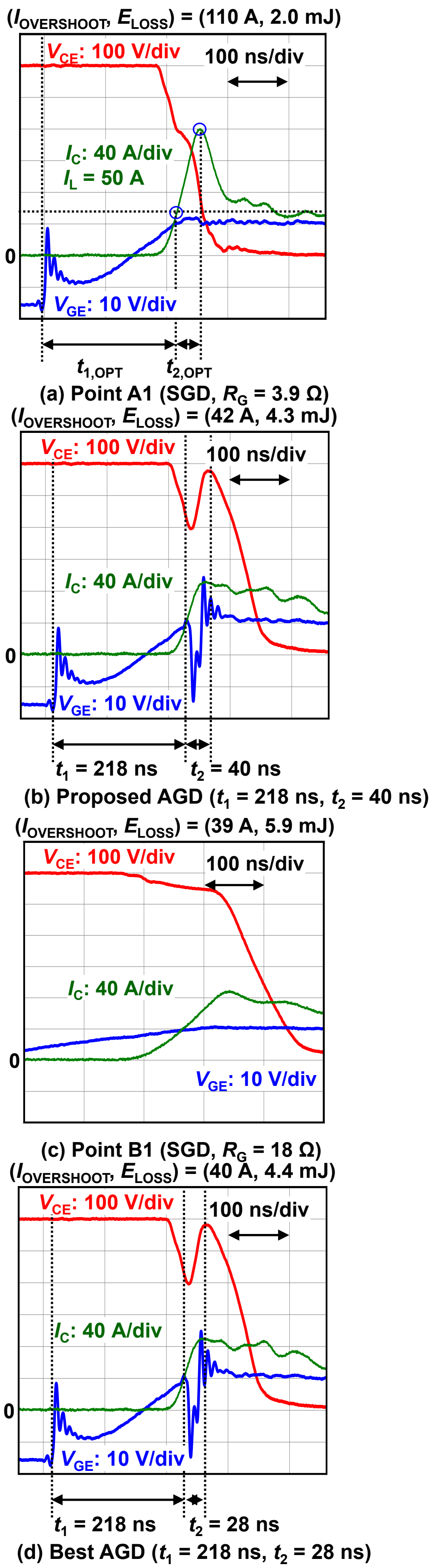

Fig. 12. Measured waveforms of Point A1, Proposed AGD, Point B1, and Best AGD in Fig. 9 (a) at I_L = 50 A.

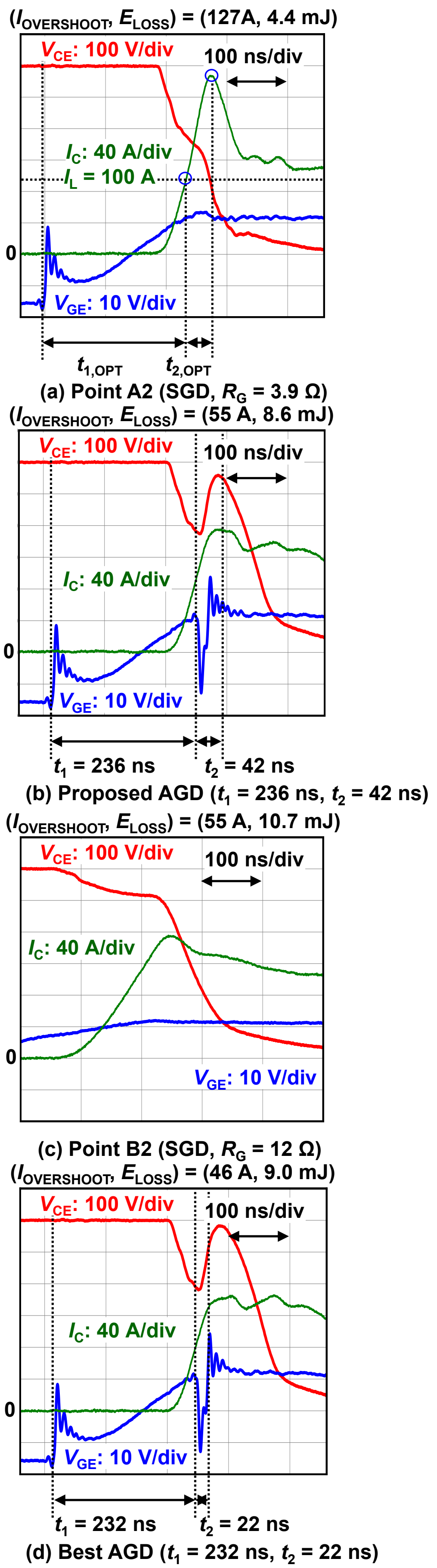

Fig. 13. Measured waveforms of Point A2, Proposed AGD, Point B2, and Best AGD in Fig. 9 (b) at I_L = 100 A.

600V superjunction MOSFETs," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2019, pp. 252–254.

[11] Y. Yang, Y. Wen, and Y. Gao, "A novel active gate driver for improving switching performance of high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7775–7787, 2019.

[12] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, 2021.

[13] M. Sayed, S. Araujo, F. Carraro, and R. Kennel, "Investigation of gate current shaping for SiC-based power modules on electrical drive system power losses," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–10.

[14] K. Horii, R. Morikawa, K. Hata, K. Morokuma, Y. Wada, Y. Obiraki, Y. Mukunoki, and M. Takamiya, "Sub-0.5 ns step, 10-bit time domain digital gate driver IC for reducing radiated EMI and switching loss of SiC MOSFETs," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–8.

[15] D. Zhang, K. Horii, K. Hata, and M. Takamiya, "Digital gate driver IC with fully integrated automatic timing control function in stop-and-go gate drive for IGBTs," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1225–1231.

[16] D. Zhang, K. Horii, K. Hata, and M. Takamiya, "Digital gate driver IC with real-time gate current change by sensing drain current to cope with operating condition variations of SiC MOSFET," in *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023, pp. 374–380.