Fully Integrated Closed-Loop Active Gate Driver IC With Real-Time Control of Gate Current Change Timing by Gate Current Sensing

Yaogan Liang
The University of Tokyo
Tokyo, Japan
liangy@iis.u-tokyo.ac.jp

Katsuhiro Hata
Shibaura Institute of Technology
Tokyo, Japan
khata@shibaura-it.ac.jp

Makoto Takamiya
The University of Tokyo
Tokyo, Japan
mtaka@iis.u-tokyo.ac.jp

***Abstract*— In order to provide a low-cost closed-loop active gate driver (AGD) that is applicable to both 3-pin and 4-pin power devices, a fully integrated closed-loop gate current sensing (GCS) AGD IC for IGBTs is proposed that controls the timing of gate current changes in real time. In an active gate driving where the gate current is changed three times from large to small to large at turn-on, GCS AGD has the function of changing the time of the first and second slots in real time by detecting the change in gate current using two comparators. Double pulse test measurements of IGBTs are performed at 600 V and under nine combinations of conditions including load current of 20 A, 50 A and 80 A, and temperature of 25 ˚C, 75 ˚C and 125 ˚C, using GCS AGD IC fabricated with 180 nm BCD process. The results show that the proposed GCS AGD reduces the switching loss (E_{LOSS}) and the collector current overshoot ($I_{OVERSHOOT}$) in all nine conditions compared to the conventional single-step gate driving. Specifically, in the nine conditions, with the same $I_{OVERSHOOT}$, the E_{LOSS} is reduced by 16% to 30%, and without increasing E_{LOSS}, the reduction in $I_{OVERSHOOT}$ range from 14% to 21%.**

Keywords—active gate driver, gate current sensing, switching loss, current overshoot, trade-off curve

I. INTRODUCTION

Active gate driver (AGD) [1-28], which changes the gate driving strength multiple times in fine time slots during the switching period of power devices, is attracting attention as a technology that can solve the trade-off problem between energy loss and noise during power device switching. AGD with closed-loop [9-28] instead of open-loop [1-8] is essential to cope with operating condition variations such as load current and temperature. The target of this paper is to develop a fully integrated closed-loop AGD IC with automatic control of gate current (I_G) change timing that senses only the gate terminal of power devices at any reasonable gate resistance (R_G) value. Table I shows a comparison table of the closed-loop AGD IC with automatic control of I_G change timing. Drain-to-source voltage (V_{DS}) sensing cannot be fully integrated on IC because of the high voltage of V_{DS} [26] or requires a high voltage IC process [23], resulting in high AGD costs. Sensing using a Kelvin emitter or source [24, 26] can be used with 4-pin power devices, but not with 3-pin power devices. While gate-to-source voltage (V_{GS}) sensing [22, 28] provides gate terminal-only sensing, [22] is not fully integrated because it requires an FPGA, and [28] has been demonstrated to operate at high R_G of 125 Ω, and [28] is expected to malfunction when used under fast switching conditions at low R_G. To solve the problems, a fully integrated closed-loop gate current sensing (GCS) AGD IC with no restriction on R_G value for IGBTs is proposed controlling the timing of I_G changes in real time, which is applicable to both 3-pin and 4-pin power devices.

TABLE I. COMPARISON TABLE OF CLOSED-LOOP AGD IC WITH AUTOMATIC CONTROL OF I_G CHANGE TIMING

	APEC'23 [24]	TIE'23 [23]	ISPSD'24 [26]	ISPSD'22 [22]	TPEL'24 [28]	This work
Target power device	IGBT	GaN	SiC	SiC	SiC	IGBT
Measured conditions	600 V, 80 A	400 V, 10 A	Simulated	Simulated	400 V, 40 A	600 V, 80 A
Sensor input	V_{Ee} (1)	V_{DS}	V_{DS} , V_{Ss} (2)	V_{GS}	V_{GS}	I_G
Sensing gate terminal only	No	No	No	Yes	Yes	Yes
Arbitrary R_G value	Yes	Yes	Yes	Yes	No(3)	Yes
Real-time control	Yes	Yes	No	No	Yes	Yes
Number of states per switching	3	4	4	2	3	3
I_G levels	6 bit	3	NA	5	NA	6 bit
Fully integrated on IC	Yes	Yes	No(4)	No	Yes	Yes
IC Process	180 nm BCD	500 nm, 600 V SOI(5)	180 nm BCD	180 nm BCD	180 nm BCD	180 nm BCD

(1) Voltage between power emitter and Kelvin emitter
(2) Voltage between power source and Kelvin source
(3) R_G = 125 Ω
(4) Voltage divider for V_{DS} is not integrated.
(5) Requires IC process with breakdown voltage higher than the main circuit voltage.

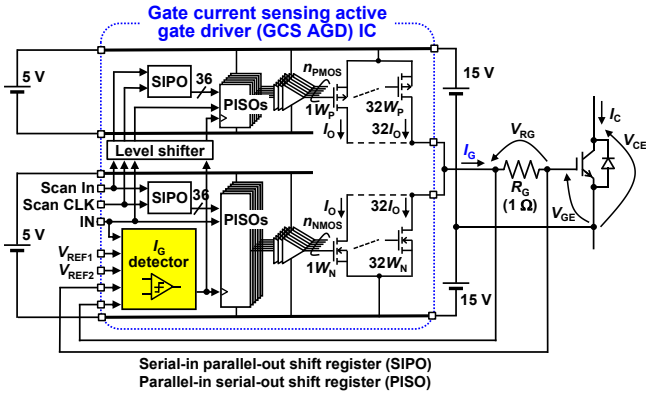

Fig. 1: Circuit schematic of proposed GCS AGD IC.

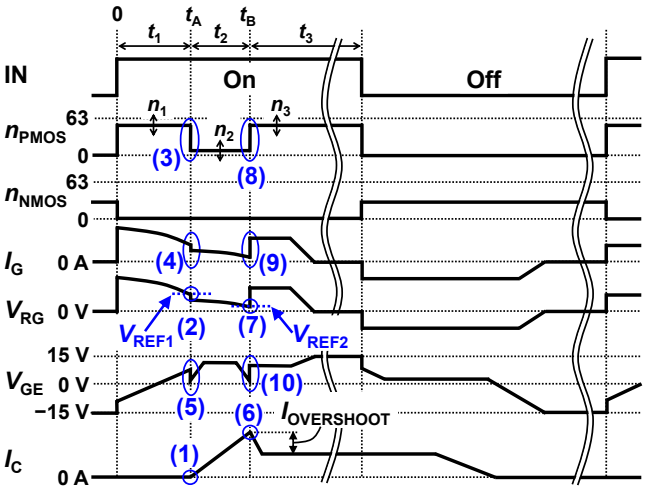

Fig. 2: Timing chart of proposed GCS AGD IC.

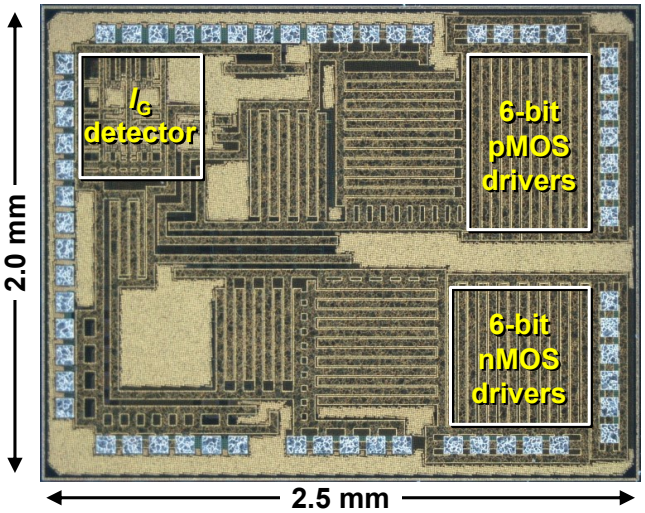

Fig. 3: Die photo of GCS AGD IC.

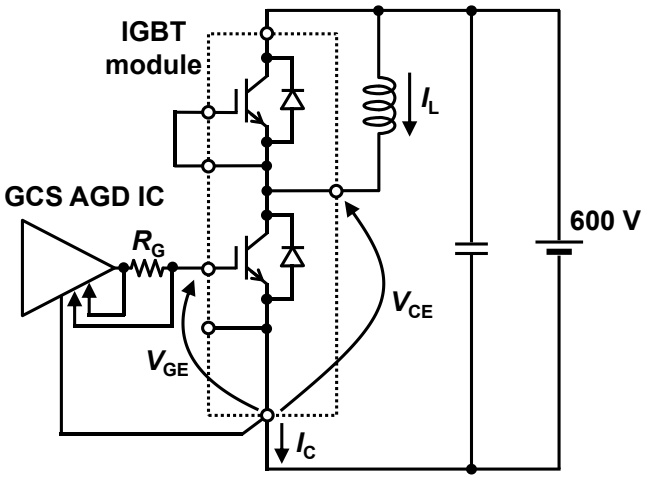

Fig. 4: Circuit schematic of double pulse test.

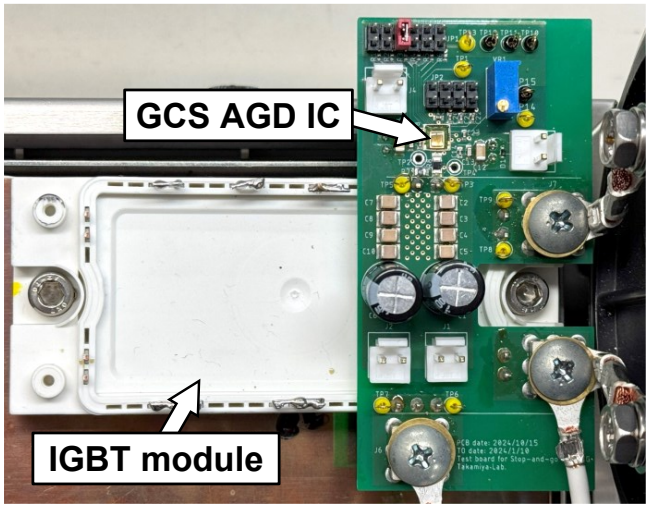

Fig. 5: Measurement setup.

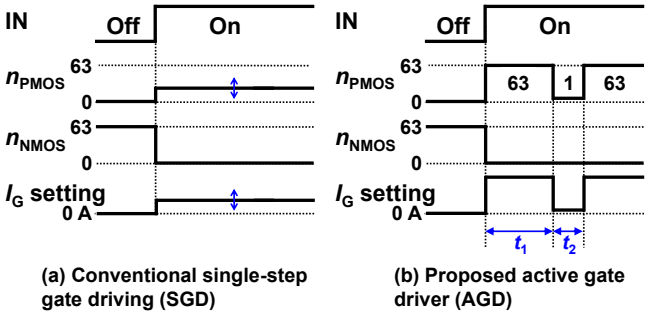

Fig. 6: Timing charts for turn-on.

II. Proposed Gate Current Sensing Active Gate Driver IC

Figs. 1 and 2 show a circuit schematic and a timing chart of the proposed GCS AGD IC, respectively. The IC includes I_G detector to determine the timing of I_G changes, controller for the state change, and a 6-bit digital gate driver with variable I_G in 64 levels, where $I_G = n_{PMOS} \times 95$ mA and n_{PMOS} is an integer from 0 to 63. At turn-on, an active gate driving is performed in three slots from t_1 to t_3 with different I_G of strong (n_1) -weak (n_2) -strong (n_3). n_1 to n_3 are preset by a digital input (Scan In), while t_1 and t_2 are automatically determined by I_G detector. To sense I_G, the voltage drop (V_{RG}) due to I_G and R_G is given to I_G detector, and V_{RG} is compared with two reference voltages (V_{REF1} and V_{REF2}) by two comparators inside I_G detector, respectively. Fig. 2 shows the sequence for determining the end timing of t_1 (t_A) and the end timing of t_2 (t_B). t_A is the timing when the collector current (I_C) rises from 0 A and t_B is the timing when I_C peaks. The role of I_G detector is to detect t_A and t_B from V_{RG}. V_{REF1} and V_{REF2} should be adjusted in advance so that t_A and t_B can be detected, respectively. When gate-to-emitter voltage (V_{GE}) reaches the IGBT threshold voltage and I_C rises from 0 A (1), V_{RG} crosses V_{REF1} and I_G detector detects t_A (2). As the controller changes n_{PMOS} from n_1 to n_2 (3), I_G decreases (4) and V_{GE} also decreases (5). When I_C peaks (6), V_{RG} crosses V_{REF2} and I_G detector detects t_B (7). As the controller changes n_{PMOS} from n_2 to n_3 (8), I_G increases (9) and V_{GE} also increases (10). Fig. 3

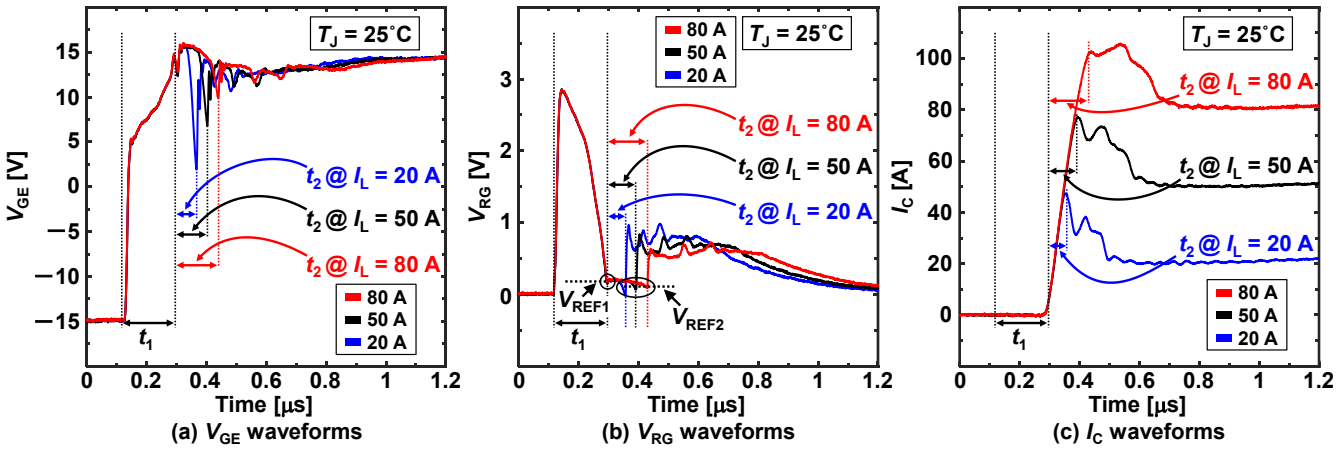

Fig. 7: Measured V_{GE}, V_{RG}, and I_C waveforms in GCS AGD with varied load current (I_L) from 20 A to 80 A at T_J = 25 ˚C.

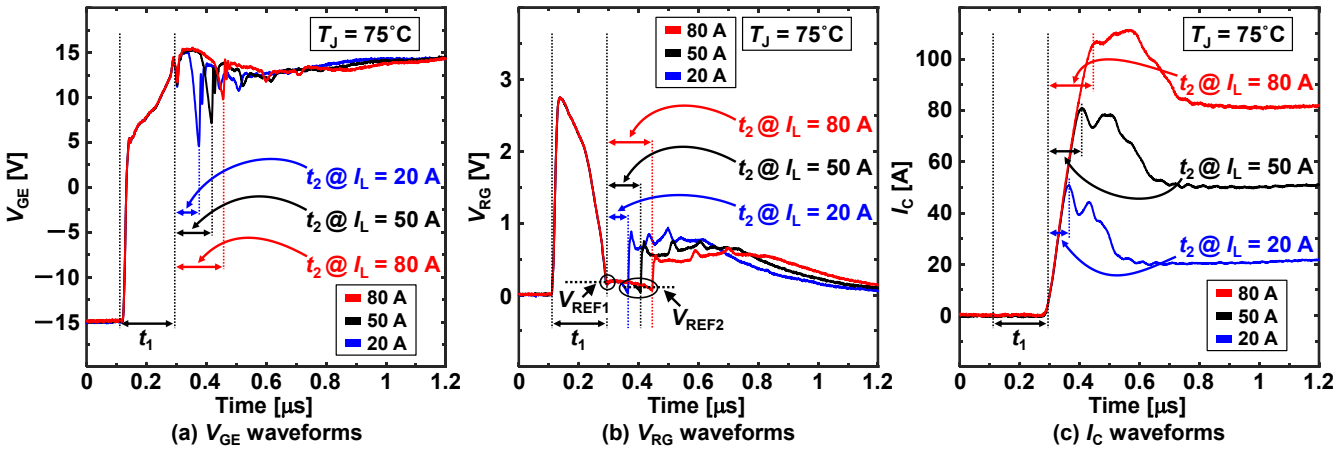

Fig. 8: Measured V_{GE}, V_{RG}, and I_C waveforms in GCS AGD with varied load current (I_L) from 20 A to 80 A at T_J = 75 ˚C.

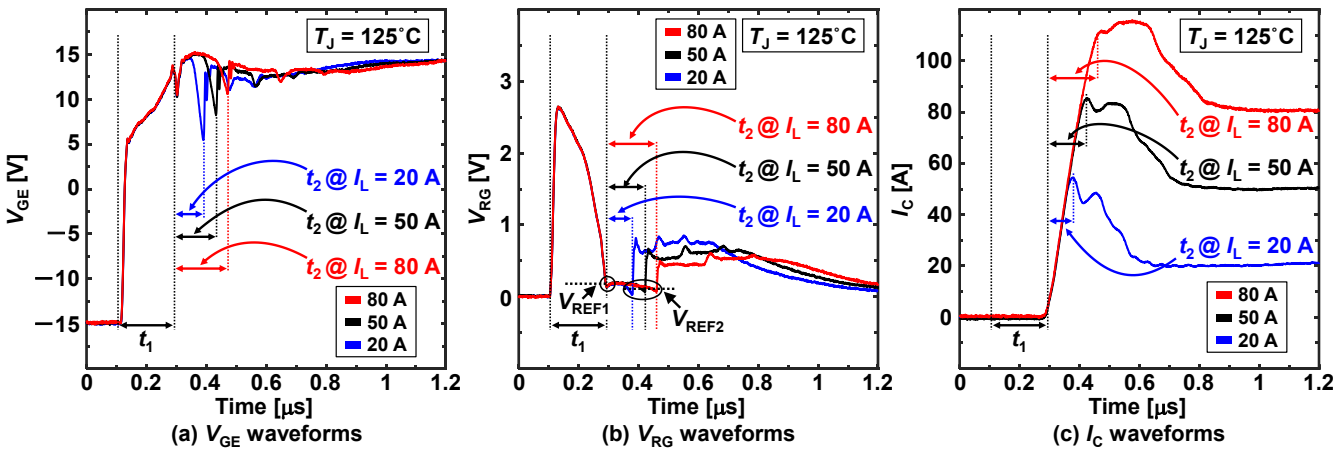

Fig. 9: Measured V_{GE}, V_{RG}, and I_C waveforms in GCS AGD with varied load current (I_L) from 20 A to 80 A at T_J = 125 ˚C.

shows a die photo of GCS AGD IC fabricated with 180-nm BCD process.

III. Measured Results

Figs. 4 and 5 show a circuit schematic and a measurement setup of the double pulse test at 600 V using the developed GCS AGD IC and an IGBT module (FS100R12N2T4, 1200 V, 100 A), respectively. R_G is 1 Ω. Note that the role of R_G in this paper is not to adjust the gate driving strength but to be a sense resistor for I_G measurement. In this paper, the gate driving strength adjustment is done by digitally controlling n_{PMOS} in Fig. 2. This IGBT module has a Kelvin emitter pin, but since the purpose of this paper is to demonstrate the effectiveness of the proposal in a 3-pin IGBT, the Kelvin emitter pin is left floating for the

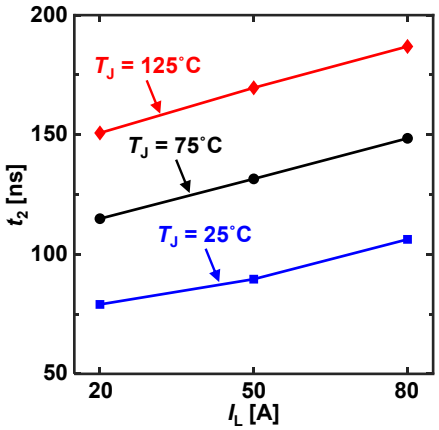

Fig. 10: Measured t_2 vs. I_L at T_J = 25 ˚C, 75 ˚C, and 125 ˚C.

measurements. Figs. 6 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and the proposed AGD for comparison, respectively. In SGD, n_{PMOS} is varied, which emulates a conventional gate driver with varied gate resistance. In AGD, (n_1, n_2, n_3) are preset to (63, 1, 63), and t_1 and t_2 are automatically determined by GCS.

Figs. 7, 8 and 9 show the measured V_{GE}, V_{RG}, and I_C waveforms in GCS AGD with varied load current (I_L) from 20 A to 80 A and with different T_J from 25 ˚C to 125 ˚C, respectively. In Fig. 7 (b), Fig. 8 (b) and Fig. 9 (b), it is clearly observed that t_1 is determined at the intersection of V_{RG} and V_{REF1}, and t_2 is determined at the intersection of V_{RG} and V_{REF2}. In Figs. 7, 8 and 9, as I_L increases, t_1 remains constant at the same T_J, and as T_J becomes higher, t_1 slightly increases because I_G decreases as gate driver IC temperature rises, increasing gate capacitance charging time. On the other hand, Fig. 10 shows the measured t_2 vs. I_L relationship of the measured results at different T_J. Because t_2 represented the time that I_C changes from zero to its peak value, t_2 is automatically changed by GCS AGD for best performance under different conditions. It can be observed that t_2 increases approximately linearly with I_L at the same T_J. And for the same I_L, t_2 duration increases as T_J increases, because according to the characteristics of the tested IGBT module, $I_{OVERSHOOT}$ increases as T_J increases. Therefore, the proposed GCS AGD can automatically extend the time slots (t_2) with weak driving strength to suppress the surge current under different I_C and T_J conditions.

Figs. 11 (a) to (c) show the measured switching loss (E_{LOSS}) vs. the collector current overshoot ($I_{OVERSHOOT}$) of the conventional SGD and the proposed AGD under nine combinations of conditions including I_L = 20 A, 50 A and 80 A, and T_J = 25 ˚C, 75 ˚C and 125 ˚C. All the trade-off curves of the conventional SGD is measured with varied n_{PMOS} from 4 to 63. The result points of proposed AGD is marked as colored stars. Because the proposed AGD breaks the trade-off relationship between E_{LOSS} and $I_{OVERSHOOT}$ under all conditions by automatically changing t_1 and t_2, Fig. 11 (a) to (c) clearly show that the proposed AGD is on the lower left side compared to the trade-off curve of the conventional SGD. At I_L = 20 A in Fig, 11 (a), compared with the conventional SGD, the proposed AGD reduces E_{LOSS} by 16 %, 16 %, and 16 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 14 %, 17 %, and 21 % under E_{LOSS}-aligned condition at T_J = 25 °C, 75 °C, and 125 °C, respectively. At I_L = 50 A in Fig, 11 (b), compared with the conventional SGD, the proposed AGD reduces E_{LOSS} by 30 %, 26 %, and 29 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 18 %, 20 %, and 21 % under E_{LOSS}-aligned condition at T_J = 25 °C, 75 °C, and 125 °C, respectively. At I_L = 80 A in Fig, 11 (c), compared with the conventional SGD, the proposed AGD reduces E_{LOSS} by 25 %, 22 %, and 26 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 18 %, 14 %, and 17 % under E_{LOSS}-aligned condition at T_J = 25 °C, 75 °C, and 125 °C, respectively.

In Figs. 11 (a) and (c), Points A1 to D1 and Point A2 to D2 are defined, where Point B1 and B2 are the proposed AGD, Point A1 and A2 are SGD with closest $I_{OVERSHOOT}$ comparing to Point B1 and B2, and Point C1 and C2 are SGD with the closest E_{LOSS} comparing to Point B1 and B2. Point D1 and D2 are SGD with n_{PMOS} = 63, which are equivalent to t_2 = 0 ns in AGD, and thus worth comparing with Point B1 and B2. Figs. 12 (a) to (d) and Figs. 13 (a) to (d) show the measured waveforms of Points A1 to D1 and A2 to D2 in Figs. 11 (a) and (c) at I_L = 20 A, T_J = 25 ˚C and I_L = 80 A, T_J = 125 ˚C, respectively. Point B1 in Fig. 12 (b) and Point B2 in Fig 13 (b) clearly demonstrate the time slot (t_1 and t_2) change operation of the proposed GCS AGD IC.

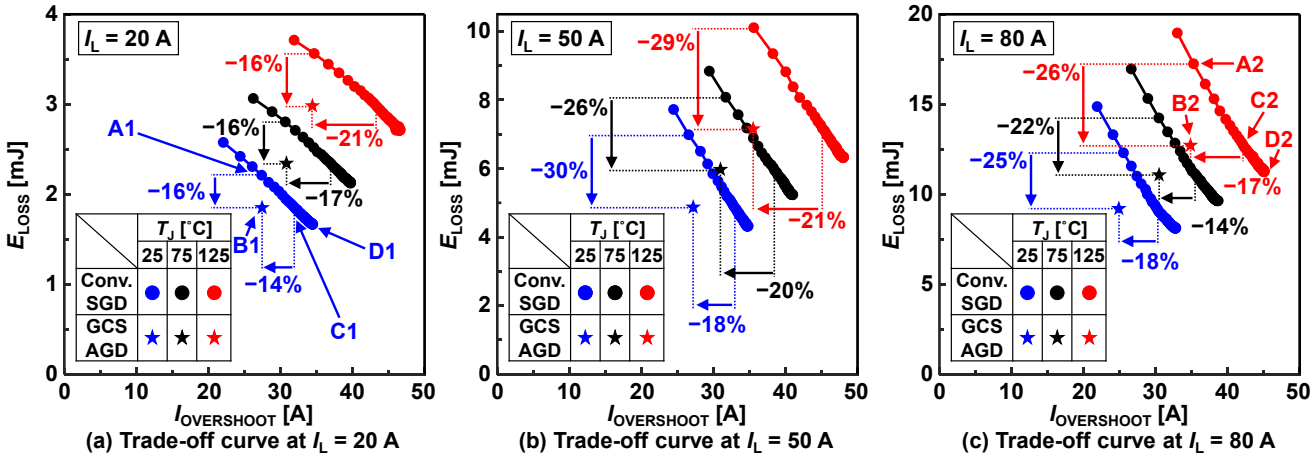

Fig. 11: Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SGD and proposed AGD at I_L = 20 A, 50 A, and 80 A and T_J = 25 ˚C, 75 ˚C, 125 ˚C.

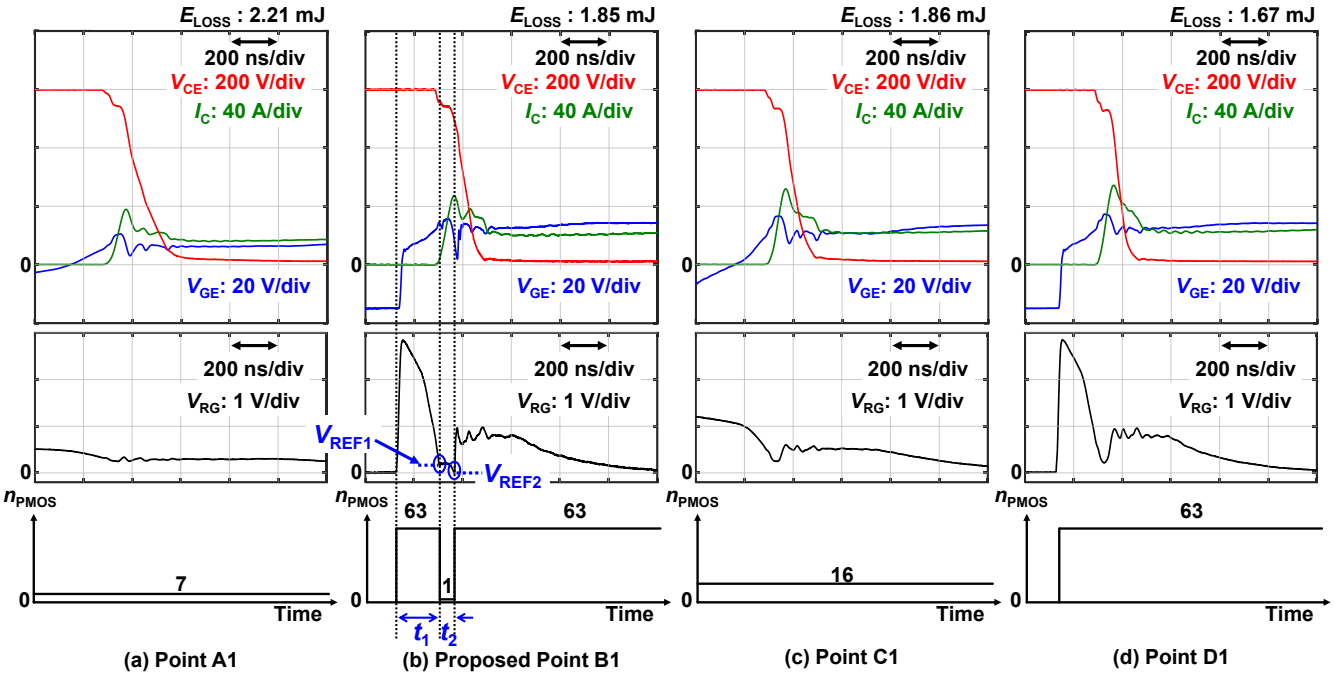

Fig. 12: Measured waveforms of Points A1 to D1 in Fig. 11 (a) at I_L = 20 A and T_J = 25 ˚C.

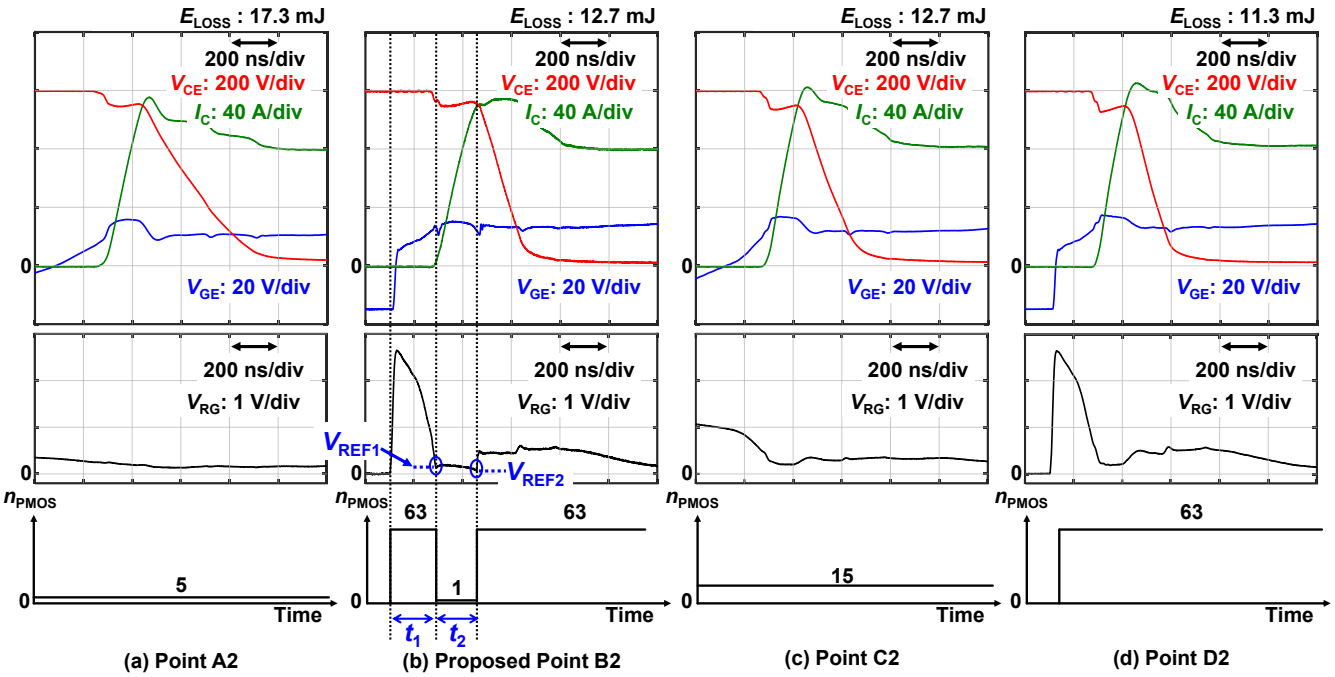

Fig. 13: Measured waveforms of Points A2 to D2 in Fig. 11 (c) at I_L = 80 A and T_J = 125 ˚C.

Point A1 and A2 have similar $I_{OVERSHOOT}$ as B1 and B2, but the I_C and V_{CE} overlaps are larger. The I_C and V_{CE} overlaps in C1 and C2 are similar as B1 and B2, but the $I_{OVERSHOOT}$ is higher. Compared with D1 and D2, the proposed point B1 and B2 greatly reduced the $I_{OVERSHOOT}$ and dI_C/dt for the strong-weak-strong I_G configuration. As shown in Table I, this paper is the first work achieving sensing only the gate terminal, no restriction on R_G value, real-time control, and fully integrated on IC in the closed-loop AGD IC with automatic control of I_G change timing.

IV. Conclusions

In this work, the first fully integrated GCS AGD IC is proposed to break the trade-off relationship between E_{LOSS} and $I_{OVERSHOOT}$ in real time and without restriction on R_G value. The proposed IC automatically determines the timing of I_G changes

and varies the driving strength in the order of strong-weak-strong to suppress surge current without greatly increasing E_{LOSS}. For verification, double pulse test experiments are conducted under nine condition combinations with I_L = 20 A, 50 A and 80 A and T_J = 25 ˚C, 75 ˚C and 125 ˚C. Compared with the conventional SGD, the results of AGD move to the lower-left corner of the trade-off curve at all conditions. The proposed AGD reduces E_{LOSS} by 16 %, up to 30 % and up to 26 % under $I_{OVERSHOOT}$-aligned condition at 20 A, 50 A and 80 A, respectively. With almost the same E_{LOSS}, the reduction in $I_{OVERSHOOT}$ achieves up to 21 %, up to 21 % and up to 18 % at 20 A, 50 A and 80 A, respectively.

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