Demonstration of Efficiency Increase of 350 V-to-13.3 V Isolated DC-DC Converters for Electric Vehicles by Active Gate Driving

Yohei Sukita
The University of Tokyo
Tokyo, Japan
ysukita@iis.u-tokyo.ac.jp

Katsuhiro Hata
Shibaura Institute of Technology
Tokyo, Japan
khata@shibaura-it.ac.jp

Hiroki Kondo
Toyota Industries Corporation
Aichi, Japan

Kenichi Watanabe
Toyota Industries Corporation
Aichi, Japan

Kenichi Nagayoshi
Toyota Industries Corporation
Aichi, Japan

Makoto Takamiya
The University of Tokyo
Tokyo, Japan
mtaka@iis.u-tokyo.ac.jp

***Abstract*—An active gate driving (AGD) is applied to a power converter product, and the efficiency increase of the power converter by AGD is demonstrated by measurements under switching noise aligned condition compared to a conventional gate driving. Specifically, the gate driver for a single Si power MOSFET comprising a 165 kHz, 350 V-to-13.3 V isolated DC-DC converter product for electric vehicles was replaced with a developed time-domain stop-and-go active gate driver, and the DC-DC converter efficiency and the spectrum amplitude at 27 MHz of the power MOSFET drain current of the conventional single-step gate driving and the proposed AGD are compared in measurements at 1.2 kW (= 13.3 V, 90 A) output. The results show that the proposed AGD reduces switching loss by 45% compared to the conventional single-step gate driving under the drain current spectrum amplitude alignment condition, resulting in a 10% reduction in total DC-DC converter loss and a 0.9% increase in DC-DC converter efficiency from 90.3% to 91.2%.**

Keywords—active gate drive, switching loss, DC-DC converter, efficiency

I. Introduction

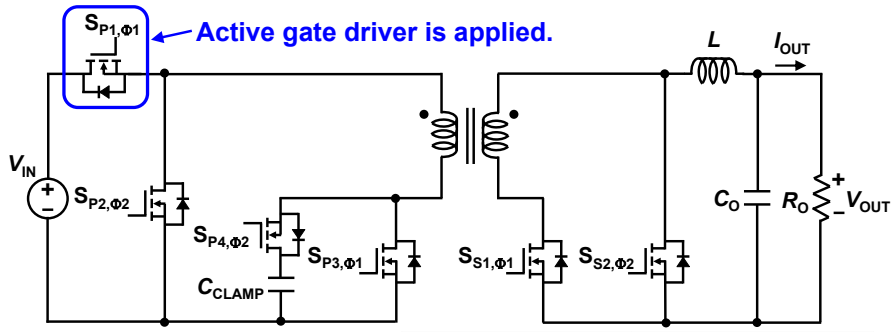
Active gate driving (AGD), which changes the gate driving strength multiple times in fine time slots during the switching period of power devices, is attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching. Most papers on AGD, however, are limited to measurements of double-pulse tests in half-bridge circuits [1-16], and very few papers have quantitatively demonstrated the advantages of AGD to the whole power converter with measurements [17-19]. Table I shows previous papers that have applied AGD to power converters. In conventional gate driving, which varies the gate resistance, loss and noise during power device switching are in a trade-off relationship. Therefore, to demonstrate the superiority of AGD over the conventional gate driving, it is necessary to either align noise and compare loss or align loss and compare noise. [17] and [18], however, do not show the measured efficiency increase under noise-aligned conditions. [19] shows the measured efficiency increase under noise-aligned conditions, however, it lacks reality because the power converter is not a commercial product, but a prototype. To solve the problems, in this paper, AGD is applied to a power converter product, and the efficiency increase of the power converter by AGD is demonstrated by measurements under noise-aligned conditions.

TABLE I. Comparison Table of Power Converters With AGDs Applied

Reference	[17]	[18]	[19]	This work
Power device	GaN	IGBT	SiC	Si MOSFET
Power converter	Boost converter	Buck converter	3-phase inverter	Isolated DC-DC
Types of Power Converters	Prototype	Prototype	Prototype	Product
V_{IN}	12 V (DC)	300 V (DC)	282 V (DC)	350 V (DC)
V_{OUT}	24 V (DC)	50 V (DC)	200 V (AC)	13.3 V (DC)
Output power	NA	500 to 5 kW	NA	1.2 kW
Switching frequency	NA	10 kHz	2 kHz, 20 kHz	165 kHz
Efficiency increase by AGD	Loss: 9.79 W ➔1.55 W (Simulated)	92.4% ➔93.1% (0.7%)	95.1%➔95.4% (0.3%) @ 2 kHz 83.9%➔85.2% (1.3%) @ 20 kHz	90.3% ➔91.2% (0.9%)
Types of noise	V_{DS} spectrum	NA	Surge voltage	I_D spectrum
Measured efficiency increase under noise-aligned conditions	No	No	Yes	Yes

II. Time-Domain Stop-And-Go Active Gate Driver

Fig. 1 shows a circuit schematic [20] and specifications of a 350 V-to-13.3 V isolated DC-DC converter product for electric vehicles to which AGD is applied. The time-domain stop-and-go active gate driver (TD AGD) [1-16], which changes the gate driving strength three times from “strong to high-Z to strong”, is applied only to the turn-on of Si power MOSFET (S_{P1}), which has the largest hard switching loss in the DC-DC converter. Figs. 2 and 3 show the circuit schematic of TD AGD and IN1 generator, which generates t_1 and t_2, the key parameters determining the performance of TD AGD, respectively. IN2 generator is the dummy delay circuit of IN1 generator. Figs. 4 and 5 show the timing chart and PCB photo of TD AGD, respectively. In the timing chart in Fig. 4, the delay of the



Parameters	Value
Input voltage (V_{IN})	350 V
Output voltage (V_{OUT})	13.3 V
Output current (I_{OUT})	80, 90 A (This work)
Output power (P_{OUT})	1.1, 1.2 kW (This work) 2.2 kW (Rating)
Switching frequency	165 kHz

Fig. 1: Isolated DC-DC converter for EVs to which AGD is applied.

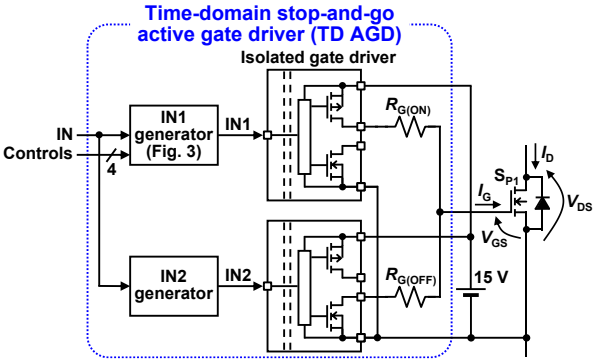


Fig. 2: Circuit schematic of TD AGD.

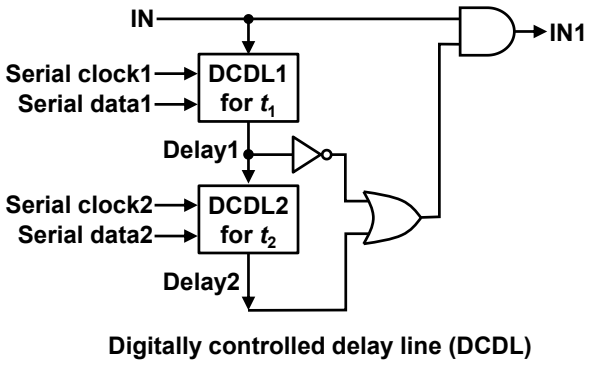


Fig. 3: Circuit schematic of IN1 generator.

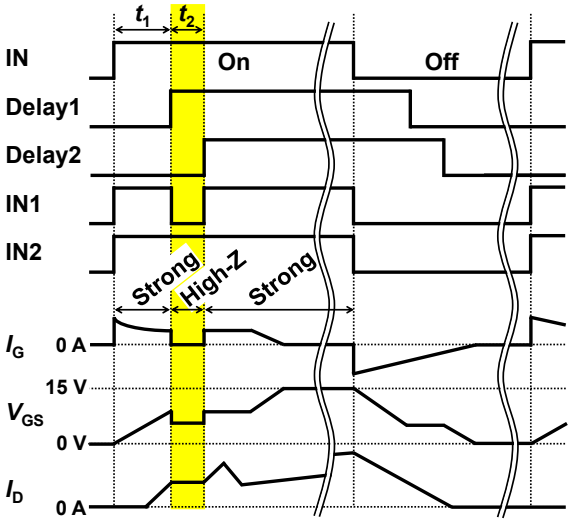


Fig. 4: Timing chart of TD AGD.

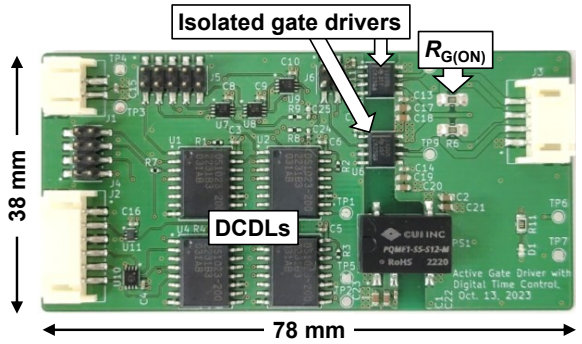


Fig. 5: PCB photo of TD AGD.

isolated gate drivers and the logic gates is assumed to be zero. As shown in Fig. 4, the first strong drive period after turn-on is defined as t_1, and the next high-Z drive period as t_2. TD AGD, implemented with two isolated gate drivers (UCC5320SCDR) and two 8-bit digitally controlled delay lines (DCDLs) (DS1023S-200+), allows t_1 and t_2 to be changed in 2 ns steps through digital control signals of "Serial data1" and "Serial data2" in Fig. 3.

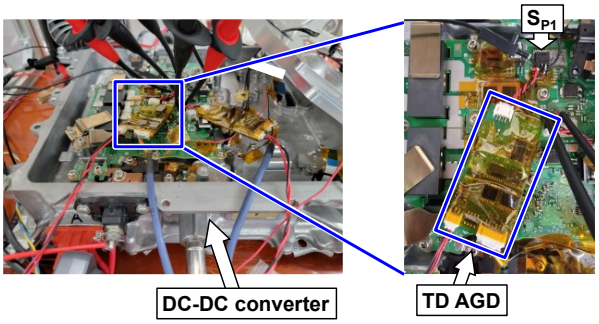


Fig. 6: Measurement setup of DC-DC converter.

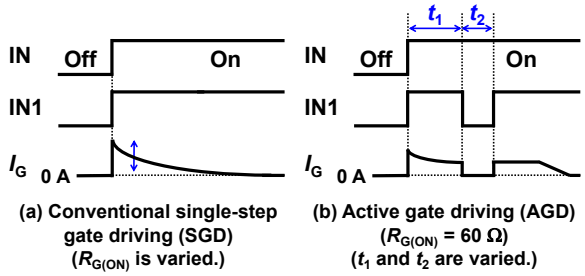


Fig. 7: Timing charts of the conventional SGD and proposed AGD at turn-on for comparison.

III. Measured Results

A. Measurement Setup

Fig. 6 shows the measurement setup of the DC-DC converter with the gate driver of S_{P1} modified to TD AGD. The measurements were performed under the conditions shown in Fig. 1. Figs. 8 to 14 show the measured results at output current (I_{OUT}) = 90 A, and Figs. 15 to 17 show the measured results at I_{OUT} = 80 A. In this paper, the performance improvement effect of AGD is investigated in I_{OUT} range where the DC-DC converter is in hard-switching operation instead of soft-switching. Figs. 7 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and the proposed AGD at turn-on for comparison, respectively. In SGD, the operation is performed by setting $t_1 = t_2 = 0$ ns in TD AGD and the gate resistance $R_{G(ON)}$ shown in Fig. 2 is varied in 6 ways from 30 Ω to 200 Ω. In AGD, $R_{G(ON)}$ = 60 Ω is fixed and t_1 and t_2 are varied using DCDLs.

B. Measured Results at I_{OUT} = 90 A

Figs. 8 and 9 show the measured gate-to-source voltage (V_{GS}), drain-to-source voltage (V_{DS}), and drain current (I_D) waveforms and I_D spectrums of S_{P1} in SGD, respectively. Increasing $R_{G(ON)}$ reduces switching speed of S_{P1} (Fig. 8) and I_D spectrum amplitude (Fig. 9). Since peaks of I_D spectrums are observed near 27 MHz in Fig. 9, the maximum value of I_D spectrum amplitude in the range of 26 MHz to 28 MHz is defined as I_D spectrum amplitude at 27 MHz in this paper, and it is used as an index of the switching noise.

Fig. 10 shows the measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz in SGD and AGD. The SGD curve is obtained from Figs. 8 and 9. To find the best AGD, t_1 and t_2 of TD AGD are adjusted in 2 ns steps to maximize the

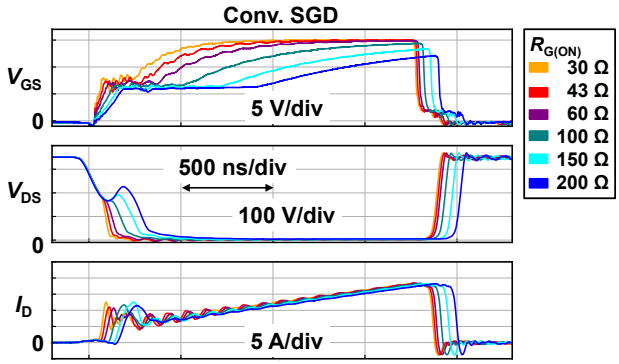


Fig. 8: Measured waveforms of S_{P1} in SGD at I_{OUT} = 90 A.

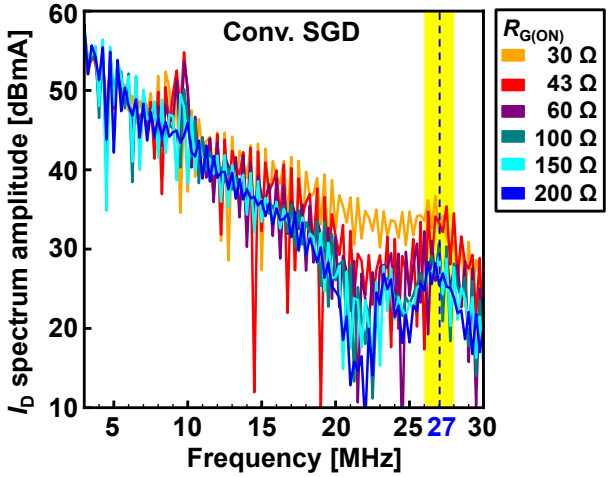


Fig. 9: Measured I_D spectrums of S_{P1} in SGD at I_{OUT} = 90 A.

efficiency increase of AGD relative to SGD under I_D spectrum amplitude alignment condition. As an example of t_1-dependent measured results of AGD, in Fig. 10, t_2 = 50 ns is fixed and t_1 is varied from 90 ns to 98 ns in 2 ns increments. The AGD with t_1 = 94 ns and t_2 = 50 ns is defined as the best AGD.

Fig. 11 shows the measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz in SGD and the best AGD. SGD shows a clear trade-off curve between efficiency and I_D spectrum amplitude. Points A and C are the conventional SGD points with efficiency and I_D spectrum amplitude approximately the same as the best AGD (Point B), respectively. Compared with Points A and C, the best AGD (Point B) increases efficiency by 0.9 % under I_D spectrum amplitude-aligned condition and reduces I_D spectrum amplitude by 2.9 dBmA under efficiency-aligned condition.

Figs. 12 and 13 show the measured waveforms and I_D spectrums of Points A to C in Fig. 11 for S_{P1}, respectively. The best AGD (Point B) with t_1 = 94 ns, t_2 = 50 ns reduces I_D spectrum amplitude at 27 MHz by splitting the I_D overshoot into two peaks by inserting t_2 compared to Point A under efficiency-aligned condition. On the other hand, the best AGD (Point B) ($R_{G(ON)}$ = 60 Ω) achieves higher efficiency by driving the gate

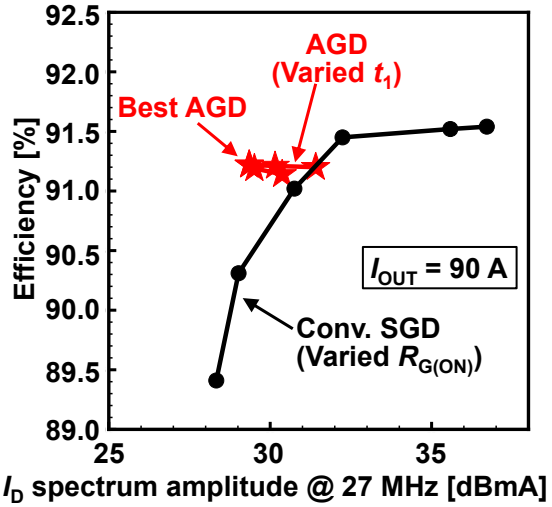


Fig. 10: Measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz at I_{OUT} = 90 A. In AGD, t_2 = 50 ns is fixed and t_1 is varied from 90 ns to 98 ns in 2 ns increments.

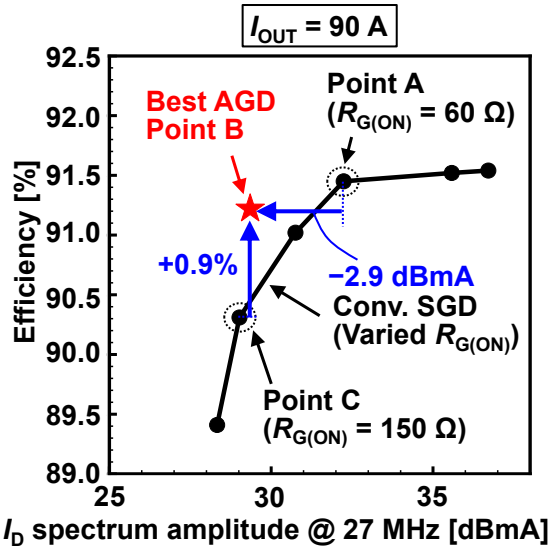


Fig. 11: Measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz at I_{OUT} = 90 A.

more strongly with lower $R_{G(ON)}$ than Point C ($R_{G(ON)}$ = 150 Ω) under I_D spectrum amplitude-aligned condition.

Fig. 14 shows an analysis of the power loss breakdown for Points B and C. Compared to the conventional Point C, the proposed best AGD (Point B) reduces switching losses by 45% from 27.9 W to 15.4 W, resulting in 10% reduction in total DC-DC converter losses from 128.8 W to 115.5 W and a 0.9% increase in converter efficiency from 90.3% to 91.2% under I_D spectrum amplitude-aligned condition.

C. Measured Results at I_{OUT} = 80 A

To investigate the I_{OUT} dependence of the parameters (t_1, t_2) of the best AGD and the performance improvement effect of

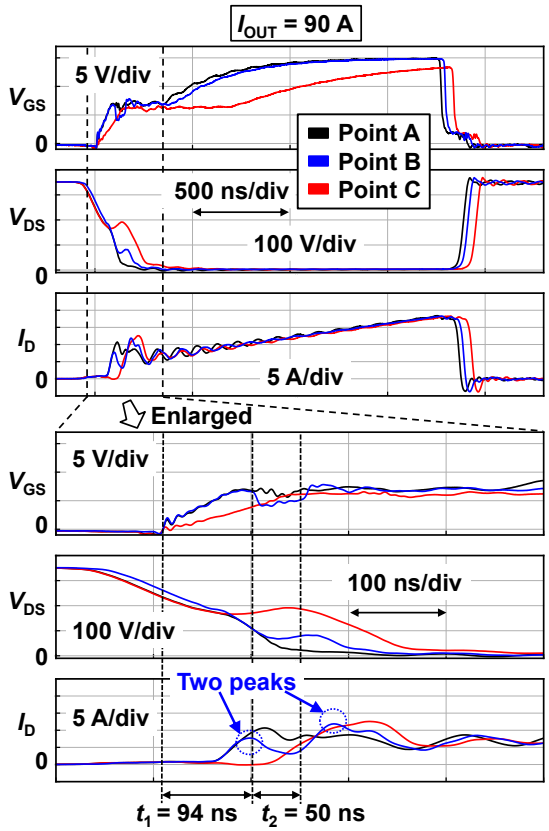


Fig. 12: Measured waveforms of Points A to C in Fig. 11 at I_{OUT} = 90 A.

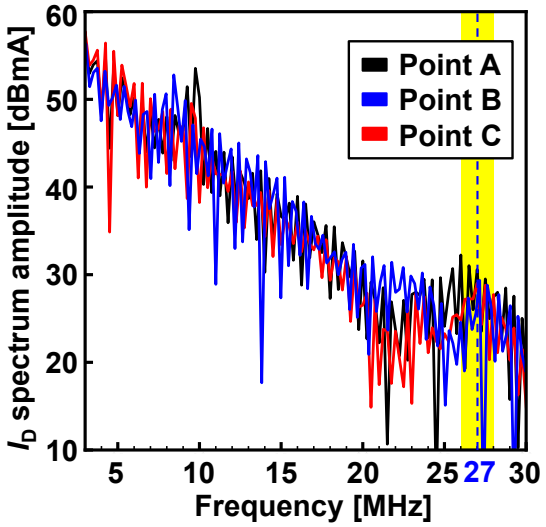


Fig. 13: Measured I_D spectrums of Points A to C in Fig. 11 at I_{OUT} = 90 A.

AGD, the measurement results at I_{OUT} = 80 A are presented in this section. Fig. 15 shows the measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz in SGD and the best AGD at I_{OUT} = 80 A. The similar AGD performance improvement effect is obtained for I_{OUT} = 80 A as for I_{OUT} = 90 A (Fig. 11). Points D and F are the conventional SGD points

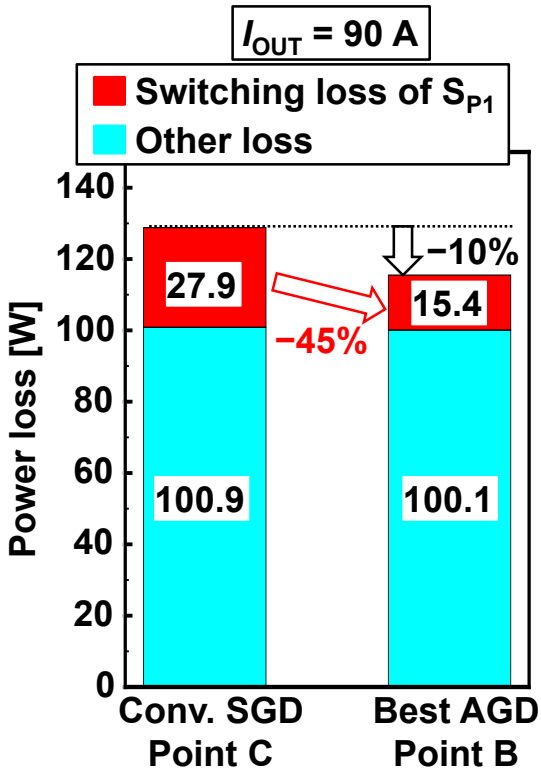


Fig. 14: Power loss breakdown for Points B and C at I_{OUT} = 90 A.

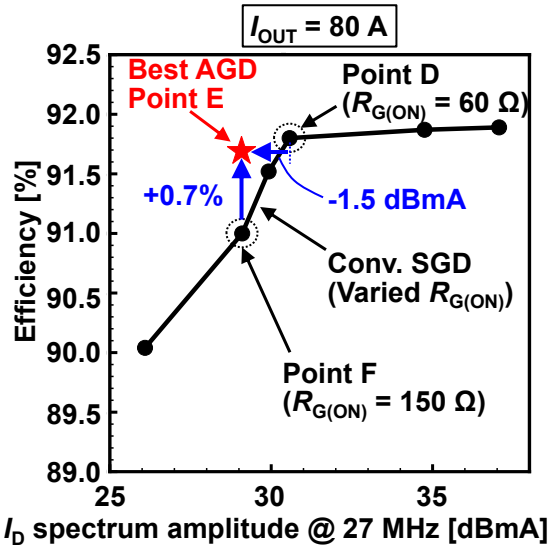


Fig. 15: Measured DC-DC converter efficiency vs. I_D spectrum amplitude of S_{P1} at 27 MHz at I_{OUT} = 80 A.

with efficiency and I_D spectrum amplitude approximately the same as the best AGD (Point E), respectively. Compared with Points D and F, the best AGD (Point E) increases efficiency by 0.7 % under I_D spectrum amplitude-aligned condition and reduces I_D spectrum amplitude by 1.5 dBmA under efficiency-aligned condition.

Fig. 16 shows the measured waveforms of Points D to F in Fig. 15 for S_{P1}. In the best AGD, (t_1, t_2) = (72 ns, 40 ns) at I_{OUT} = 80A in Fig. 16, while (t_1, t_2) = (94 ns, 50 ns) at I_{OUT} = 90A in Fig. 12. Note that (t_1, t_2) of the best AGD is different for I_{OUT} = 80 A and 90 A, which suggests that (t_1, t_2) of AGD needs to be changed depending on I_{OUT}. The theory of how to determine (t_1, t_2) is a future research challenge.

Fig. 17 shows an analysis of the power loss breakdown for Points E and F at I_{OUT} = 80 A. Compared to the conventional Point F, the proposed best AGD (Point E) reduces switching losses by 41% from 24.4 W to 14.4 W, resulting in 8% reduction in total DC-DC converter losses from 105.2 W to 96.4 W and a 0.9% increase in converter efficiency from 91.0% to 91.7% under I_D spectrum amplitude-aligned condition.

IV. Conclusions

TD AGD is applied to the 165 kHz, 350 V-to-13.3 V isolated DC-DC converter product for electric vehicles, and the efficiency increase of the converter by AGD is demonstrated by measurements at 1.2 kW (= 13.3 V, 90 A) output. Compared to the conventional SGD, the proposed TD AGD with (t_1, t_2) = (94 ns, 50 ns) reduces switching losses by 45% from 27.9 W to 15.4 W, resulting in 10% reduction in total DC-DC converter losses from 128.8 W to 115.5 W and a 0.9% increase in converter efficiency from 90.3% to 91.2% under I_D spectrum amplitude-aligned condition.

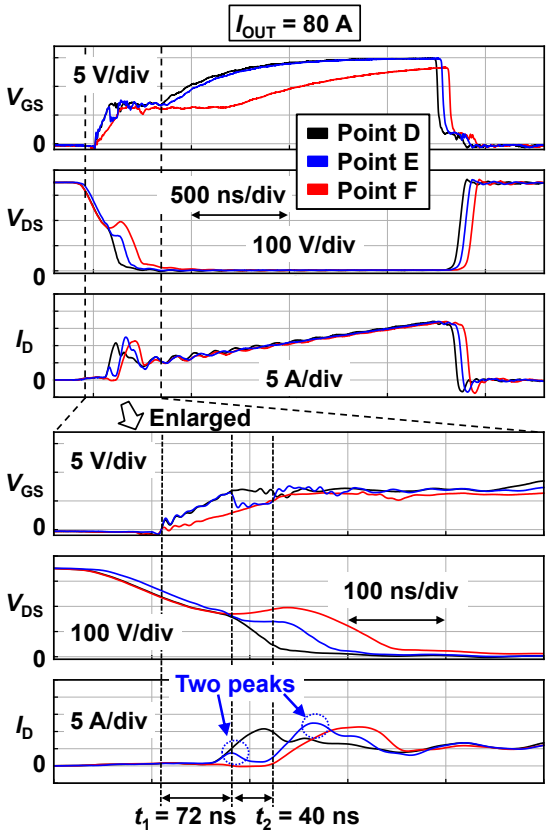


Fig. 16: Measured waveforms of Points D to F in Fig. 15 at I_{OUT} = 80 A.

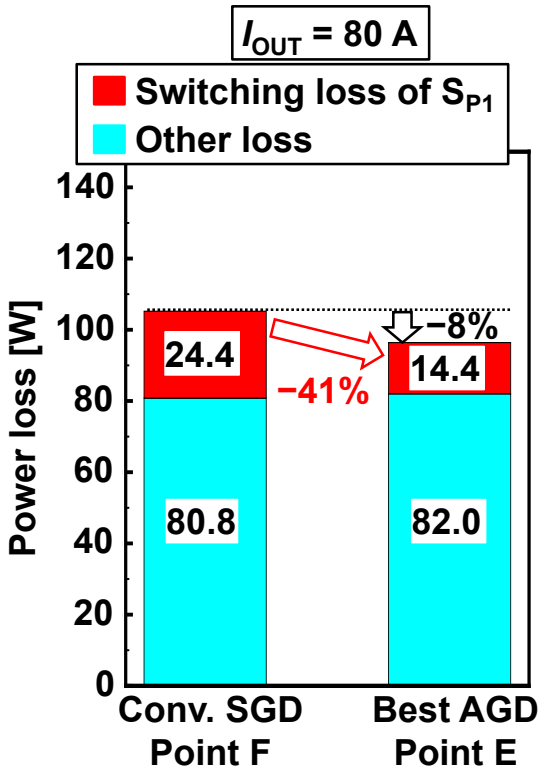


Fig. 17: Power loss breakdown for Points E and F at I_{OUT} = 80 A.

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