Closed-Loop Active Gate Driver IC With Gate Current Control When Collector Current Equals Load Current

Yaogan Liang, Yohei Sukita, Michihiro Ide, Makoto Takamiya

The University of Tokyo, Tokyo, Japan

***Abstract*— In order to reduce the switching loss (E_{LOSS}) of power devices at different load current (I_L) conditions, a closed-loop active gate driver (AGD) IC for IGBTs with novel integrated sensing functions is proposed to automatically optimize the gate driving pattern as I_L changes. The proposed AGD IC can change I_G when the collector current equals I_L by sensing and integrating the induced voltage between the Kelvin emitter and power emitter terminals during switching transient. In the switching measurements of IGBTs at 600 V using AGD IC fabricated with 180 nm BCD process, compared with the conventional single-step gate driving, the proposed AGD reduces E_{LOSS} by 20%, 24%, and 27% at I_L of 50 A, 75 A, and 100 A, respectively.**

***Keywords*— active gate driver, switching loss, closed-loop**

I. Introduction

Active gate driver (AGD), which changes the gate driving strength multiple times in fine time slots during the switching period of power devices, is attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching. AGD with closed-loop instead of open-loop is essential to cope with operating condition variations such as load current and temperature. A time-domain stop-and-go active gate driver (TD AGD) is attracting attention as a method of AGD suitable for single-chip integration of closed-loop AGD. Fig. 1 (a) shows the working principle of TD AGD, where the gate driving strength is changed three times from "strong to high-Z to strong" or "strong to weak to strong", and in this paper, the time for the first and second drive slot are defined as t_1 and t_2, respectively. Table I shows published closed-loop TD AGD ICs [1-3] and Fig. 1 (b) shows the methods of determining t_1 and t_2 [1-3]. In [4], it is shown that in order to minimize the switching loss (E_{LOSS}) in IGBT turn-on phase under collector current overshoot ($I_{OVERSHOOT}$)-alignment condition, the end timing of t_1 is the moment when the collector current (I_C) equals the load current (I_L) and the end timing of t_2 is the moment of the peak of I_C as shown in Fig. 1 (b). The validity of this method is supported by open-loop

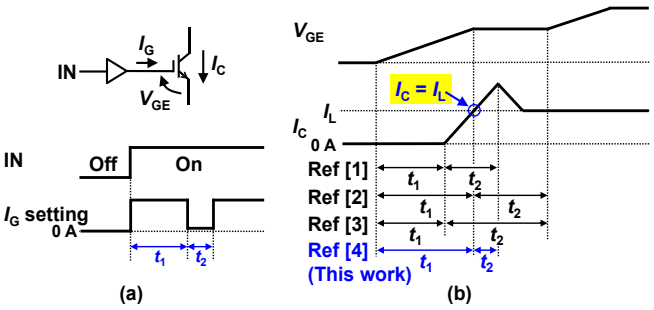

Fig. 1. Time-domain stop-and-go active gate driver (TD AGD). (a) Definition. (b) Methods of determining t_1 and t_2.

TABLE II. Comparison of Closed-Loop TD AGD ICs

	APEC'23 [1]	TIE'23 [2]	ISPSD'24 [3]	This work
Target power device	IGBT	GaN	SiC	IGBT
Measured conditions	600 V, 80 A	400 V, 10 A	Simulated	600 V, 100 A
Sensor input	V_{eE}	V_{DS}	V_{DS}, V_{ss} (1)	V_{ESS}
$I_C = I_L$ sensing	No	No	No	Yes
Real-time control	Yes	Yes	No	Yes
I_G levels	6 bit	3	NA	6 bit
IC Process	180 nm BCD	500 nm, 600 V SOI	180 nm BCD	180 nm BCD

(1) Voltage between power source and Kelvin source

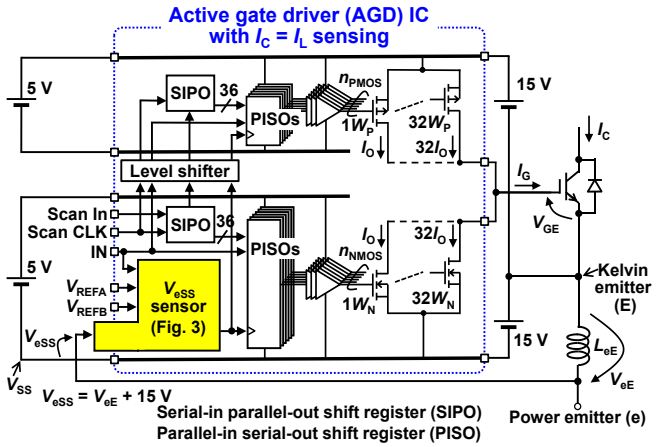

Fig. 2. Circuit schematic of proposed TD AGD IC with $I_C = I_L$ sensing.

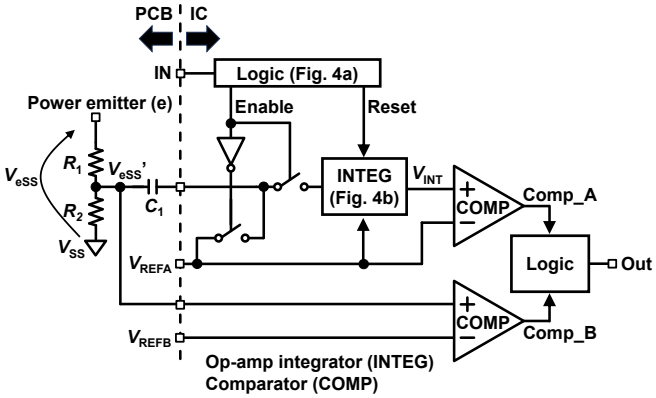

Fig. 3. Circuit schematic of proposed V_{ESS} sensor.

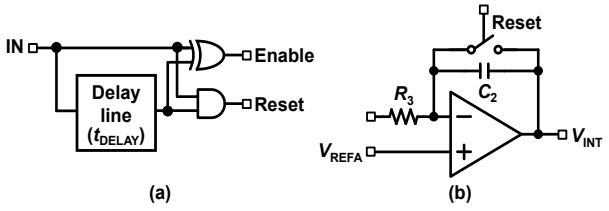

Fig. 4. Circuit schematics of (a) logic circuit and (b) op-amp integrator in V_{ESS} sensor.

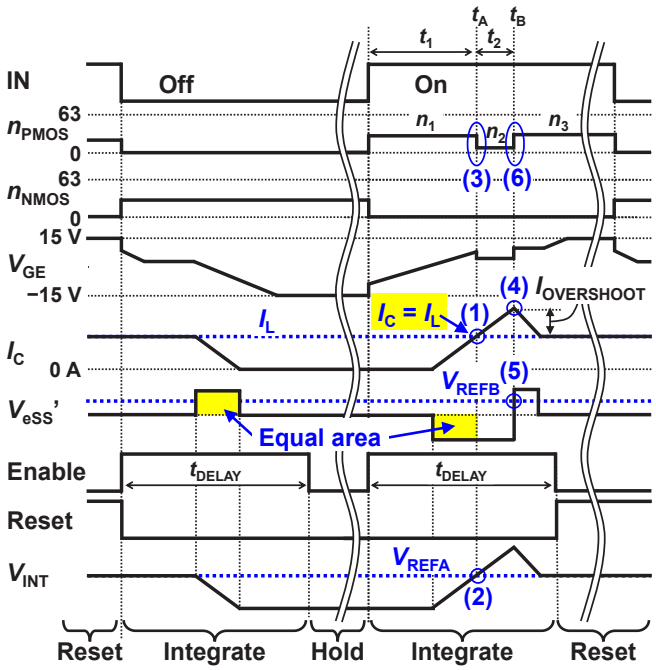

Fig. 5. Timing chart of proposed TD AGD IC with $I_C = I_L$ sensing.

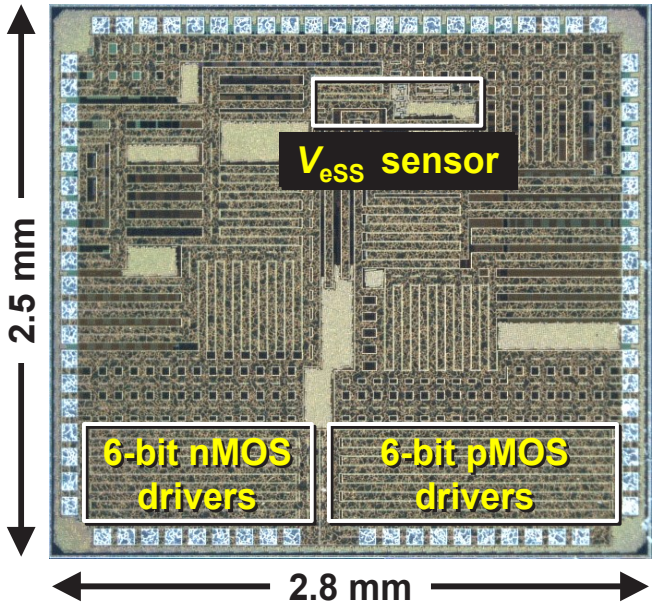

Fig. 6. Die photo of AGD IC.

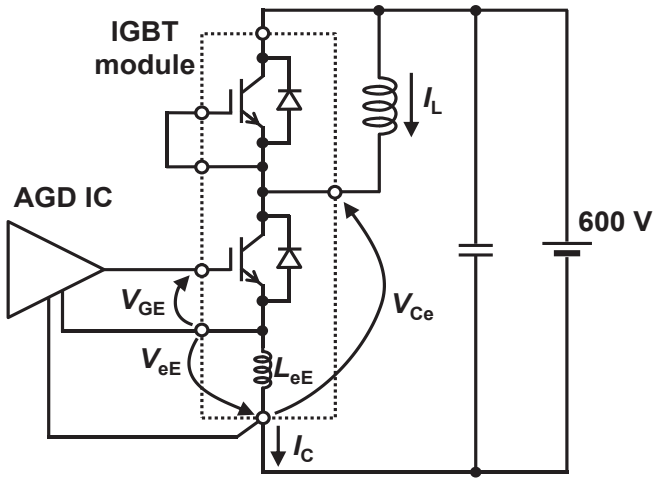

Fig. 7. Circuit schematic of double pulse test.

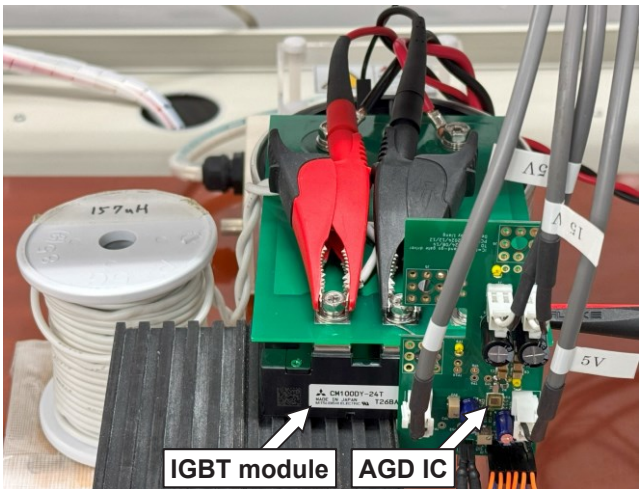

Fig. 8. Photo of measurement setup.

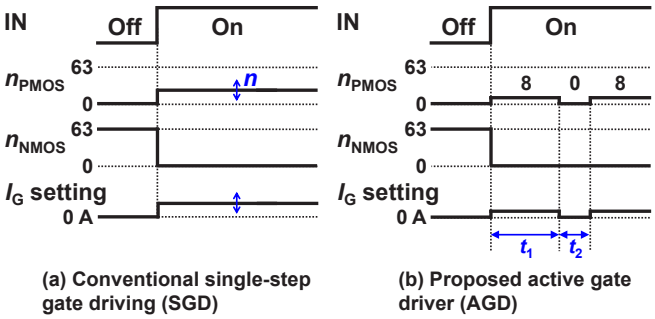

Fig. 9. Timing charts of SGD and AGD for comparison.

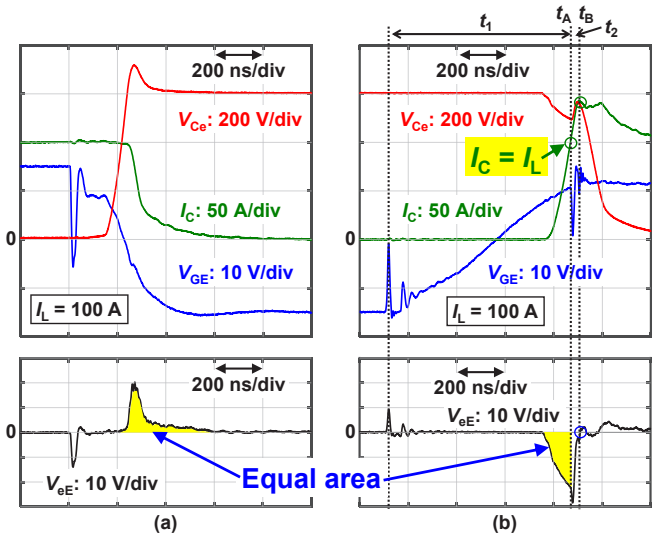

Fig. 10. Measured waveforms at I_L = 100 A. (a) Turn-off. (b) Turn-on.

measurements [4]. Therefore, in this paper, a closed-loop TD AGD IC that integrates the methods in [4] is developed. The challenge in IC design is how to sense $I_C = I_L$ to determine t_1. Adding Rogowski coils and shunt resistors for I_C measurement is not desirable because of the space cost and energy loss. Therefore, an integrated solution for sensing $I_C = I_L$ is proposed in this paper.

II. Active Gate Driver IC With $I_C = I_L$ Sensing

Figs. 2 to 5 show circuit schematics and a timing chart of the proposed closed-loop TD AGD IC with $I_C = I_L$ sensing. The proposed IC includes the V_{eSS} sensor to determine t_1 and t_2, controller for the state change, and a 6-bit digital gate

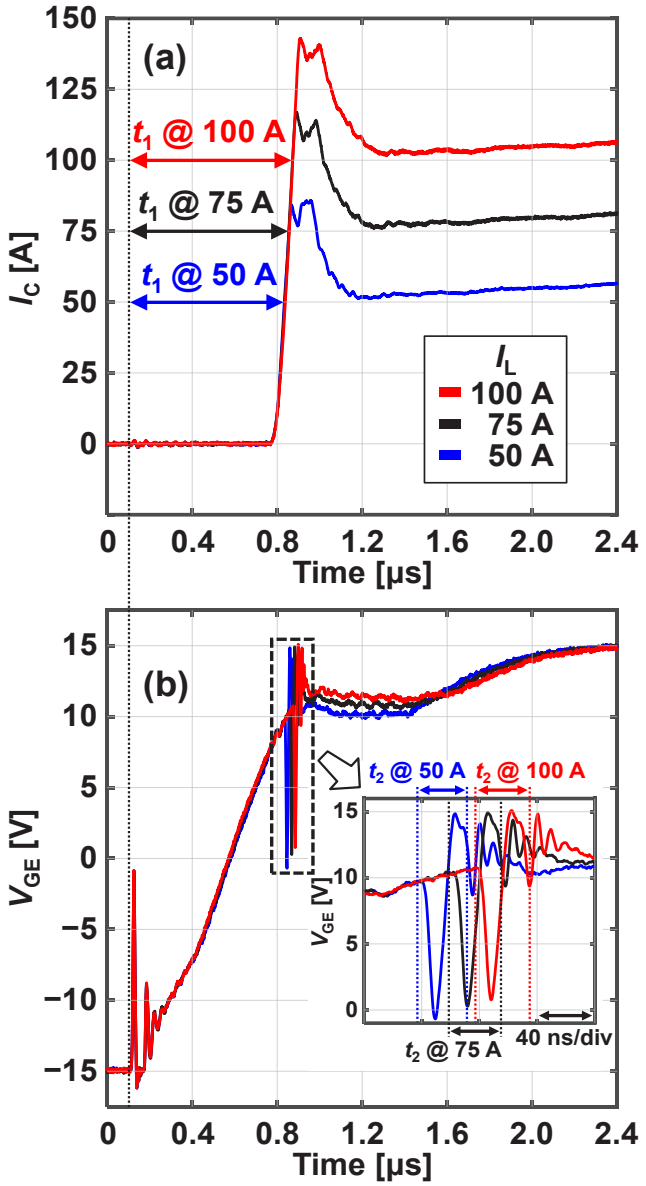

Fig. 11. Measured (a) I_C and (b) V_{GE} waveforms with varied I_L of 50 A, 75 A, and 100 A.

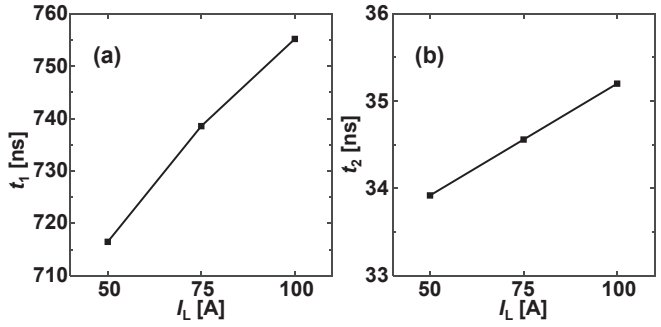

Fig. 12. Measured I_L dependence of (a) t_1 and (b) t_2.

driver with the gate current (I_G) in 64 levels, $I_G = n_{PMOS} \times 143$ mA and n_{PMOS} is an integer from 0 to 63. At turn-on, an active gate driving is performed in three slots with different I_G of strong (n_1) -weak (n_2) -strong (n_3). n_1 to n_3 are preset by a digital input (Scan In), while t_1 and t_2 are automatically determined by the V_{ESS} sensor. This paper will focus on the development of V_{ESS} sensor, because the other circuits in Fig. 2 are almost the same as [1]. The power emitter terminal is connected to the V_{ESS} sensor, and the input voltage (V_{ESS}) is V_{EE} + 15 V, where V_{EE} is the voltage between the Kelvin emitter and power emitter terminals (Fig. 2). Since the input voltage of IC must be below 5 V, the attenuator consisting of R_1 and R_2 attenuates V_{ESS} to V_{ESS}' by a factor of 1/6 (Fig. 3). Since V_{EE} is proportional to dI_C / dt, integrating V_{ESS}' using an op-amp integrator results in an integral output (V_{INT}) waveform proportional to I_C (Figs. 2 to 5). Thus, the I_L information can be sensed as the V_{INT} amplitude at turn-off (Fig. 5). In turn-on, the moment when V_{INT} returns to its initial value (V_{REFA}), i.e., the moment when the integral area of V_{ESS}' in turn-off becomes equal to the integral area of V_{ESS}' in turn-on, is the moment of $I_C = I_L$ (Fig. 5). Thus, the end timing of t_1 (t_A) is detected by comparing V_{INT} and V_{REFA} with a comparator (Figs. 3 and 5). The detection method for the end timing of t_2 (t_B) is the same as in [1]. The IC compares V_{ESS}' with the reference voltage (V_{REFB}) to find the peak of I_C waveform. To avoid accumulation of integration errors due to op-amp offsets, the op-amp integrator is operated in three modes: "Reset", "Integrate", and "Hold" (Figs. 3 to 5). Fig. 6 shows a die photo of AGD IC fabricated with 180-nm BCD process.

III. Measurement Results

Figs. 7 and 8 show a circuit schematic and a measurement setup of the double pulse test at 600 V using the developed AGD IC and an IGBT module (CM100DY-24T, 1200 V, 100 A rating), respectively. Figs. 9 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and the proposed AGD for comparison, respectively. In SGD, n is varied, which emulates a conventional gate driver with varied gate resistance. In AGD, (n_1, n_2, n_3) are preset to (8, 0, 8), and t_1 and t_2 are automatically determined by the V_{ESS} sensor. Fig. 10 shows the measured waveforms corresponding to Fig. 5 at I_L = 100 A. The proposed V_{ESS} sensor successfully detects t_A, where $I_C = I_L$, and t_B, where I_C peaks, exactly as the design intent in [4] in Fig. 1 (b) and Fig. 5. Figs. 11 (a) and (b) show the measured I_C and V_{GE} waveforms with varied I_L of 50 A, 75 A, and 100 A, respectively. Figs. 12 (a) and (b) show the measured I_L dependence of t_1 and t_2, respectively. The automatic adjustment of t_1 and t_2 in response to I_L changes is clearly indicated. Figs. 13 (a) to (c) show the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the conventional SGD and the proposed AGD at I_L = 50 A, 75 A, and 100 A, respectively. In SGD, n is varied from 3 to 14. By automatically tuning t_1 and t_2 as shown in Fig. 11, compared with the conventional SGD, the proposed AGD reduces E_{LOSS} by 20 %, 24 %, and 27 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 30 %, 26 %, and 28 % under E_{LOSS}-aligned condition at I_L = 50 A, 75 A, and 100 A, respectively. In Fig. 13 (c), Points A to C are defined, where Point B is the proposed AGD, Point A is SGD with closest $I_{OVERSHOOT}$ comparing to Point B, and Point C is SGD with the closest E_{LOSS} comparing to Point B. Figs. 14 (a) to (c) show the measured waveforms of Points A to C in Fig. 13 (c) at I_L = 100 A, respectively. In Point B, the proposed V_{ESS} sensor successfully detects t_A, where $I_C = I_L$, and t_B, where I_C peaks. By using TD AGD with (n_1, n_2, n_3) = (8, 0, 8), the proposed Point B reduces E_{LOSS} from 15 mJ to 11 mJ compared to Point A under $I_{OVERSHOOT}$-aligned condition, and reduces $I_{OVERSHOOT}$ from 59 A to 43 A compared to Point C under E_{LOSS}-aligned condition. As shown in Table I, this work is the first to realize a closed-loop AGD IC that changes I_G at $I_C = I_L$ timing with the proposed integrated V_{ESS} sensor circuit.

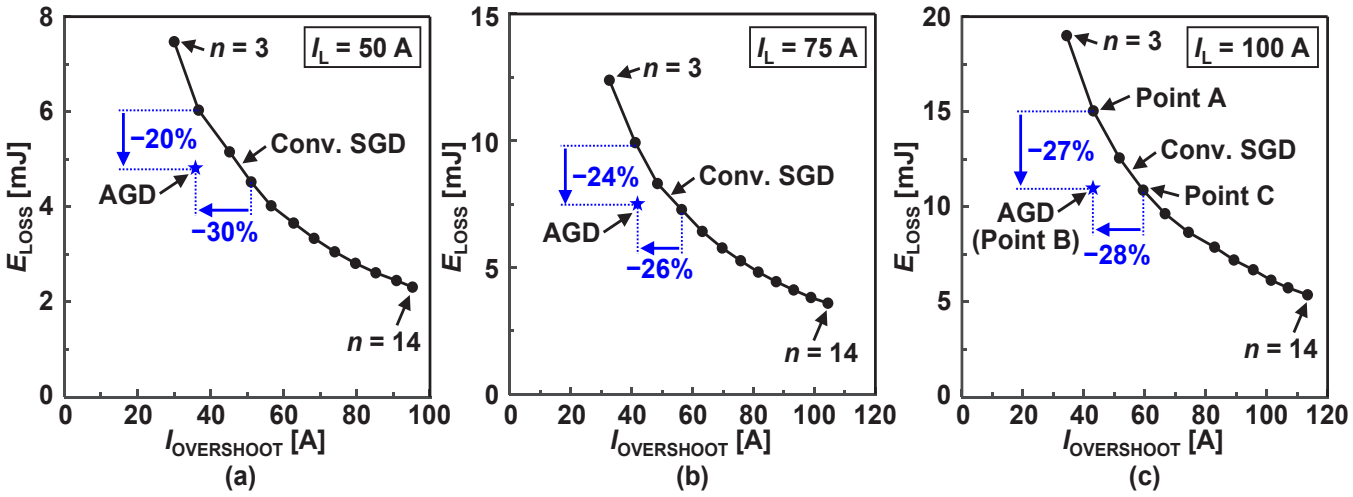

Fig. 13. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SGD and proposed AGD. (a) I_L =50 A. (b) I_L =75 A. (c) I_L =100 A.

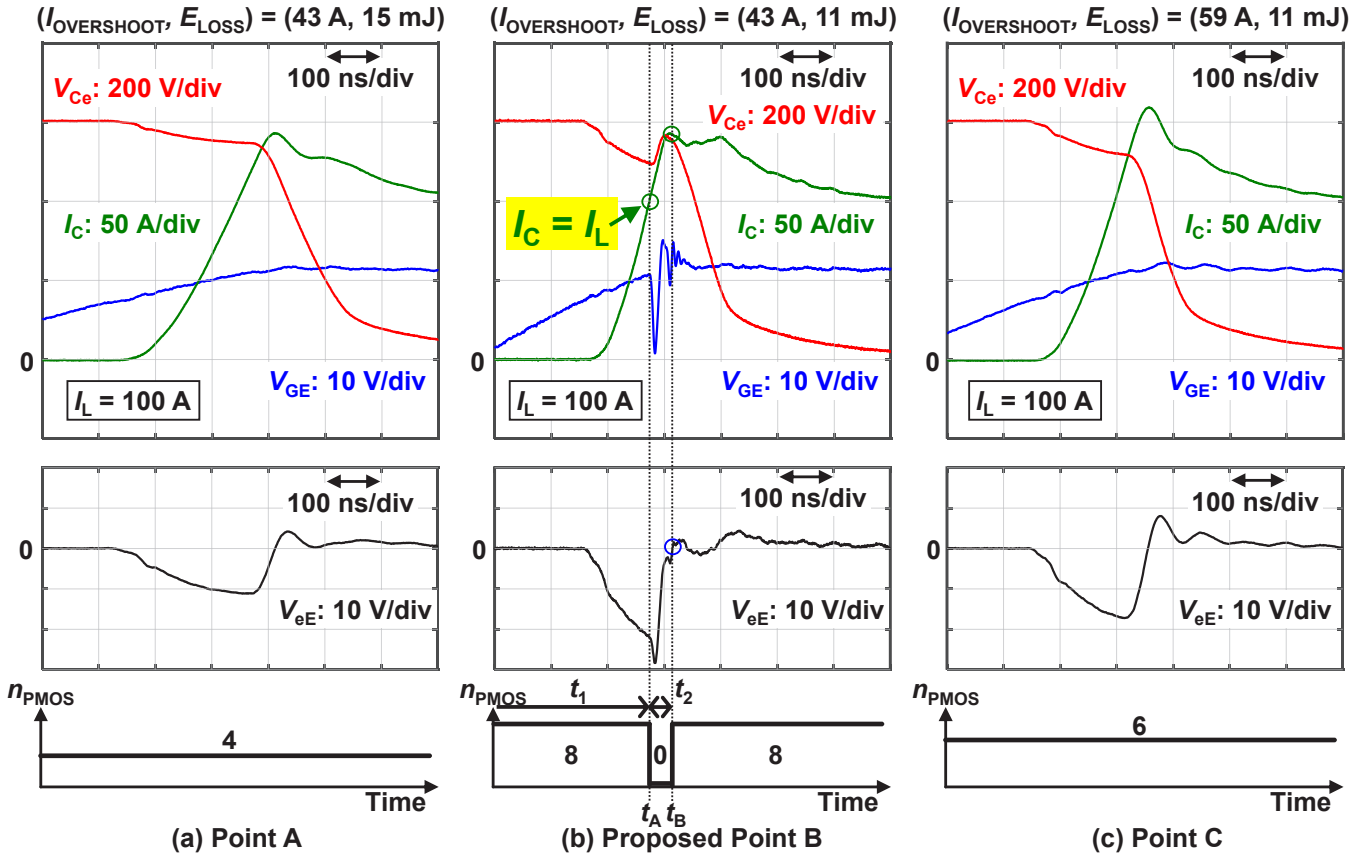

Fig. 14. Measured waveforms of Points A to C in Fig. 13 (c) at I_L = 100 A.

IV. Conclusions

The closed-loop time-domain stop-and-go AGD IC with $I_C = I_L$ sensing is proposed to constantly reduce E_{LOSS} under I_L variations. Compared with the conventional SGD, the proposed AGD reduces E_{LOSS} by 20 %, 24 %, and 27 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 30 %, 26 %, and 28 % under E_{LOSS}-aligned condition at I_L = 50 A, 75 A, and 100 A, respectively.

Acknowledgment

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References

[1] D. Zhang, K. Horii, K. Hata, and M. Takamiya, "Digital gate driver IC with fully integrated automatic timing control function in stop-and-go gate drive for IGBTs," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1225–1231.

[2] S. Yu, G. Shi, T. Wu, J. Zhu, L. Zhang, and W. Sun, "A 400-V half bridge gate driver for normallyoff GaN HEMTs with effective dv/dt control and high dv/dt immunity," *IEEE Trans. Ind. Electron.*,vol. 70, no. 1, pp. 741–751, 2023.

[3] R. Lai, Y. Yang, Y. Dai, J. Wu, Y. Shi, Z. Zhou, B. Zhang, H. Li, and X. Peng, "A quad-slope smart gate driver with mixed-signal auto-timing technique for power devices segment control," in *2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2024, pp. 347–350.

[4] Y. Sukita, K. Hata, K. Morokuma, Y. Wada, Y. Yamaoka, Y. Mukunoki, and M. Takamiya, "Method for determining optimum time in time-domain stop-and-go active gate driving," in *IEEE Southern Power Electronics Conference (SPEC)*, 2024, pp. 1-7.